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FIELD MAINTENANCE PRINT SET

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D-CS-AØ12-Ø-1	(ADV11) A-D FOR 11Ø3
D-UA-M8Ø12-Ø-Ø	(BDV11) BOOT TERMINATOR AND DIAGNOSTIC ROM
D-CS-M8Ø12-Ø-1	(BDV11) BOOT-TERMINATOR AND DIAGNOSTIC ROM
D-CS-M794Ø-Ø-1	(DLV11) SERIAL LINE UNIT
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D-CS-M8Ø43-Ø-1	(DLV11-J) 4 SERIAL LINE PER. CTLR
D-UA-5413679-0-0	(DLV11-KA) EIA-TO-2Ø MA CONVERTER
D-CS-5413679-0-1	(DLV11-KA) EIA-TO-2Ø MA CONVERTER
D-CS-M7941-Ø-1	(DRV11) PARALLEL LINE UNIT

UNIT VARIATIONS COVERED BY THIS PRINT SET

ET-LSI-11

Field Maintenance Print Set

Digital Equipment Corporation

FIELD MAINTENANCE PRINT SET
ORDER NO. MPØØ7Ø6

SIZE B | CODE TC | NUMBER ETLSI11-0-0 | REV. D

REVISIONS			
REV	C	D	
CHG. NO.	ORIGINATED	ETLSI11-MR001	
DATE	21 DEC 81		

USED ON OPTION/MODEL	
ET-LSI-11	
SHEET 1 OF 3	

DRN. R.H.	DATE 9OCT78	digital
CHK'D D.SCHANIN	DATE 12OCT78	TITLE: ET-LSI-11 FIELD MAINTENANCE PRINT SET
PROJ. ENG. D.SCHANIN	DATE 12OCT78	
FIELD SERV. G.NEALAND	DATE 12OCT78	

SIZE	CODE	NUMBER	REV.
B	TC	ETLSI11-0-0	D

DIST.

DRB 124

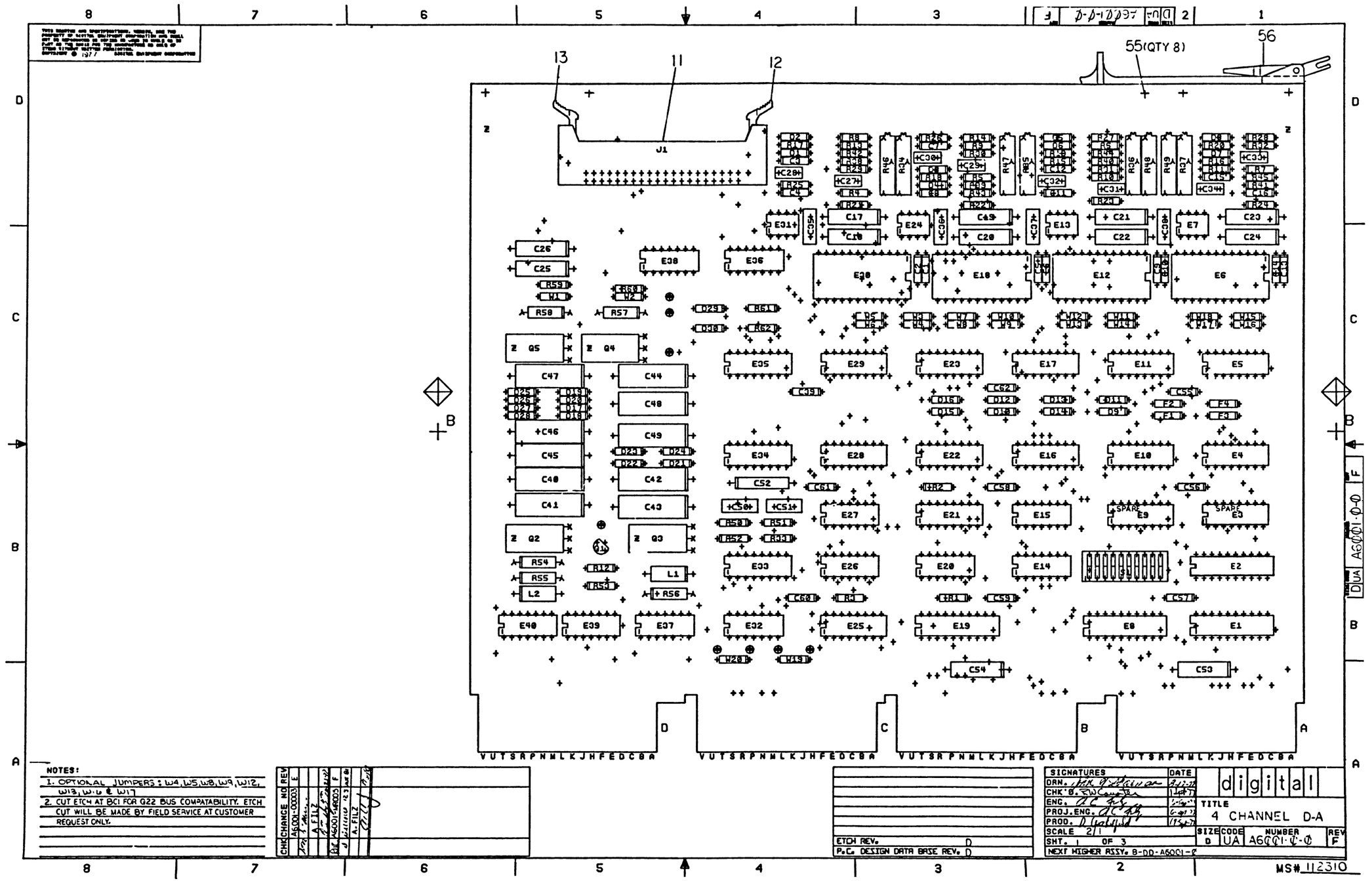
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D-UA-M795Ø-Ø-Ø	(DRV11-B) LSI-11 DMA INTERFACE
D-CS-M795Ø-Ø-1	(DRV11-B) LSI-11 DMA INTERFACE
D-UA-M8Ø49-Ø-Ø	DRV11-J
D-CS-M8Ø49-Ø-1	DRV11-J
D-UA-M794 8-Ø-Ø	(DRV11-P) LSI-11 FOUNDATION MODULE
D-CS-M7948-Ø-1	(DRV11-P) LSI-11 FOUNDATION MODULE
D-UA-M7951-Ø-Ø	(DUV11) LSI SYNC INTERFACE BOARD
D-CS-M7951-Ø-1	(DUV11) LSI-11 SYNC INTF
D-UA-M7957-Ø-Ø	(DZV11) ASYN MUX
D-CS-M7957-Ø-1	(DZV11) ASYN MUX
D-UA-M7954-Ø-Ø	(IBV11) LSI INTERFACE
D-CS-M7954-Ø-1	(IBV11) LSI11/IB INTERFACE
D-CS-M7264-Ø-1	(KD11-F) LSI-11 CPU MODULE
D-UA-M727Ø-Ø-Ø	(KD11-HA) LSI-11 CPU
D-EC-5013216-0-0	(KD11-HA) ETCH CUT DRAWING (M727Ø)
D-CS-M727Ø-Ø-1	(KD11-HA) LSI-11 CPU
D-UA-M8186-Ø-Ø	(KDF11-A) KDF11 CPU
D-EC-5013326-0-0	(KDF11-A) ETCH CUT DRAWING (M8186)
D-CS-M8186-Ø-1	(KDF11-A) KDF11-A CPU
D-UA-M8Ø16-Ø-Ø	(KPV11) POWER FAIL TIME CLOCK GEN.
D-CS-M8Ø16-Ø-1	(KPV11) POWER FAIL/LINE TIME CLK GENERATOR
D-UA-M8Ø18-Ø-Ø	(KUV11) WRITEABLE CONTROL STORE
D-CS-M8Ø18-Ø-1	(KUV11) WRITEABLE CONTROL STORE (WCS-LSI-11)
D-UA-M7952-Ø-Ø	(KWV11) PROG REAL TIME CLOCK
D-CS-M7952-Ø-1	(KWV11) PROG REAL TIME CLOCK
D-UA-M8Ø27-Ø-Ø	(LPV11) PRINTER INTERFACE
D-CS-M8Ø27-Ø-1	(LPV11) LPV11 PRINTER INTERFACE
D-CS-G653-Ø-1	MMV11-A 4K x 16 BIT MEMORY
D-CS-M7942-Ø-1	(MRV11-A) 4K/2K PROM
D-UA-M8Ø21-Ø-Ø	(MRV11-B) LSI11 UV PROM RAM
D-CS-M8Ø21-Ø-1	(MRV11-B) LSI11 UV PROM RAM
D-UA-M8Ø48-Ø-Ø	(MRV11-C) LSI11 ROM
D-CS-M8Ø48-Ø-1	(MRV11-C) LSI11 ROM
D-CS-M7944-Ø-1	(MSV11-B) 4K RAM
D-UA-M7955-Ø-Ø	MSV11-C MOS MEMORY, LSI
D-CS-M7955-Ø-1	MSV11-C MOS MEMORY, LSI
D-UA-M8Ø44-Ø-Ø	(MSV11-D) 32K 16 BIT MOS MEMORY
D-CS-M8Ø44-Ø-1	(MSV11-D) 32K 16 BIT MOS MEMORY
D-UA-M8Ø47-Ø-Ø	(MXV11-A) LSI-11 MEM & I/O
D-CS-M8Ø47-Ø-1	(MXV11-A) LSI-11 MEM AND I/O
D-UA-M94ØØ-Ø-Ø	(REV11) LSI REE BOOT CABLE CONN.
D-CS-M94ØØ-Ø-1	(REV11) LSI REF. BOOT CONN.
D-UA-M7269-Ø-Ø	(RKV11-D) RKV11 CONTROL
D-CS-M7269-Ø-1	(RKV11-D) RKV11-D CONTROL
D-UA-M8Ø14-Ø-Ø	RLV11 BUS CONTROL
D-UA-M8Ø13-Ø-Ø	RLV11 DISK CONTROL
D-CS-M8Ø14-Ø-1	RLV11 BUS CONTROL
D-CS-M8Ø13-Ø-1	RLV11 DISK CONTROL
D-CS-M7946-Ø-1	RXV11 LSI 11 INTERFACE
D-UA-M8Ø29-Ø-Ø	RXV21 LSI11 RXØ2 CONTROLLER
D-EC-5013080-0-0	(RXV21) ETCH CUT DRAWING (M8Ø29)
D-CS-M8Ø29-Ø-1	RXV21 LSI11 CONTROLLER
E-UA-5413489-0-0	(TU58) SERIAL TU58
D-CS-5413489-0-1	(TU58) TU58 ELECTRONICS:SERIAL
D-UA-M7142-Ø-Ø	VK17Ø SERIAL VIDEO BOARD
D-CS-M7142-Ø-1	VK17Ø SERIAL VIDEO MODULE

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D-UA-M8Ø2Ø-Ø-Ø	DPV11 (SYNC INTERFACE BOARD)
D-EC-5013326-0-0	(DPV11) ETCH CUT DRAWING (M8Ø2Ø)
D-CS-M8Ø2Ø-Ø-1	DPV11 LOGIC DIAGRAM
D-UA-M8188-Ø-Ø	FPF-11 (FLOATING POINT FOR LSI-11/23)
D-EC-5014348-0-0	(FPF11) ETCH CUT DRAWING (M8188)
D-CS-M8188-Ø-FPF1	(FPF11) CONTROL STORE
D-CS-M8188-Ø-FPF2	(FPF11) BYTES Ø & 7
D-CS-M8188-Ø-FPF3	(FPF11) BYTES 2 & 1
D-CS-M8188-Ø-FPF4	(FPF11) BYTES 4 & 3
D-CS-M8188-Ø-FPF5	(FPF11) BYTES 6 & 5
D-CS-M8188-Ø-FPF6	(FPF11) NADRS SEQUENCER
D-CS-M8188-Ø-FPF7	(FPF11) MIB INTERFACE
D-CS-M8188-Ø-FPF8	(FPF11) DAL INTERFACE
D-CS-M8188-Ø-FPF9	(FPF11) RESTE, CSEL, MIB & DAL ENA LOGIC
D-CS-M8188-Ø-FPFA	(FPF11) T-BUS RESOURCES
D-CS-M8188-Ø-FPFB	(FPF11) MISC. SLICE LOGIC
D-CS-M8188-Ø-FPFC	(FPF11) CAP DRAW
D-UA-M8Ø63-Ø-Ø	KXT11-AA (SINGLE BOARD COMPUTER)
D-EC-5014484-0-0	(KXT11-AA) ETCH CUT DRAWING (M8Ø63)
D-CS-M8Ø63-Ø-KXT1	KXT11-AA CPU
D-CS-M8Ø63-Ø-KXT2	KXT11-AA CLOCK CONTROL
D-CS-M8Ø63-Ø-KXT3	KXT11-AA BUS CONTROL
D-CS-M8Ø63-Ø-KXT4	KXT11-AA BUS I/O
D-CS-M8Ø63-Ø-KXT5	KXT11-AA MEMORY
D-CS-M8Ø63-Ø-KXT6	KXT11-AA SERIAL I/O
D-CS-M8Ø63-Ø-KXT7	KXT11-AA PARALLEL I/O
D-UA-M8Ø59-Ø-Ø	(MSV11-L) 128K PAR/CSR MOS MEM
D-EC-5014144-0-0	(MSV11-L) ETCH CUT DRAWING (M8Ø59)
D-CS-M8Ø59-Ø-1	(MSV11-L) 128K PAR/CSR MOS MEM



NOTES:

1. OPTIONAL JUMPERS: W4, W5, W8, W9, W12, W13, W16 & W17
2. CUT ETCH AT BCI FOR G22 BUS COMPATABILITY. ETCH CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER REQUEST ONLY.

CHK	CHANGE NO	REV
	A5001-00003	E
	A FILE	
BJC	A6001-00003	F
	A FILE	

ETCH REV. D
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE
DRN.	
CHK'D.	
ENG.	
PROJ.ENG.	
PROD.	

digital

TITLE: 4 CHANNEL D-A

SCALE 2/1 | SIZE D | CODE UA | NUMBER A6001-0-0 | REV F

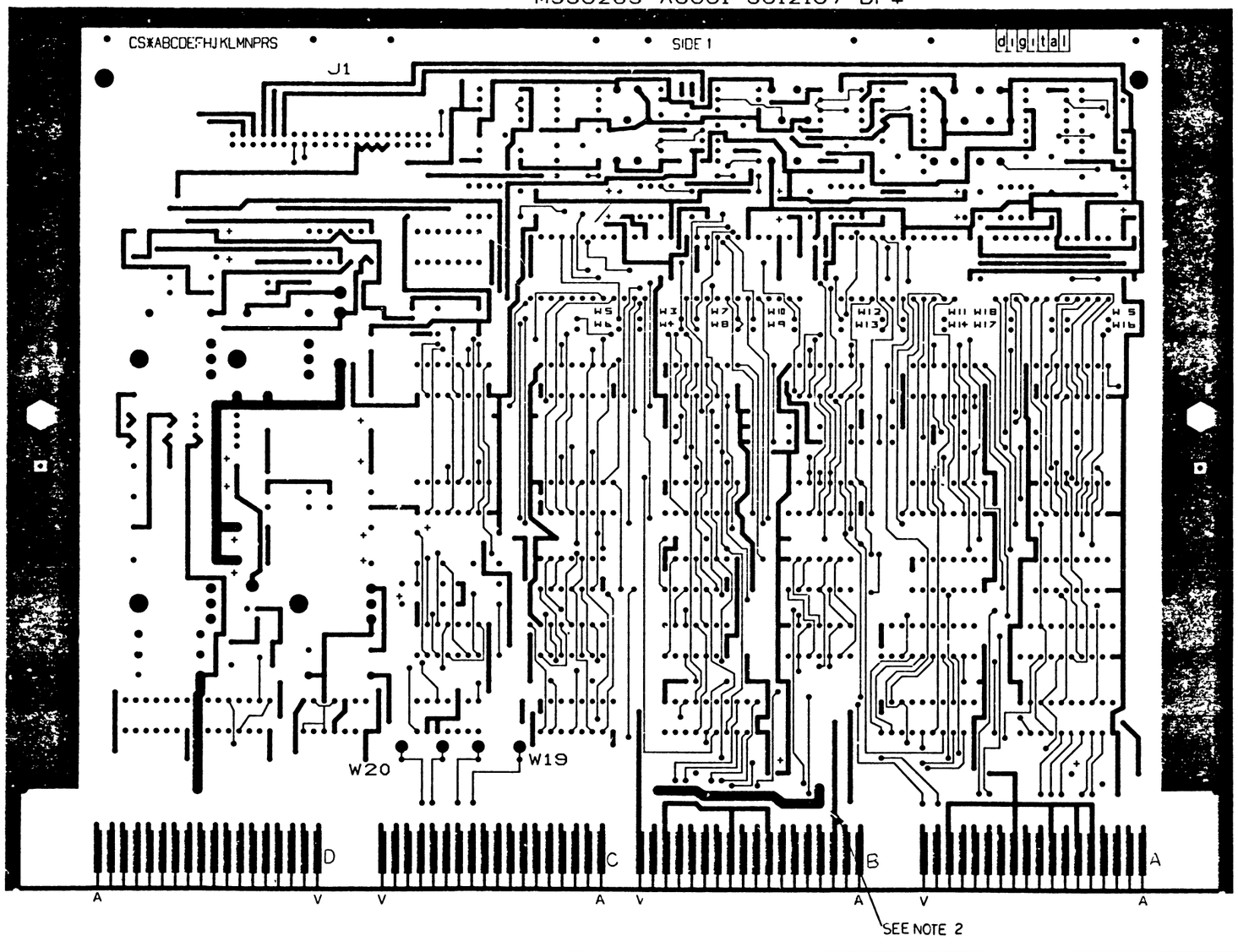
SHT. 1 OF 3

NEXT HIGHER ASSY. B-DD-A6001-0

MS# 112310

L1

MS30285 A6001 5012107 DP4

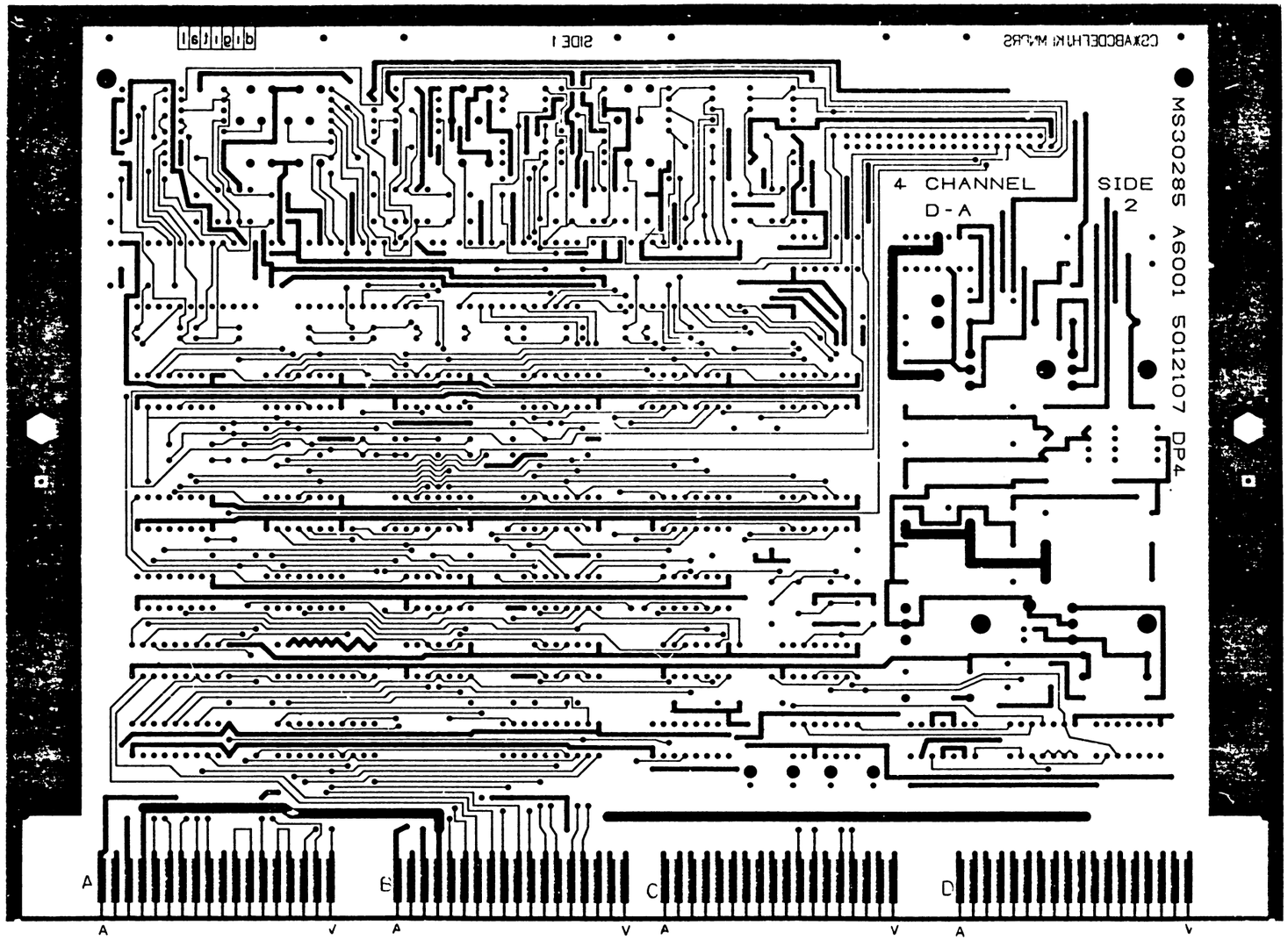


REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
4 CHANNEL D-A	D	UA	A6001-0-0	F
SCALE 2/1 SHEET 2 OF 3	DIST			

DUA6001-0-0 F

L2



REVISIONS		
CHG	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
4 CHANNEL D-A	D	UA	AECC1-C-C	F
SCALE -/1 SHEET 3 OF 3	DIST			

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8 7 6 5 4 3 2 1

D C B A

EDAL 11 L BR2 8 — BAD BD 11 H
BDAL 10 L BP2 9 — BAD BD 10 H
BDAL Φ9 L BN2 11 — BAD BD Φ9 H
BDAL Φ2 L BE2 12 — BAD BD Φ2 H
BDAL 12 L BS2 13
BAD XMIT H
BAD INWD L
S1 — JA3 JA2 JA1 MENB JAV3 JAV2 JAV1 XMIT REC — MATCH
DCΦΦ5 E19

BDAL Φ8 L BM2 8 — BAD BD Φ8 H
BDAL Φ7 L BL2 9 — BAD BD Φ7 H
BDAL Φ6 L BK2 11 — BAD BD Φ6 H
BDAL Φ1 L AV2 12 — BAD BD Φ1 H
DMA ON H
BAD XMIT H
BAD INWD L
S1 — JA3 JA2 JA1 MENB JAV3 JAV2 JAV1 XMIT REC — MATCH
DCΦΦ5 E8

BDAL Φ5 L BJ2 8 — BAD BD Φ5 H
BDAL Φ4 L BH2 9 — BAD BD Φ4 H
BDAL Φ3 L BF2 11 — BAD BD Φ3 H
BDAL ΦΦ L AU2 12 — BAD BD ΦΦ H
BBST L AP2 13
BAD XMIT H
BAD INWD L
S1 — JA3 JA2 JA1 MENB JAV3 JAV2 JAV1 XMIT REC — MATCH
DCΦΦ5 E2

BAD WR HB L
BAD DACØ L
BAD WR LB L
BAD DAC1 L
BAD DAC2 L
BAD DAC3 L
7432 E26 / 7432 E14
BAD LD DACØ L — BAD WR DACØ HB H
BAD LD DACØ L — BAD WR DACØ LB H
BAD LD DAC1 L — BAD WR DAC1 HB H
BAD LD DAC1 L — BAD WR DAC1 LB H
BAD LD DAC2 L — BAD WR DAC2 HB H
BAD LD DAC2 L — BAD WR DAC2 LB H
BAD LD DAC3 L — BAD WR DAC3 HB H
BAD LD DAC3 L — BAD WR DAC3 LB H
74ΦΦ E27 / 74ΦΦ E15

AR2 — AS2 — BIAK L
AM2 — AN2 — BDMG L
CP2 — W19 — CS2 — BIAK L
CM2 — W2Φ — CN2 — BDMG L

SSPARE 1 AE1
SSPARE 2 AF1
SSPARE 4 BC1
FOR TESTER USE
SEE NOTE 2

NOTES:
2. CUT ETCH AT BC1 FOR Q22 BUS COMPATABILITY. ETCH CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER REQUEST ONLY.

+5V — R1 1K — BAD XMIT H
ENB SYNC RXCX BRPLY — WTBT DOUT DIN VECTOR — DAL 2 DAL 1 DAL Φ — SEL 6 SEL 4 SEL 2 SEL Φ — OUTHB OUTLB INWD
DCΦΦ4 E1

BSYNC L AJ2 6 — BRPLY L 8 AF2
BD Φ2 H 2 — BAD DAC Φ L 17
BD Φ1 H 3 — BAD DAC1 L 16
BD ΦΦ H 4 — BAD DAC2 L 15
BAD DAC3 L 14
BWT BT L AK2 5
BDOUT L AE2 9 — BAD WRLB L 13
BDIN L AH2 7 — BAD WRHB L 12
BAD INWD L 11

AA2, BA2, BV1, DV1 — +5V
AC2, BC2, AJ1, BJ1, AM1, BM1, AT1, BT1
C53 15μF, C54 15μF, C55 .047μF, C39 .047μF, C56 THRU C62 .047μF

+5V — R3 10K — 74155 E25 — DMA ON H
fB3 fB2 fB1 fBΦ — DB DA — fA3 fA2 fA1 fAΦ — S1 SΦ
BAD LD DAC 3 L
BAD LD DAC 2 L
BAD LD DAC 1 L
BAD LD DAC Φ L

+5V — R2 10K — 8837 E21 — DMA ON H
B INIT L AT2 — BAD INIT H

BAD DACØ L
BAD INWD L
BAD DAC1 L
BAD DAC2 L
BAD DAC3 L
74Φ2 E2Φ
BAD READ DACØ L
BAD READ DACØ H
BAD READ DAC1 L
BAD READ DAC1 H
BAD READ DAC2 L
BAD READ DAC2 H
BAD READ DAC3 L
BAD READ DAC3 H

NOTE: 1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND	-VCC
16 PIN DIP	16	8	-
14 PIN DIP	14	7	-
DEC DCΦ4	18	9	-
DEC DCΦ5	20	10	-
2505	7	1	4
AD27ΦΦ	13	7	-

BUS & ADDRESS & DATA

REVISIONS			
CHK	CHANGE NO.	REV.	
JLF	ORIGINAL	B	
JLF	A6001-00001	C	
JLF	A6001-00002	D	
JLF	A6001-00003	E	
JLF	A6001-MM001	F	
JLF	A6001-MM005	H	

DRN		FIRST USED ON
CHK		digital
ENG		TITLE
PROJ. ENG		4 CHANNEL D-A (BAD)
PROD.		
NEXT HIGHER ASSY.		
B-DD-A6ØØ1-Ø		SIZE D CODE CS NUMBER A6ØØ1-Ø-1 REV. H
SCALE		
SHEET 1 OF 4		DIST

DEC FORM 852 DRD 1202

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NOTES

1. * DENOTES FUSIBLE RESISTOR

DAC Ø	VOLTAGE	DAC 1
W3 IN W4 OUT W5 IN W6 IN	±2.56V	W7 IN W8 OUT W9 IN W1Ø IN
W3 IN W4 OUT W5 OUT W6 IN	±5.12V	W7 IN W8 OUT W9 OUT W1Ø IN
W3 OUT W4 IN W5 OUT W6 IN	±1Ø.24V	W7 OUT W8 IN W9 OUT W1Ø IN
W3 IN W4 OUT W5 IN W6 OUT	Ø→+5.12V	W7 IN W8 IN W9 IN W1Ø OUT
W3 IN W4 OUT W5 OUT W6 OUT	Ø→+1Ø.24V	W7 IN W8 OUT W9 OUT W1Ø OUT

NOTES: 2. WHEN ADJUSTING FOR ±2.56 VOLTS BIPOLAR OR Ø→+5.12 VOLTS UNIPOLAR, REMOVE R21 OR R22 OF DACØ OR DAC1 RESPECTIVELY TO OBTAIN DESIRED RANGES AND REPLACE WITH JUMPER.

DACØ & DAC1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
4 CHANNEL D/A (DAD)	D	CS	A6ØØ1-Ø-1	H
SCALE	SHEET 2 OF 4		DIST.	

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NOTES
1. * DENOTES FUSIBLE RESISTOR

DAC 2	VOLTAGE	DAC 3
W11 IN W12 OUT W13 IN W14 IN	±2.56V	W15 IN W16 OUT W17 IN W18 IN
W11 IN W12 OUT W13 OUT W14 IN	±5.12V	W15 IN W16 OUT W17 OUT W18 IN
W11 OUT W12 IN W13 OUT W14 IN	±10.24V	W15 OUT W16 IN W17 OUT W18 IN
W11 IN W12 OUT W13 IN W14 OUT	0→+5.12V	W15 IN W16 OUT W17 IN W18 OUT
W11 IN W12 OUT W13 OUT W14 OUT	0→+10.24V	W15 IN W16 OUT W17 OUT W18 OUT

NOTES: 2. WHEN ADJUSTING FOR ±2.56 VOLTS BIPOLAR OR 0→+5.12 VOLTS UNIPOLAR, REMOVE R23 OR R24 OF DAC2 OR DAC3 RESPECTIVELY TO OBTAIN DESIRED RANGES AND REPLACE WITH JUMPER.

DAC2 & DAC3

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
4 CHANNEL D-A (DAY)	D	CS	A6001-0-1	H
SCALE	SHEET 3 OF 4	DIST.		

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NOTES:
1. * DENOTES FUSIBLE RESISTOR

AD2, BD2 +12V

PWR SW A L

PWR SW B L

+5V

+3VD

+20V

-20V

PWR +15V

PWR -15V

LM325N E38

REF

PWR SW A L

PWR SW B L

J1

DAY BIT 3 OUT
DAY BIT 2 OUT
DAY BIT 1 OUT
DAY BIT Φ OUT
DAY DAC3 OUT
DAY DAC2 OUT
DAD DAC1 OUT
DAD DACΦ OUT

DAD DAC1 HQ GND
DAY DAC2 HQ GND
DAY DAC3 HQ GND
PWR -15T
PWR +15T
DAD DACΦ HQ GND

POWER SUPPLY

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
4 CHANNEL D-A (PWR)	D	CS	A6001-0-1	H
SCALE	SHEET 4 OF 4	DIST		

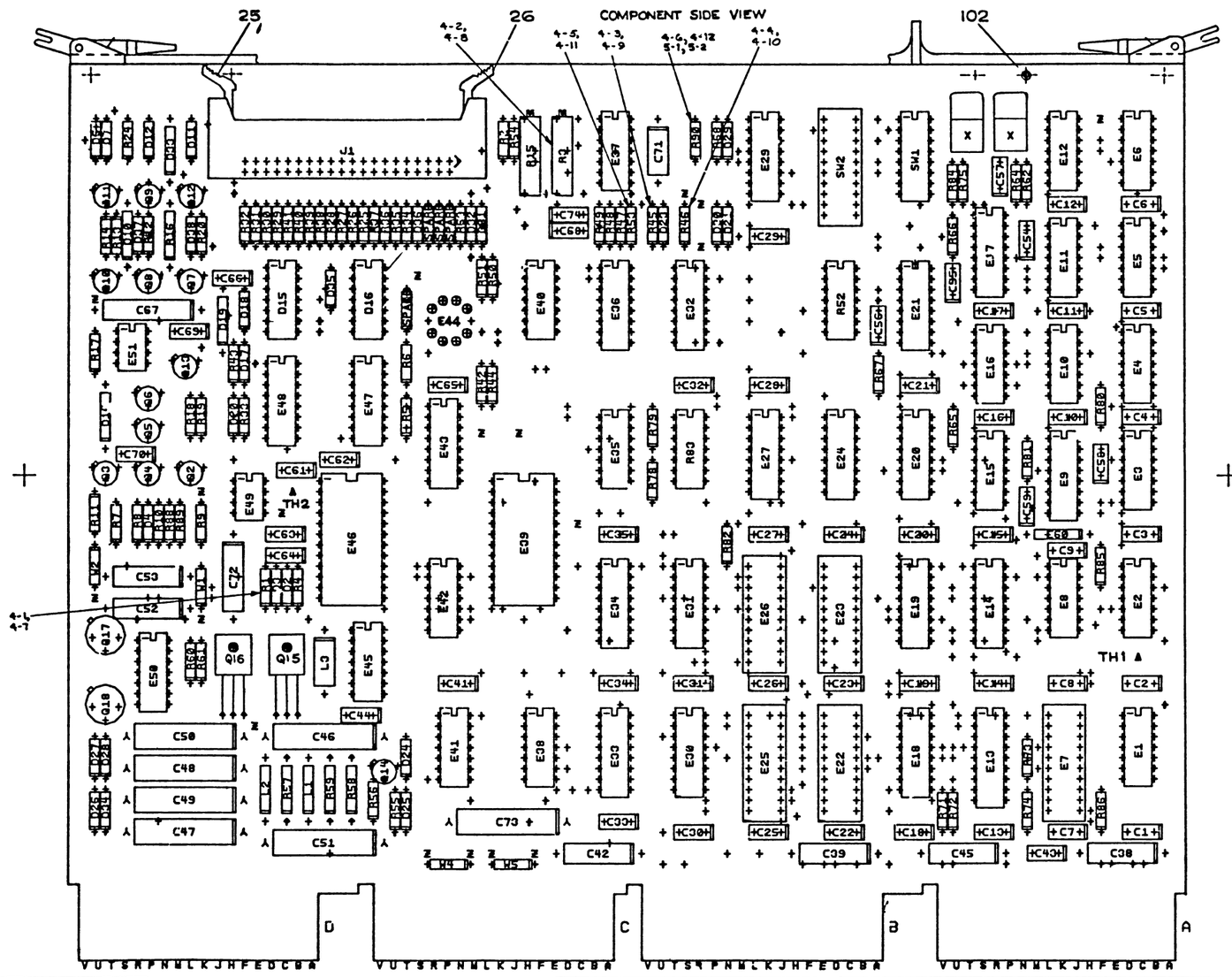
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REWORK INSTRUCTIONS
ECO #4

COMPONENT DELETES SIDE 1:
4-1. R1 (P/N 1302957)
4-2. R3 (P/N 1309143-04)
4-3. R45 (P/N 1302391)
4-4. R46 (P/N 1300479)
4-5. R53 (P/N 1304891)
4-6. R90 (P/N 1302396)

COMPONENT ADDS SIDE 1:
4-7. R1 (P/N 1303038)
4-8. R3 (P/N 1309143-05)
4-9. R45 (P/N 1309418)
4-10. R46 (P/N 1303312)
4-11. R53 (P/N 1302396)
4-12. R90 (P/N 1305425)

ECO #5
COMPONENT DELETES SIDE 1:
5-1. R90 (P/N 1305425)
COMPONENT ADDS SIDE 1:
5-2. R90 (P/N 1315012)



NOTES: 1. CUT ETCH AT BCI FOR Q22 BUS COMPATABILITY. ETCH CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER REQUEST ONLY.

CHK	CHANGE NO	REV
	A012-2124	E
	A012-00004	F
	A012-MR0005	H
	A012-MR0006	J

ETCH REV. E
P.C. DESIGN PATH BASE REV. E-P2

SIGNATURES	DATE
DRN. J. CARTER	4-12-77
CHK'D.	4-19-77
ENG.	4-19-77
PROJ. ENG.	4-14-77
PROD.	
SCALE 2/1	
SHT. 1 OF 3	

digital

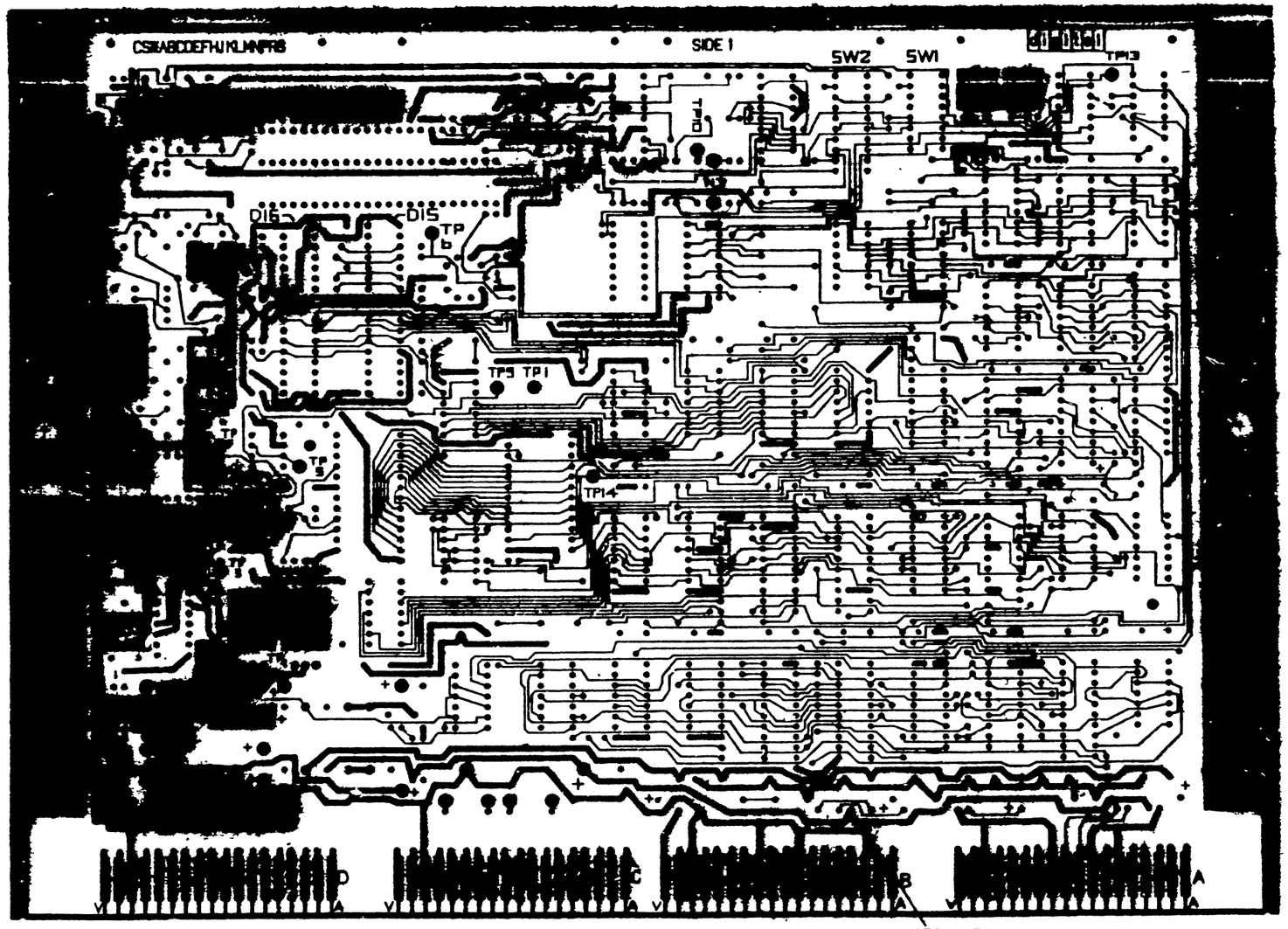
TITLE A-D FOR 1103

SIZE	CODE	NUMBER	REV
D	UA	A012-0-0	J

NEXT HIGHER ASSY. B-DD-A012-0

MS#_____

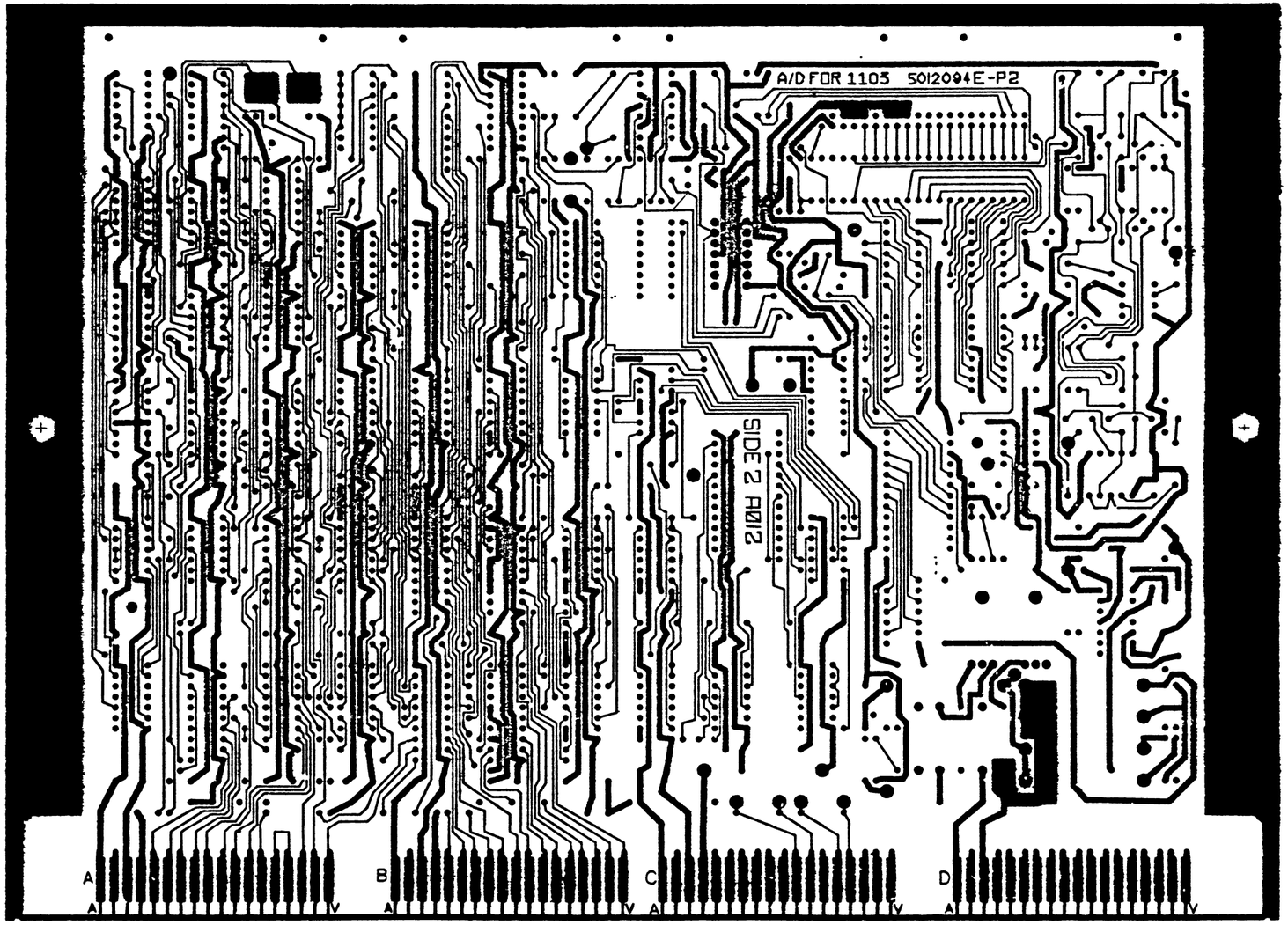
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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
A-D FOR 1103	D	UA	AØ12-Ø-Ø	J
SCALE 2/1 SHEET 2 OF 3	DIST			

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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
A-D FOR 1103	D	UA	AØ12-Ø-Ø	J
SCALE 2/1 SHEET 3 OF 3	DIST			

AØ12-Ø-Ø

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QBI READ CSR L
QBI BD 13 H
QBI BD 12 H
QBI READ CSR H
QBI INIT H
8556 E20
QBI MUX 5(1)H
QBI MUX 4(1)H

QBI READ CSR L
QBI BD 11 H
QBI BD 10 H
QBI BD 09 H
QBI BD 08 H
QBI READ CSR H
QBI WR CSR HB H
QBI INIT H
8556 E19
QBI MUX 3(1)H
QBI MUX 2(1)H
QBI MUX 1(1)H
QBI MUX 0(1)H

CAE ERROR(1)H
QBI EIE(1)H
CAE AD DONE(1)H
QBI DIE(1)H
CAE GO H
QBI READ CSR L
8Q97 E14
QBI BD 15 H
QBI BD 14 H
QBI BD 07 H
QBI BD 06 H
QBI BD 01 H
QBI BD 00 H

BDAL 15 L
BDAL 12 L
BDAL 11 L
BDAL 14 L
BUS 3
BUS 2
BUS 1
BUS 0
DAT 3
DAT 2
DAT 1
DAT 0
DC00S E26
QBI BD 15 H
QBI BD 12 H
QBI BD 11 H
QBI BD 14 H
JA3
JA2
JA1
MENB
MATCH
JAV3
JAV2
JAV1
XMIT REC
QBI XMIT H
QBI INWD L

BDAL 10 L
BDAL 09 L
BDAL 08 L
BDAL 13 L
QBI BD 10 H
QBI BD 09 H
QBI BD 08 H
QBI BD 13 H
DC00S E25

QBI VECTOR H
+5V
RS2 1K
QBI XMIT H
QBI INWD L

+5V
RS2 1K
QBI XMIT H
BSYNC L
ENB
SYNC
DC00S4 E7
DAL 2
DAL 1
DAL 0
QBI BD 01 H
QBI BD 00 H
BWTBT L
NTBT
DOUT
DIN
BDOUT L
BDIN L
QBI VECTOR H
VECTOR
RXCX
BRPLY
SEL 6
SEL 4
SEL 2
SEL 0
OUT HB
OUT LB
INWD
QBI BRPLY L
QBI CSR L
QBI DBR L
QBI WR LB L
QBI WR HB L
QBI INWD L

+5V
R73 330
AN2
QBI BIAKO L
R74 680
CAE AD DONE(1) H
QBI BD 06 H
QBIWR CSR LB H
BINIT L
QBI WR CSR HB H
QBI BD 14 H
CAE ERROR(1) H
ROSTA
A DATA
A CLK
BIAKO
BIAKI
BINIT
BDIN
B CLK
B DATA
ROSTB
DC00S3 E13
A ST
BIRQ
INITO
VECTOR
VEC B
B ST
QBI DIE (1) H
QBI BIRQ L
QBI INIT L
QBI VECTOR H
QBI VEC ROSTB H
QBI EIE (1) H
+5V
R71 330
AM2
R72 680
BIAKT L
QBI INITH

QBI READ CSR L
QBI BD 05 H
QBI BD 04 H
QBI BD 03 H
QBI BD 02 H
QBI READ CSR H
QBI AR CSR LB H
QBI INIT H
8556 E18
QBI CLK STARTS(1) H
QBI EXT STARTS(1) H
QBI MAINT AD TST(1) H
74Φ4 E38
QBI ID CODE L

QBI WR LB L
QBI DBR L
74Φ2 E2
QBI WR VERNIER H

CTL EOC L
CTL CLOCK H
QBI LD BUF H

QBI WR HB L
QBI CSR L
QBI WR LB L
QBI WR CSR HB H
QBI WR CSR LB H
74Φ8 E41
QBI WR CSR LB L
R84 1K
+5V

QBI CSR L
QBI INWD L
QBI DBR L
74Φ4 E8
QBI READ CSR L
QBI READ CSR H
QBI READ DBR L

BDAL 07 L
BDAL 06 L
BDAL 05 L
BDAL 00 L
BDAL 04 L
BDAL 03 L
BDAL 02 L
BDAL 01 L
BBS7 L
QBI VECTOR H
QBI VEC RQ STB H
DC00S5 E23
DC00S5 E22
QBI BD 07 H
QBI BD 06 H
QBI BD 05 H
QBI BD 00 H
QBI BD 04 H
QBI BD 03 H
QBI BD 02 H
QBI BD 01 H

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	+VCC	GND
16 PIN DIP	16	8	7
19 PIN DIP	19	10	9
AM 2504	24	12	12
DC00S3	18	9	9
DC00S4 *	28	14	14
DC00S5	20	10	10
IC 2581	1	7	4
IC 3481			
IC LM323K	4	7	11
IC 2588	4	7	11

CHG	CHANGE NO	REV
	A012-00002	D
	A012-00002A	
	A012-00004	E
	A012-MR005	F
	A012-MR006	H

(QBI)

SIGNATURES	DATE
DRN. G.S.	8 MAY 76
CHK'D.	11 MAY 76
ENG.	11 MAY 76
PROJ. ENG.	11 MAY 76
PROD.	11 MAY 76

digital

TITLE: A-D FOR 1103

SCALE | SIZE D | CODE CS | NUMBER A012-0-1 | REV H

SHT. 1 OF 6

ETCH REV | FIRST USED ON

MS#

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CAE DEL HOLD H
CTL CLOCK H
74S00 E6
CAE HOLD (Ø) L
8231 E3
+3V
TP14 TPTR
TP13 TPC
ADC COMP H
74Ø1 E15
74Ø4 E8
QBI MAINT AD TST (1) H
QBI MUX Ø (1) H
R92 1K
+5V
AM25Ø4 SAR E39
MSB
LSB
CC
CTL SAR 11 H
CTL SAR 11 L
CTL SAR 1Ø L
CTL SAR Ø9 L
CTL SAR Ø8 L
CTL SAR Ø7 L
CTL SAR Ø6 L
CTL SAR Ø5 L
CTL SAR Ø4 L
CTL SAR Ø3 L
CTL SAR Ø2 L
CTL SAR Ø1 L
CTL SAR ØØ L
CTL EOC L
+5V
C58 22Ø pF
R8Ø 6.81K
C59 22Ø pF
R81 6.81K
T3 74LS221 E9
T2 74LS221 E9
C60 1 µF
R85 2K
R86 1K
AK1
AL1
CTL CLOCK L
CTL CLOCK H
QBI BD Ø7 H
QBI BD Ø6 H
QBI BD Ø5 H
QBI BD Ø4 H
CAE AZT L
DATA ENA 74173 E24
OUT CONT
CLK CLR
R3(1) R2(1) R1(1) RØ(1)
D3 D2 D1 DØ
R83 1K
CTL VDAC Ø7 H
CTL VDAC Ø6 H
CTL VDAC Ø5 H
CTL VDAC Ø4 H
QBI WR VERNIER H
QBI INIT H
QBI BD Ø3 H
QBI BD Ø2 H
QBI BD Ø1 H
QBI BD ØØ H
DATA ENA 74173 E27
CTL VDAC Ø3 H
CTL VDAC Ø2 H
CTL VDAC Ø1 H
CTL VDAC ØØ H
+3VA
R78 1K
QBI READ DBR L
QBI LD BUF H
QBI ID CODE L
DATA ENA 74173 E31
QBI BD 15 H
QBI BD 14 H
QBI BD 13 H
QBI BD 12 H
DATA ENA 74173 E3Ø
QBI BD 11 H
QBI BD 1Ø H
QBI BD Ø9 H
QBI BD Ø8 H
74Ø4 E38
74Ø4 E45
QBI INIT H
DATA ENA 74173 E34
QBI BD Ø7 H
QBI BD Ø6 H
QBI BD Ø5 H
QBI BD Ø4 H
DATA ENA 74173 E33
QBI BD Ø3 H
QBI BD Ø2 H
QBI BD Ø1 H
QBI BD ØØ H

REVISIONS		
CHK	CHANGE NO	REV

(CTL)

TITLE	SIZE	CODE	NUMBER	REV.
A-D FOR 1103	D	CS	AØ12-Ø-1	H
SCALE —	SHEET 2 OF 6	DIST		

AØ12-Ø-1 H DCS

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CAE PRG GO L
CAE HOLD(1) L
CAE GO H
EXT ST L (SEE NOTE 2)
ST1 L
CLKOV L
QBI LD BUF H
QBI INIT L
READ QBI DBR L
CAE AD DONE(1) H
CAE AZT L
CAE HOLD(1)L
CAE ERROR C L
CAE TRANS INTRVL L
CAE ERROR B H
QBI EXT STARTS(1)H
QBI CLK STARTS(1)H
QBI MUX 5 (1)H
QBI MUX 4 (1)H
QBI MUX 3 (1)H
QBI MUX 2(1) H
QBI MUX 1 (1) H
QBI MUX Ø (1) H
CAE A3 H
CAE A2 H
CAE A1 H
CAE AØ H
QBI INIT L
QBI WR CSR LB L
QBI BD ØØ H
+3VB
CAE PRG GØ L
CRE HOLD(1)H
CAE HOLD(1)L
CAE HOLD(Ø)L
CAE DEL HOLD H
CAE ERROR A+C (1) H
CTL EOC L
QBIINIT L
CAE ERROR(1) L
CAE ERROR A+C(1)H
CAE ERROR B H
CAE SET ERROR L
QBI BD 15 H
QBI WR CSR HB H
CAE ERROR(1)H
CAE ERROR(1)L
CAE HOLD(1) L
CAE AZT L
QBI WR CSR HB H
CAE DEL HOLD H
CAE HOLD(1)H
CAE ZC DELAY H
J1
TP11
SE L
CAE A3 H
CAE A2 H
CAE AMUX BIT 2 H
CAE BMUX BIT 2 H
CAE EN BMUX H
CAE EN AMUX H
CAE ADZC L

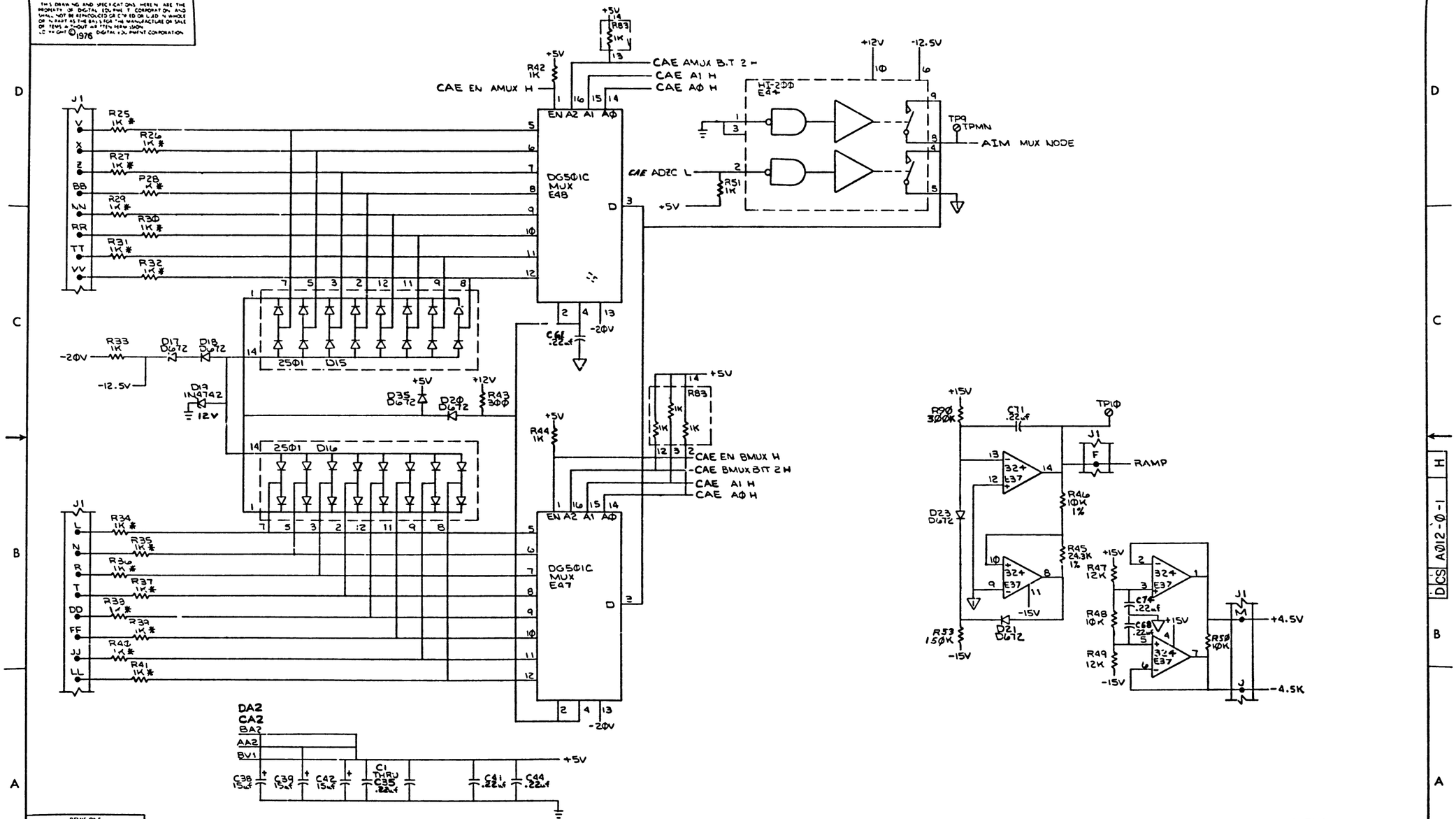
NOTES:
2. MUST BE PULSE LESS THAN 10usec

(CAE)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
A-D FOR 1103	D	CS	AØ12-Ø-1	A
SCALE	SHEET 3 OF 6	DIST.		

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
A-D FOR 1103	D	CS	AØ12-Ø-1	H.
SCALE —	SHEET 4 OF 6	DIST		

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AIM MUX NODE

TP5 TP AI

CAE HOLD(I)L

AD562 D/A E46

MSB

LSB

CTL SAR 11 L
CTL SAR 10 L
CTL SAR Φ9 L
CTL SAR Φ8 L
CTL SAR Φ7 L
CTL SAR Φ6 L
CTL SAR Φ5 L
CTL SAR Φ4 L
CTL SAR Φ3 L
CTL SAR Φ2 L
CTL SAR Φ1 L
CTL SAR ΦΦ L

TP7 TP AP

AD2700L E49

TP6 TP REF +10V

1mA I REF

MC1408-L8 E43

CTL VDAC ΦΦ H
CTL VDAC Φ1 H
CTL VDAC Φ2 H
CTL VDAC Φ3 H
CTL VDAC Φ4 H
CTL VDAC Φ5 H
CTL VDAC Φ6 H
CTL VDAC Φ7 H

Q1 2N3906
Q2 2N4250
Q3 2N4250
Q4 SE4Φ2Φ
Q5 SE4Φ2Φ
Q6 SE4Φ2Φ
Q7 SE4Φ2Φ
Q8 2N4250
Q9 2N4250
Q10 2N3906
Q11 2N3906
Q12 SE4Φ2Φ
Q13 2N5245

D2 D672
D3 D672
D4 D672
D6 D672
D7 D672
D36 D37 D37 D777
D37 D672
D38 3.3V IN746A
D14 1N754A 6.8V
D33 MCL1Φ4

R1 133 1%
R2 1K *
R3 200Ω 10 TURN GAIN
R4 10K
R5 12.1K
R6 30Ω.1
R7 909
R8 75Φ
R9 2.7K
R10 75
R11 75
R12 3K
R13 1K
R14 3K
R15 50K OFFSET ADJUST
R16 .25% 25PPM
R17 15K
R18 10Φ
R19 10Φ
R20 10K
R24 2.7K
R54 1K *

C62 .22µF
C63 .22µF
C64 .01µF
C65 820pf
C66 22pf
C67 .ΦΦ22µF
C69 22µF
C70 .22µF

+15V
-15V
+5V
4mA
CCW

ADC COMP H

J1

NOTES:
1. * DENOTES FUSIBLE RESISTOR

REVISIONS		
CHK	CHANGE NO	REV

(ADC)

TITLE	SIZE	CODE	NUMBER	REV.
A-D FOR 1103	D	CS	A012-Ø-1	H
SCALE —	SHEET 5 OF 6	DIST		

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NOTES:
1. CUT ETCH AT BC1 FOR Q22 BUS COMPATABILITY. ETCH CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER REQUEST ONLY.

R79 1K +5V

E35 8281 LD R A QA B QB C QC D QD CB CA

7410 E42 — APS SWA L

7404 E12

7410 E42 — APS SWB L

7410 E42

CTL CLOCK L

C43 .22uf C45 15uf +12V C73 39uf

CD2 BD2 AD2

APS SWA L — 7406 E41 — R56 1K — R55 150 — Q14 DEC 6S34D — L1 .22uh — C46 39uf — D24 DG72 — D25 DG72

Q15 D45C6 — R58 470 1/2W — R59 470 1/2W — TP4 ØTPPD

+5V R57 82 1/2W — Q16 D44C3 — L2 .22uh

APS SWB L — 7406 E41

LM325N E5μ — Q17 DEC 2219 — R60 5.1 — TP3 ØTP+ — W1 — +15V

C52 15uf — C53 15uf — W2 — -15V

C51 22uf — C48 39uf — C50 22uf — D26 DG72 — D27 DG72 — D34 DG72 — D29 DG72 — C47 39uf — C49 22uf

REF — Q18 DEC 2219 — TP- TP2 — R61 5.1 — -7.5V — -2ØV

L3 22uh — C72 6.8uf

SEE NOTE 1

BC1 AF1 AT1 AM1 AJ1 BT1 BM1 BJ1 BC2 AC2 CC2 CT1 DC2 DT1

TP1 ØHOG

SPARE LOGIC

W5 — CN2 — CN2

W4 — CR2 — CS2

AR2 — AS2

7408 E4

7401 E15

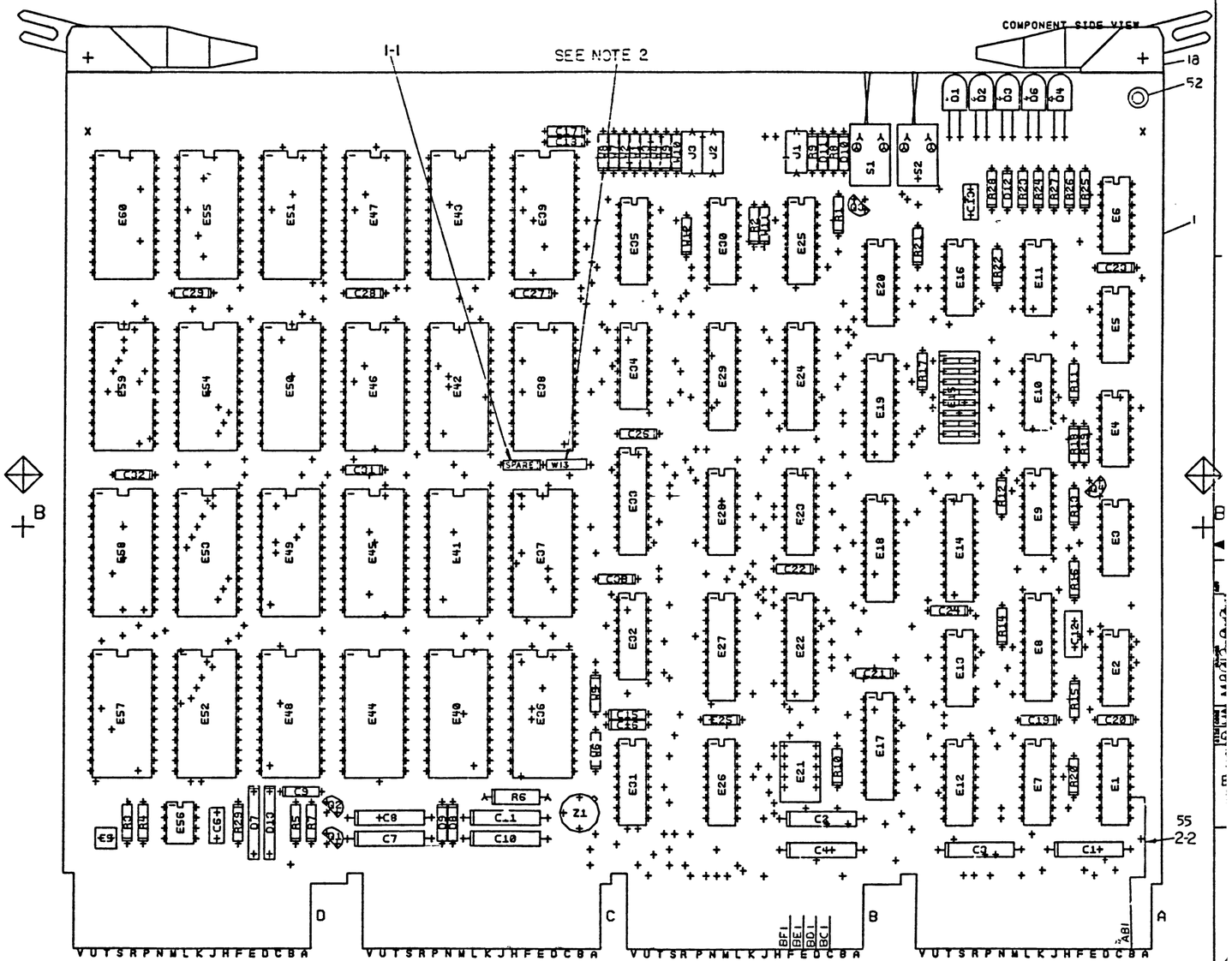
7400 E11

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
A-D FOR 1103 (APS)	D	CS	AØ12-Ø-1	H
SCALE —	SHEET 6 OF 6	DIST		

AØ12-Ø-1 REV H

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NOTES:
1. 8 HOLES .0465 (+.002-.0045) MAYNARD ONLY
2. W1,4,6,8,10,11 & 13 ARE OPTIONAL, DO NOT INSTALL
3. INSTALL SOCKETS FOR E36 E48 E40, E52, E53, & E57 ONLY

CHK	CHANGE NO	REV
	M8012-A5001	C
	M8012-A5003	D
	M8012-A5004	E
	M8012-A5005	F
	M8012-A5007	H
	M8012-A5008	J
	M8012-A5009	K

ETCH REV.
P.C. DESIGN DATA BASE REV.

SIGNATURES	DATE
DRN.	
CHK'D.	
ENG.	
PROJ.ENG.	
PROD.	

digital

TITLE: BOOT TERMINATOR AND DIAGNOSTIC ROM

SCALE 2/1 | SIZE D | CODE UA | NUMBER M8012-0-0 | REV K

SHT. 1 OF 2

NEXT HIGHER ASSY. 8-DD-M8012-0

MS#

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REWORK INSTRUCTIONS

ECO #1

COMPONENT DELETES SIDE 1.

1-1. DELETE C30, .047 uF (P/N 1012784)

COMPONENT ADDS SIDE 1:

ECO #2

~~2-1 CUT ETCH SIDE 2 BETWEEN E01 PIN 11 AND FINGER AB2~~

2-2 ADD WIRE SIDE 1 BETWEEN E01 PIN 11 AND FINGER AB1

~~ECO # 5~~

~~WIRE ADD3, SIDE 1~~

~~5-1 ADD WIRE FROM FINGER BC1 TO E1 PIN 15~~
~~5-2 ADD WIRE FROM FINGER BD1 TO E1 PIN 14~~
~~5-3 ADD WIRE FROM FINGER BE1 TO E1 PIN 13~~
~~5-4 ADD WIRE FROM FINGER BF1 TO E1 PIN 12~~

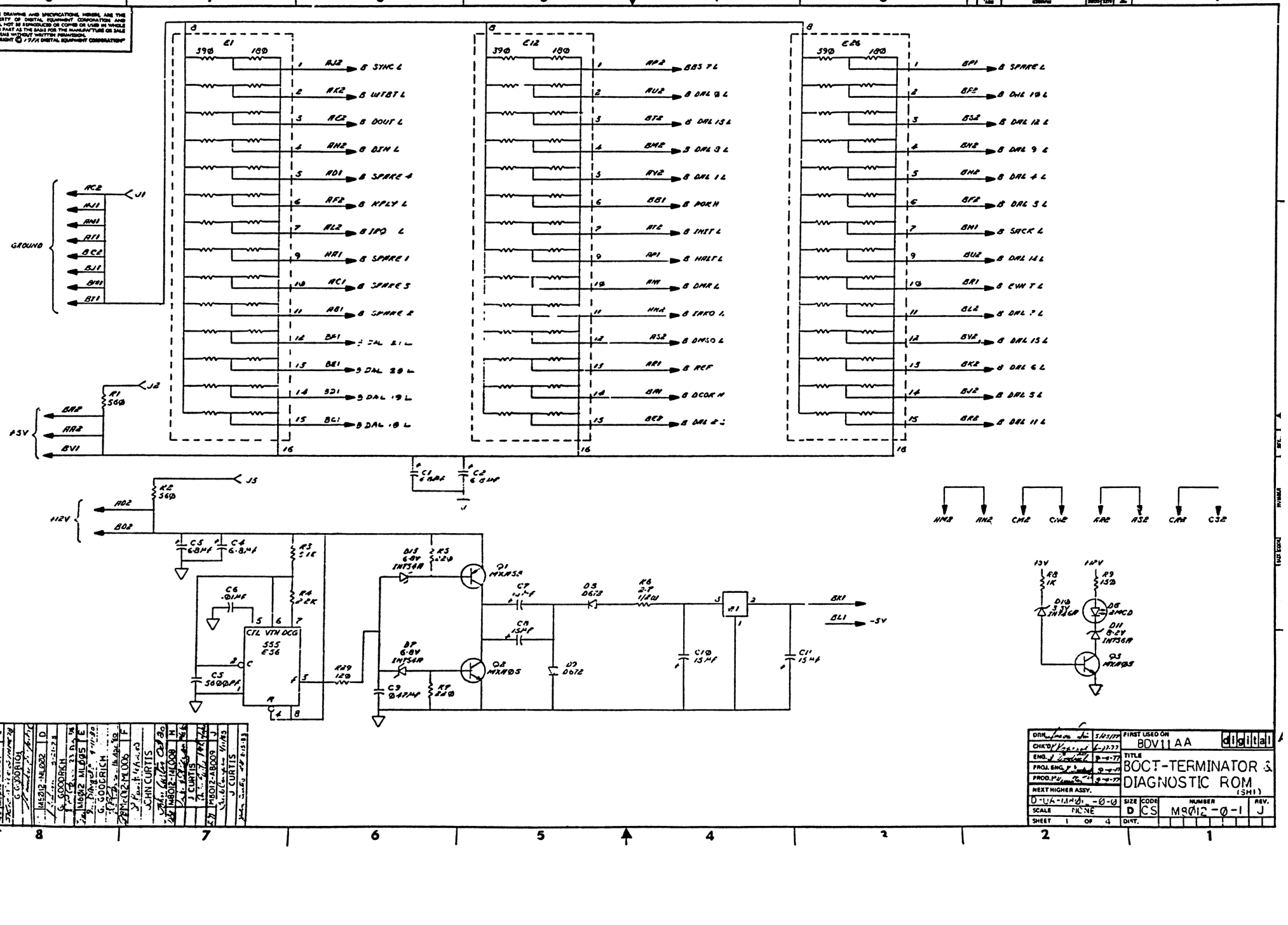
ECO # 9

9-1 REMOVE JUMPERS W3 AND W5.
9-2 INSTALL JUMPERS W4 AND W13.

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BOOT TERMINATOR AND DIAGNOSTIC ROM	D	DUA	M8012-0-0	K
SCALE 2/1 SHEET 2 OF 2	DIST			

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	CONSIST	REV.
USE	M8012-YM001	C
	M8012-YM002	D
	M8012-YM005	E
	M8012-YM006	F
	M8012-YM008	H
	M8012-YM009	J

DRR		5/05/77
CHK'D		6-12-77
ENG.		9-14-77
PROJ. ENG.		9-14-77
PROD.		9-14-77
NEXT HIGHER ASSY.		
D-UA-IAM0-0-0		
SCALE	NONE	
SHEET	1 OF 4	

FIRST USED ON: BDV11AA

TITLE: BOOT-TERMINATOR & DIAGNOSTIC ROM (SMI)

SIZE	CODE	NUMBER	REV.
D	CS	M9012-0-1	J

DIGT.

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SM2 REG L
SM2 SEL 4 L
SM2 INHIB L
74LS27 E3
74LS04 E5
7406 E16

BDAL 9 L(BAP)
BDAL 10 L(BA2)
BDAL 11 L(BA1)
BDAL 12 L(BA0)
BBS7 L(IAP1)
BUS 3
BUS 2
BUS 1
BUS 0
MEMB
JAI
JA2
JA3
JAV 3
JAV 2
JAV 1
XMIT
REC
DC005 E17
MATCH
DAT 3
DAT 2
DAT 1
DAT 0
SM2 DAL 9 H
SM2 DAL 10 H
SM2 DAL 11 H
SM2 DAL 12 H
+5V
R16 1K
R17 1K
SM2 INHIB L
SM2 XMIT H
E21
E15
E19
E18
E14
BDAL 6 L(BA2)
BDAL 7 L(BA1)
BDAL 8 L(BA2)
BDAL 15 L(BA2)
SM2 DAL 6 H
SM2 DAL 7 H
SM2 DAL 8 H
SM2 DAL 15 H
R13 1K
E41
BDAL 0 L(BA12)
BDAL 1 L(BA12)
BDAL 2 L(BA12)
BDAL 13 L(BA12)
SM2 DAL 0 H
SM2 DAL 1 H
SM2 DAL 2 H
SM2 DAL 13 H
BDAL 3 L(BA12)
BDAL 4 L(BA12)
BDAL 5 L(BA12)
BDAL 14 L(BA12)
SM2 DAL 3 H
SM2 DAL 4 H
SM2 DAL 5 H
SM2 DAL 14 H
R18 1K
R19 1K
R20 1K
R21 1K
R22 1K
R23 1K
R24 1K
C15 .01 MF
C12 470 PF
RUN
HALT
RESTART
S1
S2
D12 D672
DC004 E8
RXCX
XMTR
RCVR
ENB
DAL 2
DAL 1
DAL 0
WTBT
DOUT
DIN
SYNC
SEL 6
SEL 4
SEL 2
SEL 0
OUT H8
OUT L8
BRPLY
SM2 SEL 0 L
SM2 SEL 2 L
SM2 SEL 4 L
SM2 SEL 6 L
SM2 OUT L8 L
SM2 OUT H8 L
SM2 SYNC L
BWTBT L(BA2)
BDOUT L(BA2)
BDIN L(BA2)
74LS10 E11
74LS27 E2
74LS04 E13
74LS74 E16
SM2 RPI L
SM2 SYNC H
SM2 DC NOK L
SM2 REG H
SM2 REG L
SM2 XMIT H
SM2 XMIT L
SM2 DAL 12 H
8T23 E9
DO(1)
DI(1)
D2(1)
D3(1)
D4(1)
D5(1)
D6(1)
D7(1)
SM2 DAL 11 H
SM2 DAL 5 H
SM2 DAL 4 H
74LS32 E13
74LS08 E5
7406 E16
SM2 DC NOK H
SM2 DC NOK L
SM2 HALT L
SM2 REPLY L
SM2 SYNC L
0541 E7
(BAI) B DCOK H
(IAP1) B HALT L
(IAP2) B REPLY L
(IAI2) B SYNC L

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
BOOT-TERMINATOR & DIAGNOSTIC ROM (SM2)	D	CS	M8012-0-1	J
SCALE NONE	SHEET 2 OF 4	DIST.		

8 7 6 5 4 3 2 1

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74LS273 E27 — SH2 DAL 15 H … SH2 DAL 8 H; SH3 R15 N … SH3 R8 N
74LS257 E32 — SH3 R11 N, SH3 R10 N, SH3 R9 N, SH3 R8 N; SH3 A10 N, SH3 A9 N, SH3 A8 N, SH3 A7 N
74LS257 E34 — SH3 R7 N … SH3 R4 N; SH3 A14 N, SH3 A13 N, SH3 A12 N, SH3 A11 N
74LS273 E29 — SH2 DAL 0 H … SH2 DAL 7 H; SH3 R0 N … SH3 R7 N
74LS273 E35 — SH2 DAL 8 H … SH2 DAL 15 H; SH3 R8 N … SH3 R15 N
74LS74 E5 — SH3 A14 N → SH3 A14 L
74LS139 E33 — SH2 PRI L; W3, W4; W1, W2; SH3 A10 H, SH3 A9 H, SH3 A13 H; SH3 SP3 L … SH3 SP0 L
74LS257 E28 — SH3 R7 N … SH3 R4 N; SH4 07 H … SH4 04 H; SH2 DAL 7 H … SH2 DAL 4 H
74LS257 E30 — SH3 R15 H … SH3 R12 H; SH4 015 H … SH4 012 H; SH2 DAL 15 H … SH2 DAL 12 H
74LS257 E23 — SH3 R3 N … SH3 R0 N; SH4 03 H … SH4 00 H; SH2 DAL 3 H … SH2 DAL 0 H
74LS257 E31 — SH3 R11 N … SH3 R8 N; SH4 011 H … SH4 008 H; SH2 DAL 11 H … SH2 DAL 8 H
74LS139 E36 — W11; SH3 A12 H, SH3 A11 H; SH3 SE1 L, SH3 SE2 L, SH3 SB1 L, SH3 SB2 L
74LS74 E5 — W9, W10; SH3 A14 H, SH3 A14 L
74LS27 E3 — SH2 REG L, SH2 SEL 0 L, SH2 OUT HB L → SH2 DC NOK L
74LS27 E2 — SH2 REG L, SH2 SEL 6 L, SH2 OUT LB L → SH2 DC NOK L
74LS27 E4 — SH2 REG L, SH2 OUT LB L, SH2 SEL 4 L → SH2 DC NOK L
74LS27 E4 — SH2 REG L, SH2 SEL 2 L, SH2 OUT HB L → W10
74LS10 E5 — SH2 SEL 2 L; SH2 REG H, SH2 XMIT H → W9
74LS10 E11 — SH2 REG H, SH2 XMIT H, SH3 OUT 2 L → W12
74LS299 E22 — SH2 DAL 15 H … SH2 DAL 11 H; SH2 DAL 13 H, SH2 DAL 10 H, SH2 DAL 12 H
74LS399 E24 — SH2 DAL 7 H … SH2 DAL 4 H; SH2 DAL 6 H, SH2 DAL 0 H, SH2 DAL 1 H, SH2 DAL 5 H
74LS175 E25 — SH2 DAL 5 H … SH2 DAL 2 H; SH2 DAL 0 H … SH2 DAL 3 H
74S74 E10 — SH2 DAL 6 H; SH2 REG L, SH2 OUT LB L, SH2 SEL 6 L; SH2 DC NOK L
74S86 E6 — SH2 DAL 5 H … SH2 DAL 2 H; SH2 DAL 0 H … SH2 DAL 3 H
SH2 SYNC H → SH2 DC NOK L
B EVNT L BRI → E21 → Q4 MPSA05; +5V, R18 1K, R19 1K
+12V: C17, C18 .047UF
+5V: W13, W15, W16; C12, C22; C14 THRU C16 .047MF
R23 … R28 220Ω; D4 … D1 2N5209; +5V
SH3 A10 H → W7 → SH3 SI2; SH3 SI1

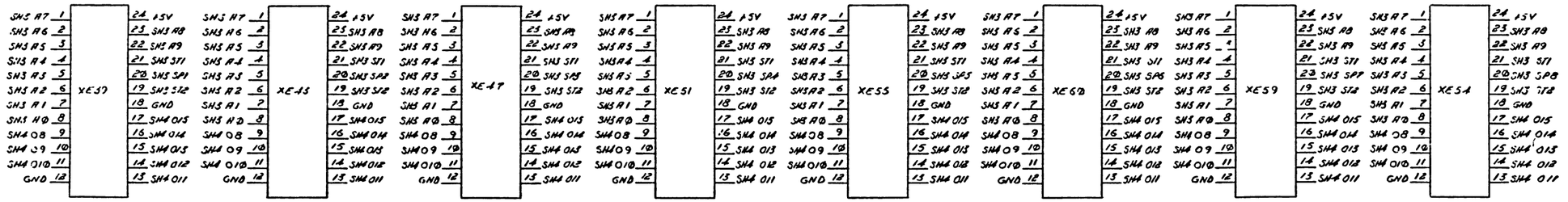
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
BOOT-TERMINATOR & DIAGNOSTIC ROM (SH3)	D	CS	M8012-0-1	J
SCALE NONE	SHEET 3 OF 4		DIST.	

DEC FORM NO. DRD 138

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NOTES: ALL SIGNALS ON THIS SHEET, EXCEPT THOSE CONNECTED TO PIN 20 OF ALL SOCKETS ON THIS SHEET ARE HIGH INPUTS AND OUTPUTS. THE SIGNALS CONNECTED TO PIN 20 OF ALL SOCKETS ON THIS SHEET ARE LOW

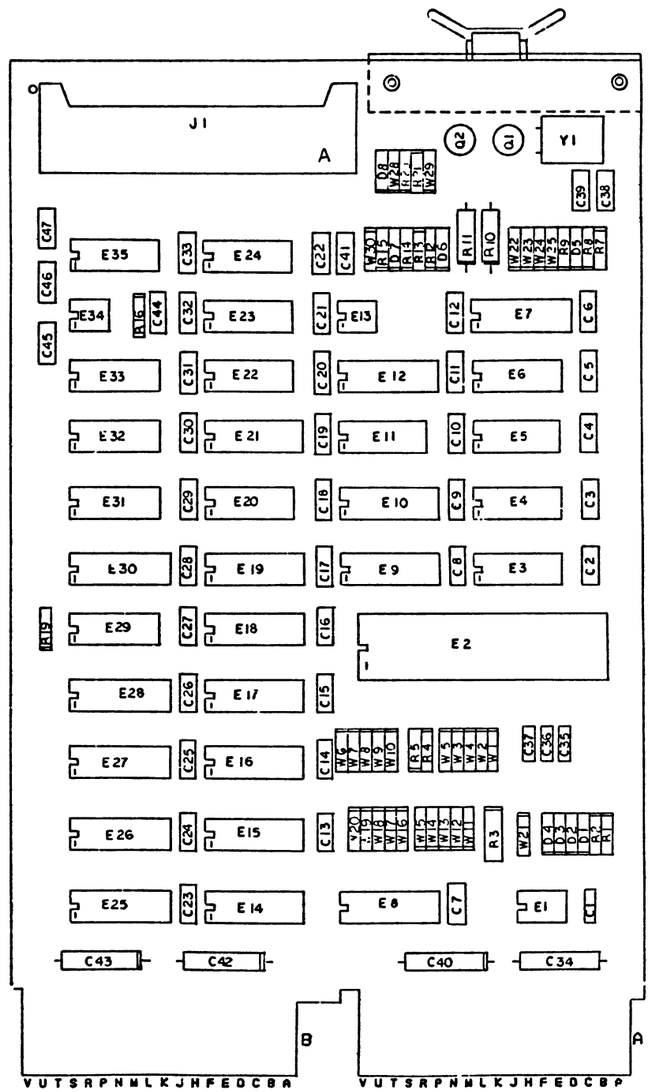


REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BOOT-TERMINATOR & DIAGNOSTIC ROM (SH4)	D	CS	M8012-0-1	J
SCALE NONE	SHEET 4 OF 4	DIST.		

DEC FORM NO. DRD 138

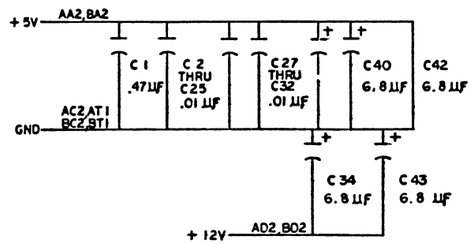
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I.C. DEC MH8026C	3			6
I.C. DEC HSUART	3	1	2	
I.C. DEC 1488			1	14
I.C. DEC 7493	10	5		
I.C. DEC 74175	8	16		
I.C. DEC 74157	8	16		
I.C. DEC 74155	8	16		
I.C. DEC 8837	8	16		
I.C. DEC 8641	8	16		
I.C. DEC 8136	8	16		
IC TYPE	GND	+5V	-12V	+12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



NOTES:

STEP E	+ Y AXIS ___ STEP 0 TIMES
REPEAT	+ X AXIS 5.250 STEP 1 TIMES

CHG	CHANGE NO	REV
CSA	M7940-A8007	A
	ORIGINATED	
CSB	M7940-A8008	K
	J. CURTIS	
	M7940-A8009	L
	J CURTIS	
	M7940-A8010	M
	JW. CURTIS	
CSC	M7940-M1011	N
	D-EBRT 28-NOV-75	
	T.RILEY	

SIGNATURES	DATE
DRN. VINCENT	4-28-75
CHK'D. FERGISON	5-8-75
MECH. ENG. CYR	6-12-75
PROJ. ENG. CYR	6-12-75
PROD. DEHAZE	6-12-75
SCALE 2/1	
SHT. 1 OF 5	
NEXT HIGHER ASSY. D-UA-M7940-0-0	

digital

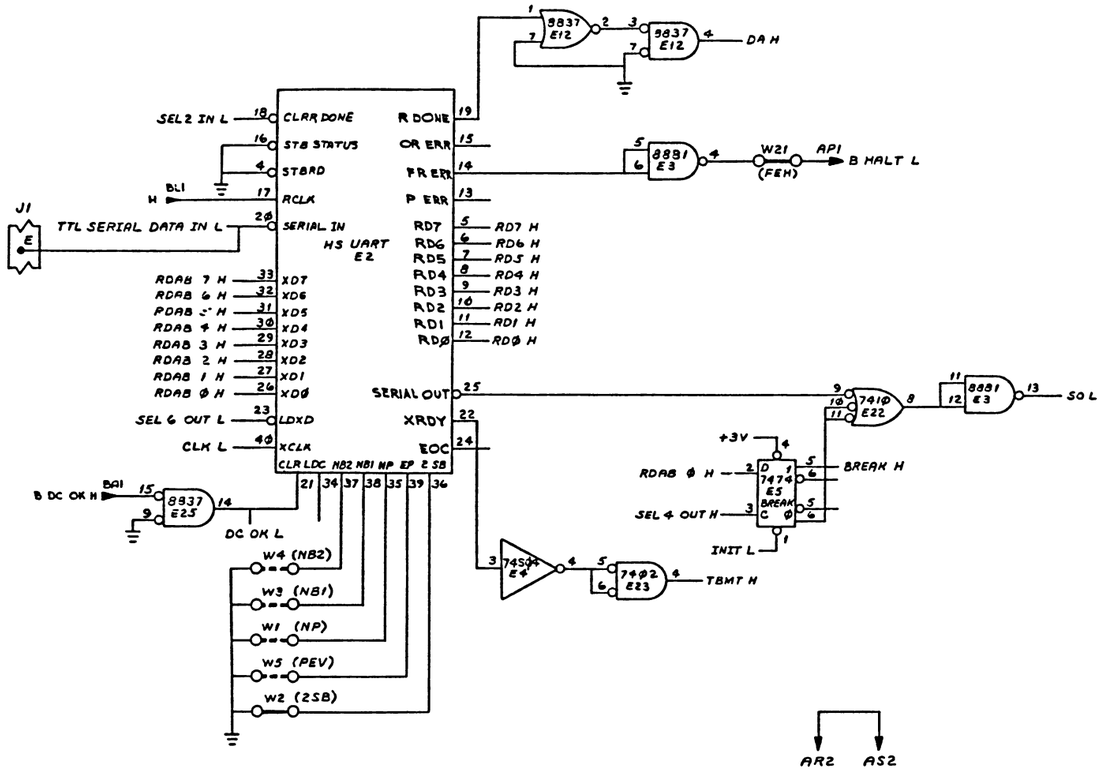
TITLE SERIAL LINE UNIT

SIZE	CODE	NUMBER	REV
D	CS	M7940-0-1	N

M7940-0-1 N CS D

8 7 6 5 4 3 2 1 MS#

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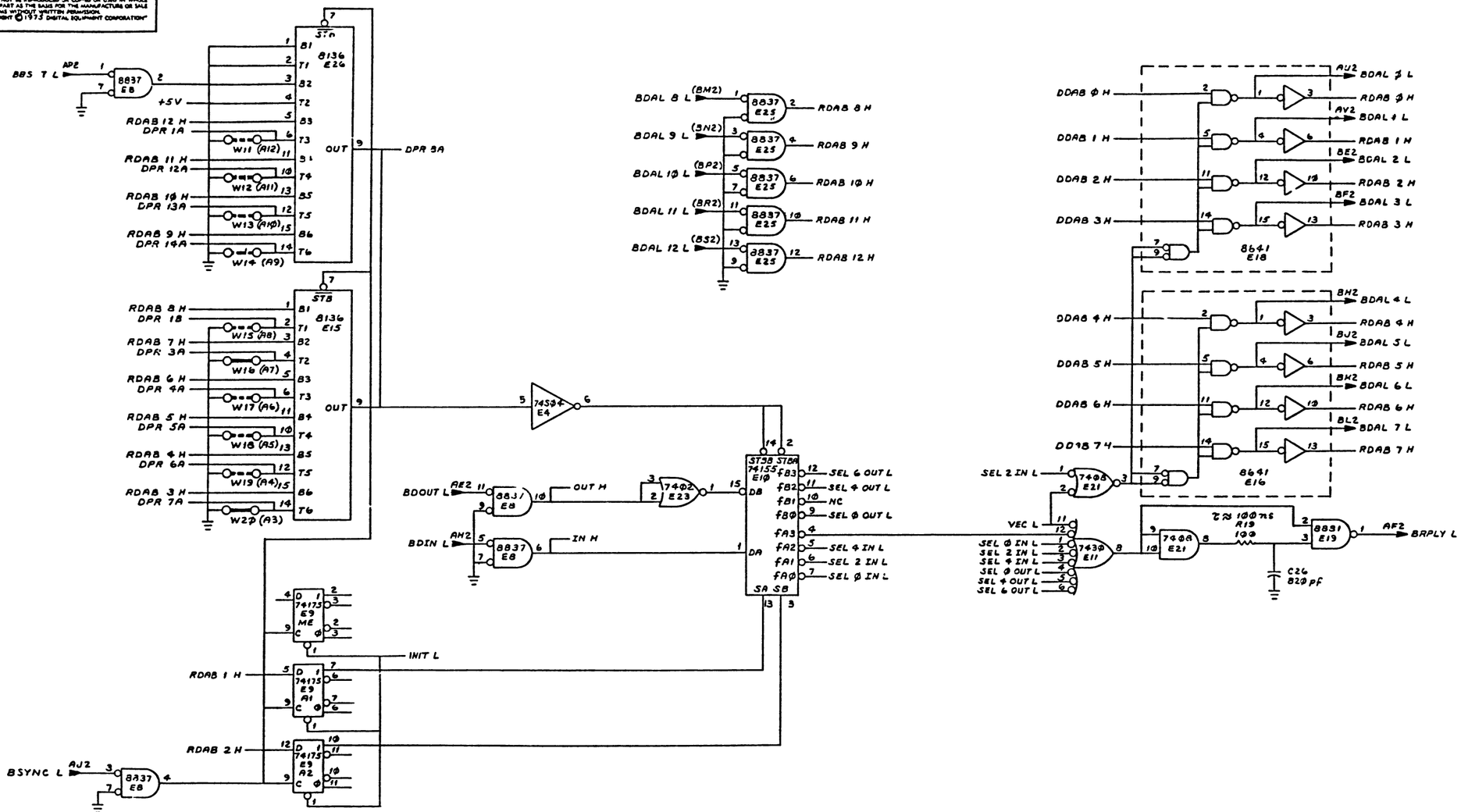
(UART & MULTIPLEXOR LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
SERIAL LINE UNIT	D	CS	M7940-0-1	N
SCALE	SHEET 2 OF 5	DIST.		

DEC FORM NO. BMD 1.10

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(BUS ADDRESS & I/O LOGIC)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SERIAL LINE UNIT	D	CS	M7940-Ø-1	N
SCALE —	SHEET 3 OF 5	DIST		

DEC FORM NO. D102 1/26

M7940-Ø-1 N

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TTL SERIAL DATA IN L — 74S04 E4 — 8881 E3 — DPR 10B — 7493 E6 START DETECT R3(1) R2(1) R1(1) R0(1) CLR CLK0 CLK8C — CLK L

INIT H — 7402 E23

RDAB Ø H — 7474 E5 READER RUN — SEL Ø OUT H

+3V — R8 330 — R7 220 — +5V — R13 68 — Q1 6534D — D5 D664 — R5 47 — R4 47 — AL1

E24 — W3Ø — AL1

DPR 1A … DPR 16A — +5V — E14 — 330 680

DPR 1B … DPR 16B — +5V — E28 — 330 680

(+3V) DPR 11A

R2 470 — MH 0026C E1 — C37 .47µf — D2 D664 — D3 D664 — D1 D664 — C36 .47µf — R3 120 — D4 IN759A — AK1 — -12V @ 40 ma MAX

R1 470 — 74S04 E4 — MH 0026C E1 — C35 .47µf

9 — 74S04 E4 — 8

C38 33pf — DC OK L

Y1 2.4576MHz — R9 10M — C39 33pf — CO 3470Z E7 BAUD RATE GEN. — CP IX OX IM — S0 S1 S2 S3 — 8837 E12 — BK1 — CLK L

EXT UART CLK IN H — BH1

W22 (FR0) — W23 (FR1) — W24 (FR2) — W25 (FR3)

EIA DATA IN L — 1489 E35 — EIA/TTL RCVD DATA H — C45 330pf

SO L — 1438 E24 — EIA TRANS. DATA H — C42 330pf

CLEAR TO SEND H — 1489 E35 — 7402 E23 — MODEM ST. H — C46 330pf

CARRIER

DATA SET RDY H — 1489 E35 — C47 330pf

J1 — M F V DD C H S K KK A B SS TT UU VV

1488 E24 — RQST TO SEND H

DATA TERM RDY H

+3V — 1488 E29 — BUSY H

8837 E12 — 20MA/TTL RCVD DATA L

+5V — R16 2K

TP1 — C44 .005µf — TP2 — INSERT FOR TTY USE ONLY

4N26-00 E34 — OCI — R14 220 — D7 IN4004 — R21 100. (CL2)

+5V — R15 150 — R11 270 — +12V — W28 (CL1)

4N26-00 E13 — OCI — SO L — R12 68K — Q2 MX455 — D6 IN4004 — D8 MCL1301 — R20 100 (CL3) — R10 270 — +12V — W29 (CL4)

SEE NOTE 3,9

* SEE NOTE 2

(PERIPHERAL & BAUD RATE LOGIC)

REVISIONS

CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SERIAL LINE UNIT	D	CS	M7940-J-1	N
SCALE —	SHEET 4 OF 5	DIST.		

DEC FORM NO. BMD 5.10

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INIT L
+3V
7474 E31 RDINT RQST
7408 E32
8881 E19
AL2
BIRQ L
INIT L
+3V
7474 E31 TDINT RQST
7408 E32
+3V
7474 E20 E21 IACK AD
7410 E22
7408 E21
VEC L
DPR 9A
BIAK I L
AM2
8837 E8
INH
INIT L
+3V
7474 E20 E21 IACK TD
INH
INIT L
+3V
7410 E22
8881 E19
AM2
DPR 10A
BIAK O L
VEC 2 H
BINIT L
AT2
8837 E8
74S04 E4
INIT L
INIT H
DA H
RD INT EN H
7408 E32
RDAB 6 H
SEL 0 OUT H
SEL 0 OUT L
8837 E12
7474 E33 RD EN
INIT L
TBMT H
7408 E32
+3V
RDAB 6 H
SEL 4 OUT H
SEL 4 OUT L
8837 E12
7474 E33 TD EN
TDINT EN H
DPR 11A +3V

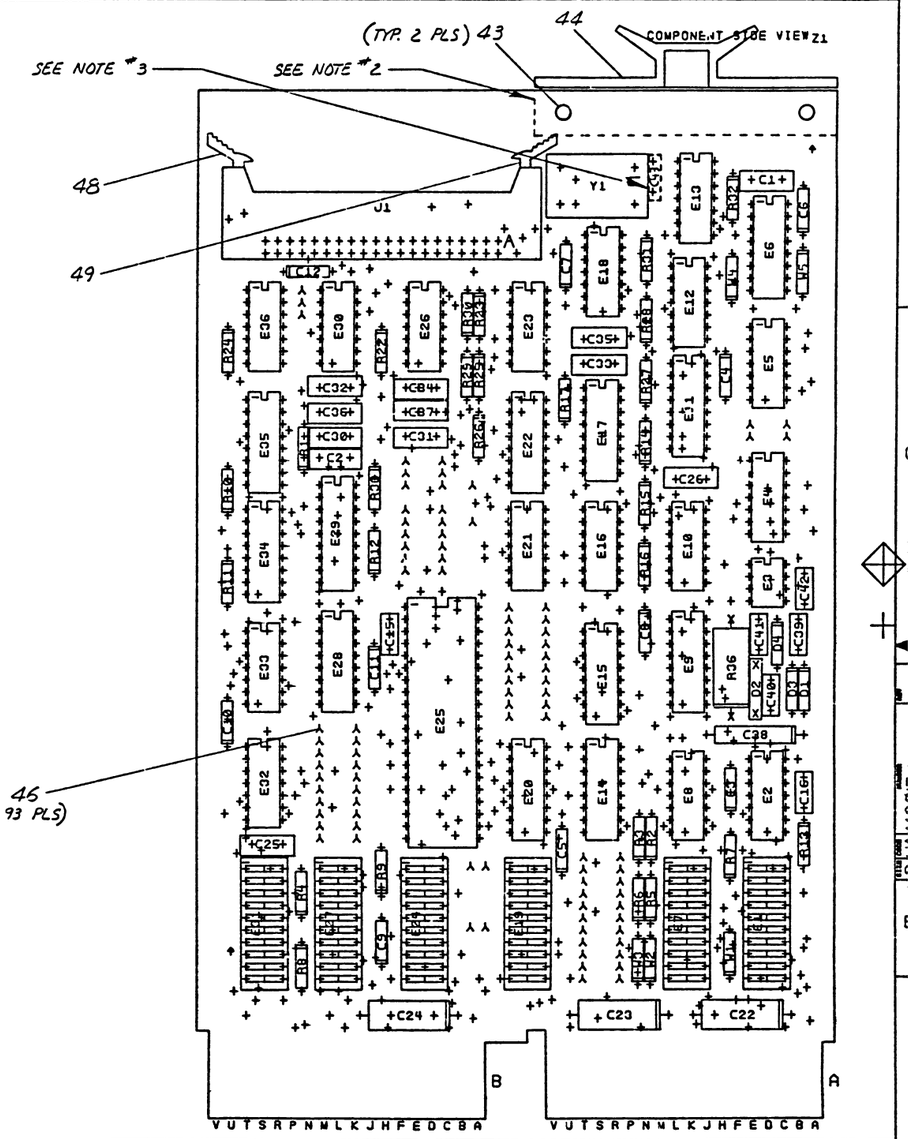
(INTERRUPT & ENABLE LOGIC)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SERIAL LINE UNIT	D	CS	M7940-0-1	N
SCALE	SHEET 5 OF 5	DIST.		

DEC FORM NO. DRD 128

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NOTES: 1. .012 ETCH .013 SPACING.
2. ITEM NO. 45 UNDERNEATH HANDLE
3. OPTIONAL ITEM, USE PART NO. 10-10279-00.

STEP X	+ Y AXIS .9 STEP .9 TIMES
REPEAT	+ X AXIS 5.25C STEP .2 TIMES

CHK	CHANGE NO	REV
	M8017-AB004	F
	REVISED & REDRAWN	
	J. CURTIS	
	M8017-AB005	H
	J CURTIS	
	6TO:	
	M8017A-YB008	J
	J. CURTIS	

ETCH REV. D-P4

SIGNATURES		DATE
DRN.	FRANK SMART	6-22-77
CHK D.	FRANK SMART	6-22-77
MECH. ENG.	M. D. MICHAUD	7-1-77
PROJ. ENG.	M. D. MICHAUD	7-1-77
PROD.	M. D. MICHAUD	7-1-77

digital

TITLE: A.L.I.

SCALE 2/1 | SHT. 1 OF 1 | SIZE D | CODE UA | NUMBER M8017-AA | REV J

NEXT HIGHER ASSY. 8-00-M8017-AA

MS# 15039

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MISCELLANEOUS JUMPERS		
JUMPERS IN	JUMPERS OUT	FEATURE
1, 2		5 DATA BITS
1	2	6 DATA BITS
2	1	7 DATA BITS
	1, 2	8 DATA BITS *
P		PARITY CHECK
	P	NO PARITY CHECK *
-E		ODD PARITY
	-E	EVEN PARITY *
PB		PDP11 BAUD RATES ENABLED
	PB	PDP11 BAUD RATES DISABLED *
BG		BREAK GENERATION ENABLED *
	BG	BREAK GENERATION DISABLED
C, C1	S, S1	COMMON SPEED *
S, S1	C, C1	SPLIT SPEED
H		HALT ON FRAMING ERROR
	H	NO HALT ON FRAMING ERROR *
B	-B	BOOT ON FRAMING ERROR *
-B	B	NO BOOT ON FRAMING ERROR *
-FR		NO FORCE OF REQ TO SEND *
	-FR	FORCE REQ TO SEND ON
-FD		NO FORCE OF DTR *
	-FD	FORCE DTR NO
RS		REQUEST TO SEND ENABLED *
	RS	REQUEST TO SEND DISABLED
FB		FORCE BUSY ENABLED *
	FB	FORCE BUSY DISABLED *
	M1	FACTORY USE ONLY *
INIT	DCOK	UART CLEAR SIG.

BAUD RATE SELECT JUMPERS					
RECEIVER	R3	R2	R1	R0	BAUD RATE
TRANSMITTER	T3	T2	T1	T0	
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110 * RECEIVER
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600 * TRANSMITTER
	R	R	R	R	19200

I = INSTALLED R = REMOVED

INSTALL WIRE P/N 91-05740 (SEE ITEM 47 OF KPL)

SEE NOTE #2

DEVICE ADDRESS JUMPERS			
JUMPERS IN	JUMPERS OUT	ADDRESS	
A9, A5, A6, A8 A9, A8, N1, N2	A9, A7	CONSOLE 177560	
A9, A7, A8, A9 A11, N2	A4, A5 A6, P/F	DLV11-E UNIT #1 175610	*

ADDRESS SETUP DIAGRAM — SEE NOTE #3

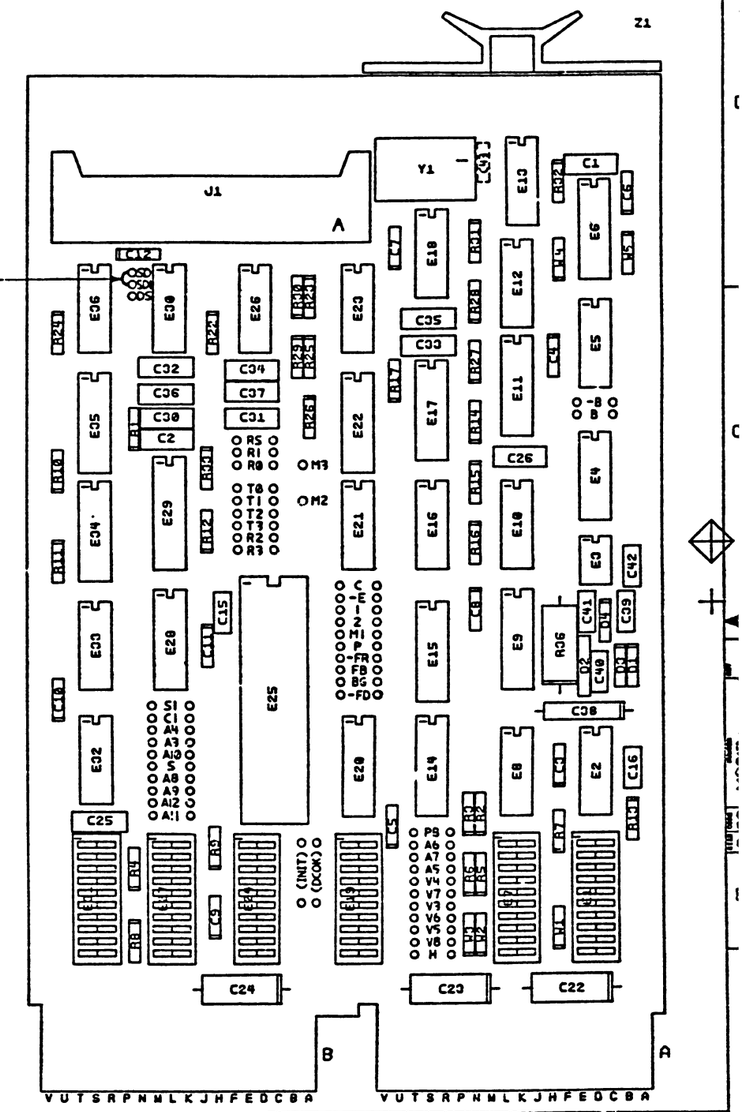
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SEE NOTE #2

VECTOR ADDRESS JUMPERS			
JUMPERS IN	JUMPERS OUT	ADDRESS	
V4, V5	V3, V6, V7 V8	CONSOLE 60, 64	
V6, V7	V3, V4, V5 V8	DLV11-E UNIT #1 300, 304	*

VECTOR SETUP DIAGRAM — SEE NOTE #3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



4, W1, W2, W3, W5 NOT INSTALLED.

NOTES: 1. * MODULE SHIPPED FROM FACTORY IN THIS CONFIGURATION.
2. CONFIGURATIONS SHOWN FOR DEVICE VECTOR ADDRESSES ARE ONLY A FEW EXAMPLES. FOR A COMPLETE LIST, SEE DLV11-E/DLV11-F USERS MANUAL. 3. ADDRESS SETUP DIAGRAMS PROVIDED FOR USERS CONVENIENCE.

STEP E	+ Y AXIS	STEP TIMES
REPEAT	+ X AXIS	STEP TIMES

CHK	CHANGE NO	REV
	M80/ABUJA	F
	REVISED - REDRAWN	
	J. CURTIS	
	J. CURTIS	
	INSTALL W1 & W2	H
	J. CURTIS	
	M.O'Connor	J
	M.O'Connor	
	J.CURTIS	

SIGNATURES		DATE
DRN.	B. B. BLODGETT	6-7-77
CHK'D.	F. SMART	7-1-77
MECH. ENG.	M. D. MICHAUD	7-1-77
PROJ. ENG.	M. D. MICHAUD	7-1-77
PROD.	M. D. MICHAUD	7-1-77
SCALE	2/1	
SHT.	1 OF 6	

digital

TITLE ASYN LINE INTERFACE

SIZE	CODE	NUMBER	REV
D	CS	M8017-AA-1	J

NEXT HIGHER ASSY. B-00-M8017-AA

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[K-3] SEL 4 IN L
[K-3] INWD L
74LS00 E32
74LS04 E12
74LS04 E12
BIRQ 5L AA1
BIRQ 7L BP1
BIRQ 6L AB1
[K-5] R DONE (I) H
[K-7] R INT EN (I) H
[K-7] DSET INT (I) H
[K-7] DSET INT EN (I) H
74LS20 E32
74LS32 E32
74LS00 E32
+3V
[K-7] SEL 0 OUT LB H
BINIT L
[K-5] XRQY H
74LS04 E12
74LS04 E26
[K-4] SEL 4 OUT LB H
[K-3] DAT 6 H
BIAKI L
AM2
BDIN L
BAI
BDC OK H
[K-5] DC OK L
API
B MALT L
[K-5] FE H
8641 E11
+5V
R1 1K
[K-5] +3V
AA2 BA2
C3 THRU C12 .047mfd
C23 8mfd
C24 8mfd
C16 .47mfd
C39 THRU C43 .47mfd
C22 8mfd
GND
+12V AD7
AC2 AT1 BC2 BT1
DC003 E7
RQSTA H
ENA DATA H
INIT L
ENA CLK H
INTERRUPT
BIAKO L
RQSTB H
ENB DATA H
ENB CLK H
VECTOR H
BDIN L
VEC RQSTB H
BIAKI L
BIAKO L
AL2
B1RQ L + [B1RQ 4L]
[K-5] T INT EN (I) H
VECTOR H
VEC RQST B H
AM2
[K-3] DAT 15 H
[K-3] DAT 12 H
[K-3] DAT 11 H
[K-3] DAT 14 H
+5V
[K-3] DAT 10 H
[K-3] INIT H
[K-3] INIT L
[K-3] DAT 13 H
R8 2.4K
R9 2.4K
XMIT H
REC H
DAT3
DAT2
DAT1
DAT0
BUS3
BUS2
BUS1
BUS0
JA3
JA2
JA1
JV3
JV2
JV1
MENB L
MATCH H
DC005 E27 SST
(AH2)
(AH1)
(AH)
(A9)
(A8)
(V8)
BV2 BDAL 15 L
BS2 BDAL 12 L
BR2 BDAL 11 L
BU2 BDAL 14 L
BP2 BDAL 10 L
BM2 BDAL 9 L
BT2 BDAL 8 L
BDAL 13 L
[K-3] DAT 7 H
[K-3] DAT 6 H
[K-3] DAT 5 H
[K-3] DAT 0 H
R5 33Ø +5V
R6 68Ø
+5V
R7 330Ω
R2 33Ø +5V
R3 68Ø
BL2 BDAL 7 L
BK2 BDAL 6 L
BJ2 BDAL 5 L
AU2 BDAL 0 L
(A7)
(A6)
(A5)
(V7)
(V6)
(V5)
DC005 E19 SST
[K-3] DAT 4 H
[K-3] DAT 3 H
[K-3] DAT 2 H
[K-3] DAT 1 H
(A4)
(A3)
(V4)
V3
DC005 E29 SST
BM2 BDAL 4 L
BF2 BDAL 3 L
BG2 BDAL 2 L
AV2 BDAL 1 L
+5V
AP2
BBS7 L
DC004 E1 PROTOCOL
ENB H
BWTBT L
BSYNC L
BDOUT L
BDIN L
BDAL 2
BDAL 1
BDAL 0
VECTOR
RICK
INWD L
OUT LB L
OUT UB L
REPLY L
SEL 6 L
SEL 4 L
SEL 2 L
SEL 0 L
AK2
AJ2
AE2
AF2
BRPLY L
[K-3] OUT HB L
[K-3] OUT LB L
[K-3] SEL 0 L
[K-3] SEL 2 L
[K-3] SEL 4 L
[K-3] SEL 6 L
R4 1K +5V
C25 470pf
[K-3] DAT 2 H
[K-3] DAT 1 H
[K-3] DAT 3 H

* DC003 BRACKETED #'S REFER TO DC003 PRIME CHIP.
PIN No. 20 — +5V
PIN No. 9 — GND.

5012499 D
(BUS RECEIVERS & DRIVERS) [K-3]

DRN.	--	FIRST USED ON	digital
CHK'D	7-1-77		
ENG.	7-1-77	TITLE	ASYN. LINE INTERFACE
PROJ. ENG.	7-1-77		
PROD			
NEXT HIGHER ASSY.			
SCALE	--	SIZE D	CODE CS
SHEET 2 OF 6		DIST	NUMBER M5017-AA-1
			REV J

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[K-5] DAT 12 H
[K-5] DAT 13 H
[K-5] DAT 14 H
[K-5] DAT 15 H
74LS298 E34
R9 10K
R10 10K
R11 10K
R12 10K
R13 10K
[K-5] DC OK L
C26 470 PF
R14 1K
R15 2.5K
[K-5] DAT 11 H
[K-5] SEL 4 L
[K-5] OUT 8 L
[K-5] DIN L
[K-5] +5V
[K-5] DAT 0 H
[K-5] OUT LB L
[K-5] SEL 4 L
[K-5] DAT 2 H
[K-5] INIT L
74LS74 E16
74LS74 E18
74LS74 E19
[K-4] BREAK (1) H
[K-5] SERIAL OUT H
[K-4] 30 MARK H
[K-4] MAINT (1) H
[K-4] MAINT (1) L
[K-4] SEL 4 OUT LB H
[K-4] 11Β BAUD H
[K-4] SEL 4 IN L
R16 10K
R17 10K
R18 10K
OSC 5.0688 MHZ Y1
5816 E29
(SEE NOTE 1)
INT R CLK H
INT T CLK H
(S1)
74LS04 E21
74LS00 E22
74LS02 E23
74LS32 E24
74LS86 E25
74LS08 E17
74LS00 E16
74LS02 E15
74LS32 E14
74LS86 E13
74LS04 E12
74LS393 E3
74LS153 E22
J2 CC
COMM CLK INPUT H
EXT R CLK H
EXT T CLK H
COMM CLK EN L
[K-4] SI MARK H
[K-4] S0 MARK H
[K-4] MAINT (1) H
[K-4] R CLK H
[K-4] T CLK H
[K-4] SERIAL IN H
J1 U S H H
R17 10K
74LS394
N/C
W5
W4
(SEE NOTE 3)
C38 6.8 μF
C39 .47 μF
C42 .47 μF
C41 .47 μF
C40 .47 μF
D1 D664
D4 D664
D3 D664
D2 BZX70A 5% 1W
R36 82 1W
AK1 -12V 70 MA MAX.
AL1 [K-4] -12V RET (SEE NOTE 2)

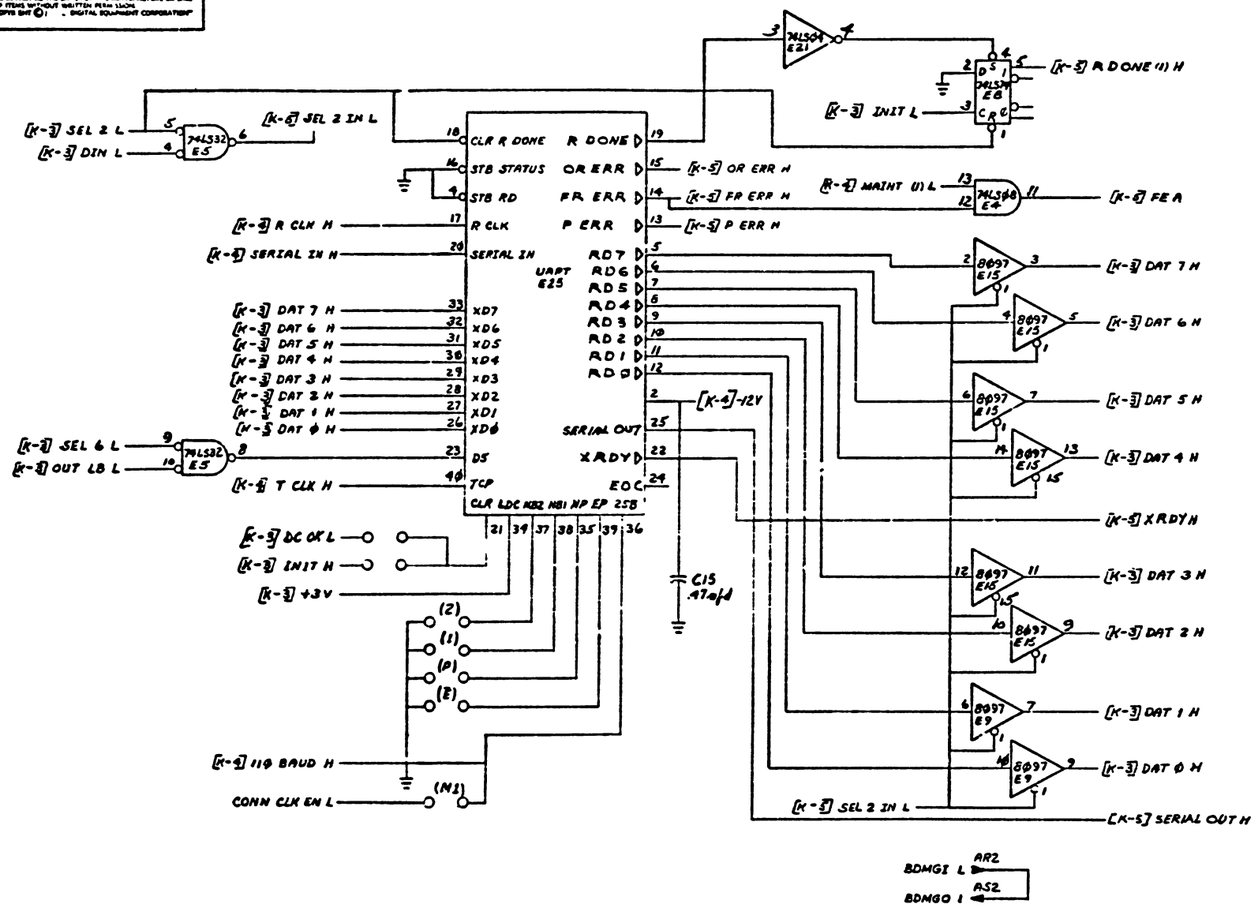
NOTES:
1. AK1 AND AL1 ARE TIED TOGETHER ON THE BUS
2. AK1 AND AL1 ARE TIED TOGETHER ON THE BUS.
3. W4 NORMALLY INSTALLED

(TCSR, BAUD RATE CKT AND -12V SUPPLY) [K-4]

REVISIONS		
ECR	CHANGE NO	REV

TITLE: ASYN LINE INTERFACE
SIZE D | CODE CS | NUMBER M8017-AA-1 | REV J
SCALE | SHEET 3 OF 6 | D ST

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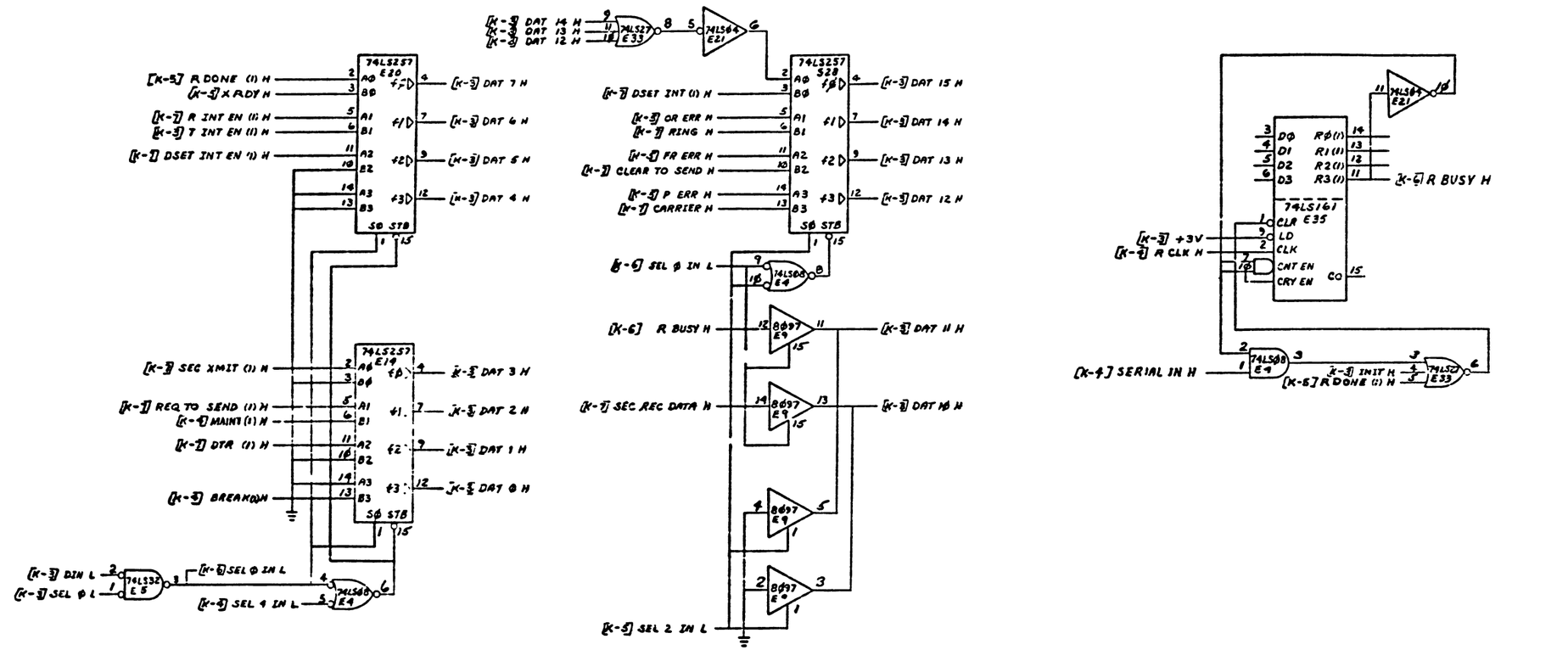


(UART CKT) [K-5]

REVISIONS			
CHK	CHANGE NO	REV	

TITLE	SIZE	CODE	NUMBER	REV.
ASYN LINE INTERFACE	D	CS	M8017-AA-1	J
SCALE	SHEET 4 OF 6	DIST		

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(INTERNAT BUS DRIVERS & RCVR BUSY CKT) [K-6]

REVISIONS		
ENG	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN LINE INTERFACE	D	CS	M8017-AA 1	J
SCALE	SHEET 5 OF 6	DIST		

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NOTE:
1. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC8JV OR EC8SC CABLE. THESE CABLES ALSO CONNECTS J1 PINS M TO E.

22 EIA RING H — J1 X — 1489 E30 — 74S64 E26 — [K-7] RING H
6 EIA CARRIER H — 1489 E30 — 74S64 E26 — [K-7] CARRIER H
5 EIA CLEAR TO SEND H — 1489 E30 — 74S64 E26 — [K-7] CLEAR TO SEND H
12 EIA SEC REC DATA H — 1489 E30 — 74S64 E26 — [K-7] SEC REC DATA H
6 EIA DATA SET RDY
3 EIA RECEIVE DATA H — 1489 E13 — 74S64 E26 — J1 M — EIA INTLCK H
+5V — TT, A, B, UU, VV
TTL SI MARK L — 74LS04 E21 — [K-7] SI MARK H

C30 470 PF; C2 330 pF; C31 220 PF; R22 470Ω; R23 220; R24 1K; 74LS240 E23
C32 470PF; R25 1K; C33 220PF; R26 2K; 74LS240 E23
C34 470 PF; R27 1K; C35 220PF; R28 2K; 74LS240 E23
C36 470 PF; R29 1K; C37 220 PF; R30 2K; 74LS240 E23
C1 470 PF

74LS175 E17: D3 R3(1), D2 R2(1), R2(0), D1 R1(1), R1(0), D0 R0(1), R0(2), CLR, CLK
[K-3] DAT 5 H; [K-3] DAT 3 H; [K-3] DAT 2 H; [K-3] DAT 0 H
M3; [K-7] DSET INT EN (1) H
M2; [K-7] SEC XMIT (1) H; [K-7] SEC XMIT (1) L
FA; [K-7] REQ TO SEND (1) H; [K-7] REQ TO SEND (1) L
[K-7] RINT EN (1) H
R31 2.4K; 1489 E13
74LS02 E2: [K-3] SEL Ø L, [K-3] OUT LB L; [K-7] SEL Ø OUT LB H

[K-3] INIT. L
[K-3] DAT 1 H; [K-7] SEL Ø OUT LB H
74LS74 E36
(-FD); [K-7] DTR (1) H
R32 2.4K; 1489 E13; [K-7] DTR (1) L
+3V

J1
[K-4] SD MARK H; 1488 E18; EIA XMIT DATA 2
[K-7] DTR (1) L; 1488 E18; EIA DATA TERMINAL READY 20
[K-7] REQ TO SEND (1) L; 1489 E18; (RS); EIA REQ TO SEND 4; (FB); EIA FORCE BUSY 25
[K-7] SEC XMIT (1) L; 1488 E18; EIA SEC XMIT DATA 11

[K-3] SEL Ø IN L
[K-3] INIT L

* ETCH CONNECTS PIN 11 OF BERG HOUSING TO PIN 1 OF E30 THROUGH STAKE PINS SD AND SD1. IF USAGE OF PIN 2 TO PIN 1 OF E30, CUT ETCH ON SIDE TWO CONNECTING STAKE PIN SD1 AND STAKE PIN SD, THEN WIREWRAP STAKE PIN DS TO STAKE PIN SD1.

(MODEM CONTROL CKT) K-7

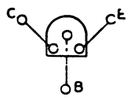
REVISIONS		
CHK	CHANGE No.	ECO

TITLE: ASYN LINE INTERFACE
SIZE: D
CODE: CS
NUMBER: M8017-AA-1
REV: J
SCALE:
SHEET 6 OF 6
DIST:

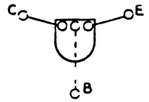
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VIEW FROM SIDE 1:

VENDOR NAME: GPSA(GE)



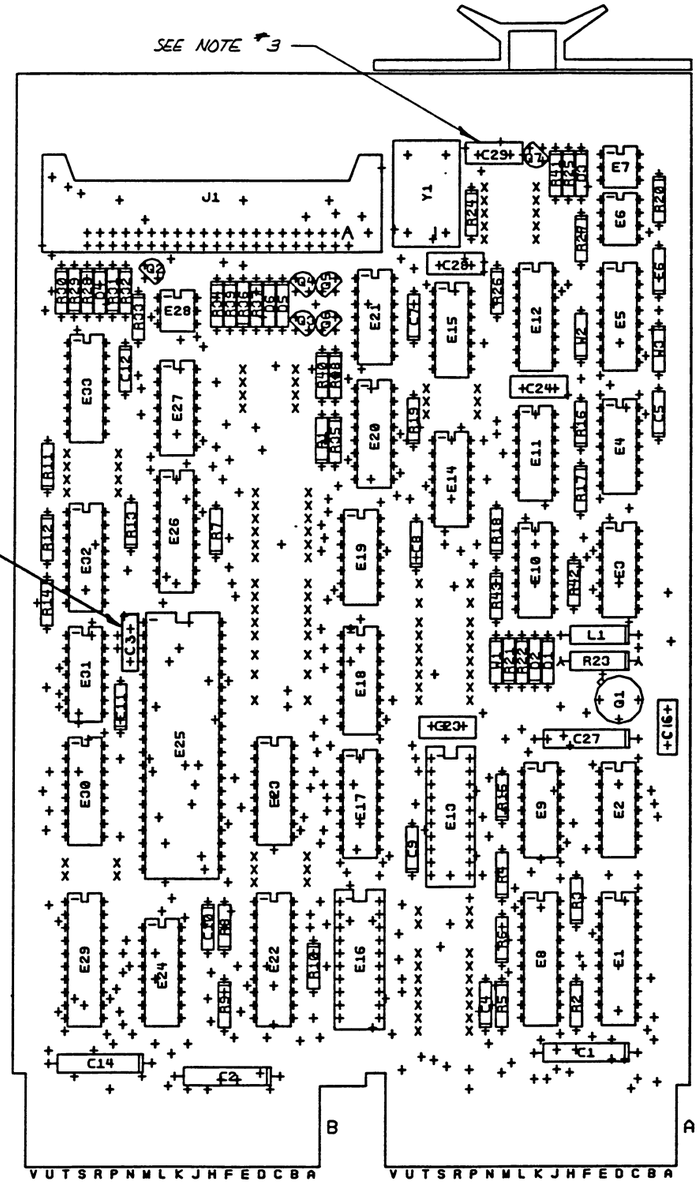
MOTOROLA, ITT
NATIONAL TRANSISTOR
NATIONAL SEMICONDUCTOR



ACTUAL Q2 INSERTION IS DEPENDANT UPON VENDOR VARIATION

SEE NOTE #3

SEE NOTE #2



NOTES:
1. 8 HOLES .0465 [+.000-.0045] MAYNARD ONLY.
2. C3 AND C16 ARE HAND INSERTED AT ASS'Y.
3. C29 TO BE INSTALLED IN FIELD OR BY CUSTOMER ONLY.
4. REMOVE THE FOLLOWING UNUSED FINGERS ON ARTWORK: ADI, AEI, AFI, AHI, AJI, AMI, ANI, ARI, ASI, AUI, BCI, BDI, BEI, BFI, BJI, BMI, BNI, BRI, BSI, BUI.

CHK	CHANGE NO	REV
TO	M8028-A8004	F
TC	M8028-A8006	H
TC	M8028-A8008	J

ETCH REV. E
P.C. DESIGN DATA BASE REV. E

SIGNATURES	DATE
DRN. F. SMART	14AUG77
CHK'D. F. SMART	14AUG77
ENG. M.D. MICHAUD	23AUG77
PROJ. ENG. M.D. MICHAUD	23AUG77
PROD. F. CORTAZZO	
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M8028-0-0	

digital

TITLE ASYNCHRONOUS LINE INTERFACE

SIZE	CODE	NUMBER	REV
D	UA	M8028-0-0	J

M8028-0-0 DUA J

MS#

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BAUD RATE SELECT JUMPERS						
RECEIVER	(R3)	(R2)	(RI)	(RØ)	BAUD	
TRANSMITTER	(T3)	(T2)	(TI)	(TØ)	RATE	
	I	I	I	I	50	
	I	I	I	R	75	
	I	I	R	I	110	* RECEIVER
	I	I	R	R	134.5	
	I	R	I	I	150	
	I	R	I	R	300	
	I	R	R	I	600	
	I	R	R	R	1200	
	R	I	I	I	1800	
	R	I	I	R	2000	
	R	I	R	I	2400	
	R	I	R	R	3600	
	R	R	I	I	4800	
	R	R	I	R	7200	
	R	R	R	I	9600	* TRANSMITTER
	R	R	R	R	19200	

I : INSTALLED R : REMOVED

DEVICE ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
A4, A5, A6, A8 A9, A10, A11, A12	A3, A7	CONSOLE ADDRESS 17756X *
A3, A7, A8 A9, A11, A12	A4, A5, A6 A10	DLVII-F UNIT #1 176500

ADDRESS SETUP DIAGRAM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø

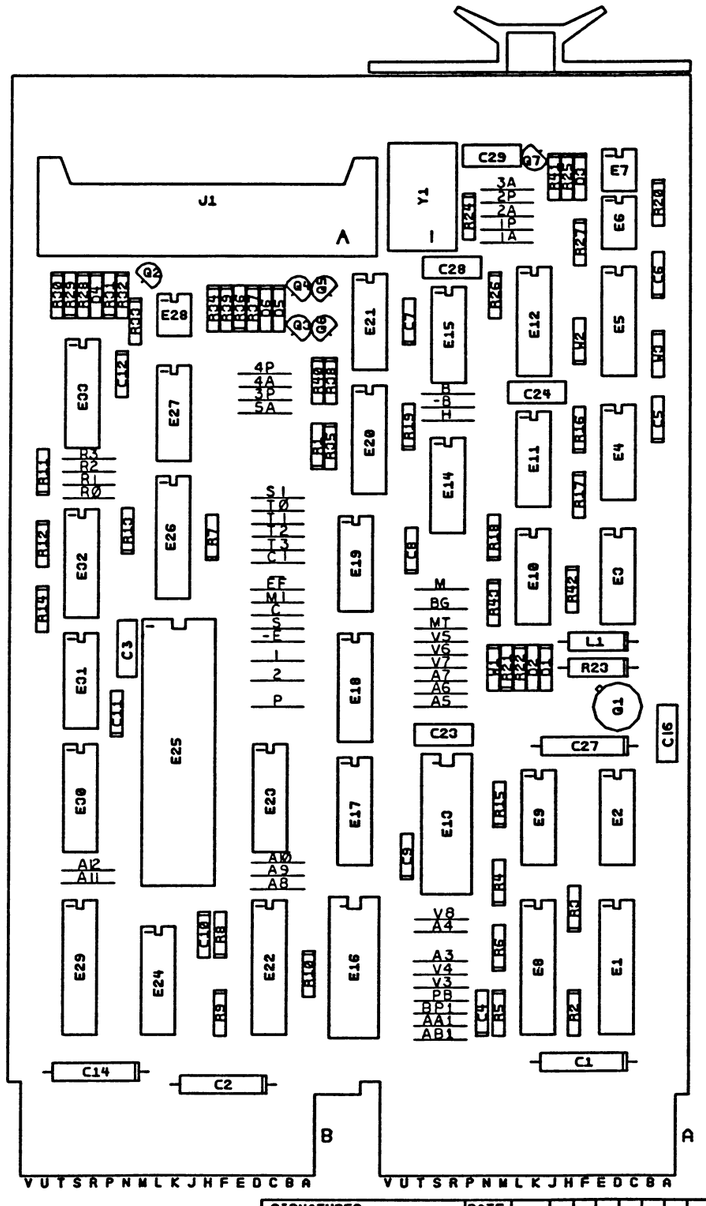
VECTOR ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
V4, V5	V3, V6, V7 V8	CONSOLE 60, 64 *
V6, V7	V3, V4, V5 V8	DLVII-F UNIT #1 300, 304

VECTOR SETUP DIAGRAM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø

MISCELLANEOUS JUMPERS			
JUMPERS IN	JUMPERS OUT	FEATURE	
1,2		5 DATA BITS	
1	2	6 DATA BITS	
2	1	7 DATA BITS	
	1,2	8 DATA BITS	*
P		PARITY CHECK	
	P	NO PARITY CHECK	*
-E		ODD PARITY	
	-E	EVEN PARITY	*
PB		PROG. BAUD RATES ENAB	
	PB	PROG. BAUD RATES DISAB	*
BG		BREAK GENERATION ENAB	*
	BG	BREAK GENERATION DISAB	
C,CI	S,SI	COMMON SPEED	*
S,SI	C,CI	SPLIT SPEED	
H		HALT ON FRAMING ERROR	*
	H	NO HALT ON FRAMING ERROR	
B	-B	BOOT ON FRAMING ERROR	
-B	B	NO BOOT ON FRAMING ERROR	*
-EF		ERROR FLAGS DISABLED	*
	-EF	ERROR FLAGS ENABLED	
1A,2A,3A	1P, 2P	ACTIVE RECIEVE 20 MA CURRENT LOOP	*
1P 2P	1A,2A,3A	PASSIVE RECIEVE 20 MA CURRENT LOOP	
4A, 5A	3P, 4P	ACTIVE TRANSMIT 20 MA CURRENT LOOP	*
3P, 4P	4A, 5A	PASSIVE TRANSMIT 20 MA CURRENT LOOP	
M	M1	FACTORY USE ONLY	*
MT		MAINTENANCE BIT ENABLED	
	MT	MAINTENANCE BIT DISABLED	*

NOTES:
1. * MODULE SHIPPED FROM FACTORY IN THIS CONFIGURATION.



NOTES:
1. 8 HOLES .0465 (+.000-.0045) MAYNARD ONLY

CH#	CHANGE NO	REV
1	M8028-A0008	D
	REVISED & REDRAWN	
2	M8028-A0009	E
3	M8028-A0008	F

SIGNATURES	DATE
DRN. B. BLODGETE	25JLY77
CHK'D. F. SMART	3AUG77
ENG. M.D. MICHAUD	29AUG77
PROJ. ENG. M.D. MICHAUD	29AUG77
PROD. F. CORTAZZO	13SEP77
SCALE — / —	
SHT. 1 OF 6	
NEXT HIGHER ASSY. D-UA-M8028-0-0	

digital

TITLE ASYN LINE INTERFACE

SIZE	CODE	NUMBER	REV
D	CS	M8028-Ø-1	F

ETCH REV. E

MS#_____

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+5V R1 10K

[K-5] SEL 2 IN L (EF) 74LS08 E19 74LS00 E14

[K-4] SEL 4 IN L

[K-3] IN WD L 74LS04 E11

* SEE NOTE 1

BIRQ5L AA1

BIRQ7L BP1

BIRQ6L AB1

DC0003 E8

[K-5] R DONE (I) H

[K-3] DAT 6 H

[K-1] SEL 0 OUT LB H

BINIT L AT2

[K-5] XRDY H

[K-3] DAT 6H

[K-4] SEL 4 OUT LB H

BIAKI L AM2

RQSTA H
ENA DATA H
ENA CLK H
INTERRUPT BIRQL
RQST B H
ENB DATA H
ENB CLK H
BDIN L
BIAKI L BIAKOL

74LS04 E11

[K-3] INIT H

[K-3] INIT L

[K-3] R INT EN (I) H

AL2 BIRQ4L

[K-3] T INT EN (I) H

VECTOR H

VEC RQST B H

AN2 BIAKO L

R2 330 +5V
R3 680

R5 330 +5V
R6 680

+5V R4 330

AH2 BDIN L

[K-3] DIN L

74LS04 E11

[K-4] SO MARK L

[K-3] SO L

[K-3] SO H

BA1 BDC OK H

[K-3] DC OK L

(H) AP1 B HALT L

[K-5] FE H

8641 E12

+5V R7 1K [K-3] +3V

DC0004 E1 PROTOCOL

BWT BT L AK2
BSYNC L AJ2
BDOUT L AE2
BDIN L
B DAL 2
B DAL 1
B DAL 0
VECTOR
RXCX

[K-3] IN WD L
OUT LB L [K-3] OUT HB L
OUT HB L [K-3] OUT LB L
REPLY L AF2 BRPLY L
SEL 6 L [K-3] SEL 0 L
SEL 4 L [K-3] SEL 2 L
SEL 2 L [K-3] SEL 4 L
SEL 0 L [K-3] SEL 6 L

R8 1K C23 470PF

+5V AA2, BA2
AC2, AT1 BC2, BT1 .047 UFD C4-12
C1 6.8 UFD
+C14 6.8
GND
C16 .047
C2 6.8
+12V AD2, BD2

[K-3] DAT 2 H
[K-3] DAT 1 H
[K-3] DAT 0 H

[K-3] DAT 15 H
[K-3] DAT 12 H
[K-3] DAT 11 H
[K-3] DAT 14 H
+5V

[K-3] DAT 10 H
[K-3] DAT 13 H

R9 2.4K R10 2.4K

XMIT H REC H
DAT3 DAT2 DAT1 DAT0
BUS3 BUS2 BUS1 BUS0
JA3 JA2 JA1
JV3 JV2 JV1
MENB L
MATCH H

DC0005 E22 SST

BV2 BDAL 15 L
BS2 BDAL 12 L
BR2 BDAL 11 L
BU2 BDAL 14 L

DC0005 E23 SST

BP2 BDAL 10 L
BN2 BDAL 9 L
BM2 BDAL 8 L
BT2 BDAL 13 L

[K-3] DAT 7 H
[K-3] DAT 6 H
[K-3] DAT 5 H
[K-3] DAT 0 H

DC0005 E13 SST

BL2 BDAL 7 L
BK2 BDAL 6 L
BJ2 BDAL 5 L
AU2 BDAL 0 L

[K-3] DAT 4 H
[K-3] DAT 3 H
[K-3] DAT 2 H
[K-3] DAT 1 H

DC0005 E16 SST

BH2 BDAL 4 L
BF2 BDAL 3 L
BE2 BDAL 2 L
AV2 BDAL 1 L

+5V
BBS7 L AP2

NOTE: 1 BRACKETED PIN #'S REFER TO DC104 - DC107 CHIPS.

[K-3]

DRN		FIRST USED ON	digital
CHK'D			
ENG.		TITLE	ASYNC LINE INTERFACE (BUS RECEIVERS & DRIVERS)
PROJ. ENG.			
PROD.			
NEXT HIGHER ASSY.			
SCALE		SIZE D CODE CS NUMBER M8028-0-1 REV. F	
SHEET 2 OF 6		DIST	

REVISIONS: REV. | CHANGE NO. | CHK

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+5V
R11 10K R12 10K R13 10K R14 10K
(R0) (R1) (R2) (R3)
[K-3] DAT 12 H
[K-3] DAT 13 H
[K-3] DAT 14 H
[K-3] DAT 15 H
74LS298 E32
A2 A1 B2 B1 C2 C1 D2 D1 WS CLK
R0(1) R1(1) R2(1) R3(1)
R15 10K
C24 470 PF
R16 1K
R17 1.5K
[K-3] DC ON L
[K-3] DAT 11 H
74LS08 E19
74LS08 E14
(P8)
[K-3] SEL 4 L
[K-3] OUT HB L
[K-3] DIN L
74LS02 E2
74LS32 E4
[K-4] SEL 4 IN L

+3V
STT STR
PA PB PC PD FP ST EXT1 EXT2
BK1 (SEE NOTE 1)
INT R CLK H
+12V
(T0) (T1) (T2) (T3)
+5V
OCS 5.0688 MHZ Y1
74LS14 E27
74LS27 E31
74LS08 E19
[K-4] 110 BAUD H

J1
CONN CLK INPUT H
EXT R CLK H
(C1)
[K-7] SI MARK H
[K-4] SO MARK H
[K-4] MAINT (1) H
EXT T CLK H
BL1
BK1
74LS153 E23
STB1 STB0 A0 B0 C0 D0 A1 B1 C1 D1 S1 S0 F0 F1
(C) (S)
[K-6] R CLK H
[K-6] T CLK H
[K-6] SERIAL IN H
(S1)
J1 U HH
CONN CLK EN L
+5V R15 10K

N/C
74LS64 E11
(1) (2)
7548 E6
+12V
421 100
422 470
Q1 2N2905A
D1 D672
423 82 JW
L1 270 uH
C27 68 MF 35V DC
D2 IN4742
AK1 -12V @ 40 mA MAX
W1 W2 W3
E5 74LS390

(BG) R18 10K +5V
[K-3] +3V
[K-3] DAT Ø H
[K-3] OUT LB L
[K-3] SEL 4 L
[K-3] DAT 2 H
[K-3] INIT L
(MT) R42 10K +5V
[K-4] SEL 4 OUT LB H
74LS74 E10
74LS02 E2
[K-4] BREAK(1) H
[K5] SERIAL OUT H
74LS08 E14
74LS04 E11
J1 SS
[K-3] SO MARK L
[K4] SO MARK H
[K-4] MAINT (1) H
[K-4] MAINT (1) L

AL1 [K4] -12V (SEE NOTE 2)

NOTES:
1) BK1 AND BL1 ARE TIED TOGETHER ON THE BUS.
2) AK1 AND AL1 ARE TIED TOGETHER ON THE BUS.

(TCSR, BAUD RATE CKT. & -12V SUPPLY) [K-4]

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN LINE INTERFACE	D	CS	M8028-0-1	F
SCALE —	SHEET 3 OF 6	DIST.		

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[K-3] SEL 2 L
[K-3] DIN L
74LS32 E4
[K-3] SEL 2 IN L
74LS08 E3
[K-3] RDA L
[K7] ADR (1) L
M
10 K R43
+5
[K-3] R CLK H
[K-4] SERIAL IN H
[K-3] DAT 7 H
[K-3] DAT 6 H
[K-3] DAT 5 H
[K-3] DAT 4 H
[K-3] DAT 3 H
[K-3] DAT 2 H
[K-3] DAT 1 H
[K-3] DAT Ø H
[K-3] SEL 6 L
[K-3] OUT LB L
74LS32 E4
[K-4] T CLK H
[K-3] INIT H
[K-3] +3V
[K-4] 110 BAUD H
CONN CLK EN L
(M1)
(2)
(1)
(P)
(E)
CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
DS
TCP
CLR LDC NB2 NB1 NP EP 2SB
UART E25
R DONE
OR ERR
FR ERR
P ERR
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RDØ
SERIAL OUT
X RDY
EOC
[K-4] -12V
C3.47 UF
[K-5] FR ERR H
[K-5] P ERR H
[K-4] MAINT (1) L
74LS04 E11
74LS08 E3
[K-5] FE H
74LS74 E9
[K-3] INIT L
[K-5] RDA L
[K-5] R DONE (1) H
8097 E18
[K-3] DAT 7 H
[K-3] DAT 6 H
[K-3] DAT 5 H
[K-3] DAT 4 H
[K-3] SERIAL OUT H
[K-5] XRDY H
8097 E24
[K-3] DAT 3 H
[K-3] DAT 2 H
[K-3] DAT 1 H
[K-3] DAT Ø H
[K-5] SEL 2 IN L
BDMGI L
BDMGO L
AR2
AS2

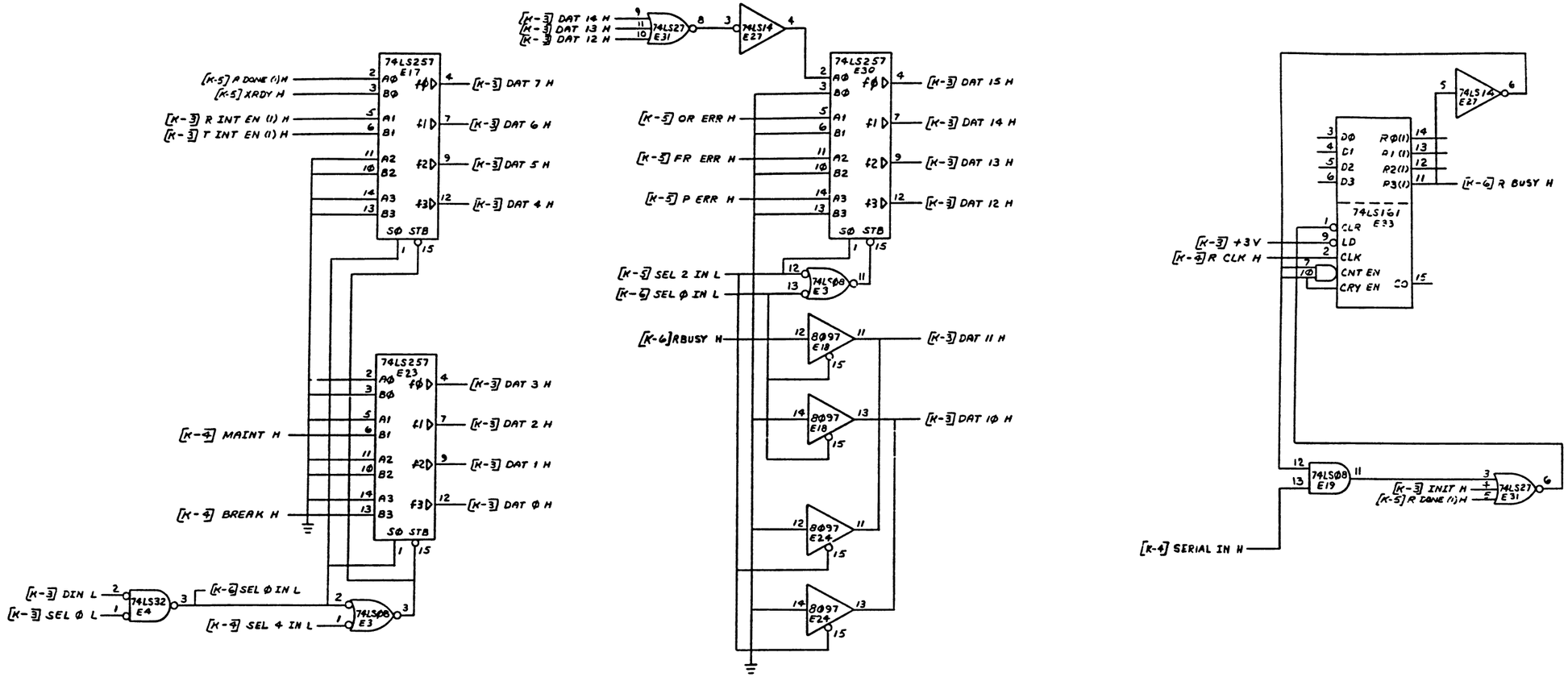
(UART CKT) [K-5]

REVISIONS
CHK | CHANGE NO. | REV

TITLE ASYN LINE INTERFACE
SIZE D CODE CS NUMBER M8028-0-1 REV. F
SCALE — SHEET 4 OF 6 DIST.

8 7 6 5 4 3 2 1

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(INTERNAL BUS DRIVERS & RCVR BUSY CKT) [K-6]

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN LINE INTERFACE	D	CS	M8028-0-1	F
SCALE —/—	SHEET 5 OF 6	DIST.		

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[K-4] SO MARK H

[13] EIA RECEIVER DATA H

TTL SI MARK L

[K-7] -12V

+12V

1488 E21

1489 E15

74LS14 E27

C28

J1

V EIA REQ TO SEND [4]

C EIA FORCE BUSY [25]

DD EIA DATA TERMINAL READY [20]

F EIA XMIT DATA [2]

M EIA INTLCK

[X7] SI MARK H

INSERT FOR TTY ONLY

+5V

4N26-2 E7

R24 1K

R41 10K

R20 1M

C29

Q7 A85

+3V

R25 220

D9 D672

R26 270

R27 180

(1A) (1P) (2A) (2P) (3A)

K

S

H

20 MA RECEIVE [7] [3]

[K-3] DAT Ø H

[K-3] SEL Ø L

[K-3] OUT LB L

74LS02 E2

74LS74 E9

[K-7] SEL Ø OUT LB H

[K-7] RDR (1) L

[K-3] INIT H

[K-6] RCVR BUSY H

R28 470

R30 68

R29 680

Q2 A55

D4 D672

R31 47

R32 47

[K-4] -12V

PP

READER RUN [6]

EE [4]

NOTE:

1. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC05-C, BC01V OR BC05L CABLES. THESE CABLES ALSO CONNECT J1 PIN M TO PIN E.
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOK CONNECTOR WHEN USING THE BC05-M CABLE. THIS CABLE ALSO CONNECTS J1 PINS H TO E.

+5V

R33 180

4N26-2 E23

R34 68K

A55 Q3

MCL 13Ø1 D6

[K3] SOH

D5 D672

[K3] SOL

LS14 E27

R35 1K

+12V

R36 1K

R37 3K

R38 1K

R39 47

R40 47

Q4 A55

Q5 A05

Q6 A05

(3P) (4A) (5A) (6P)

AA

KK

A B U3 VV

TT

20 MA TRANSMITTER [4] [2]

(CURRENT LOOP CKT) [K-7]

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN LINE INTERFACE	D	CS	M8028-0-1	F
SCALE —	SHEET 6 OF 5	DIST.		

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DETAIL -B
Q1 MOUNTING

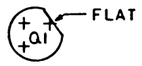
BEND MIDDLE LEAD OUT



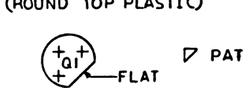
TO-92
(AS PICTURED ON UA AT RIGHT)



TO-18
(METAL CAN)



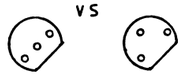
TO-105/106
(ROUND TOP PLASTIC)

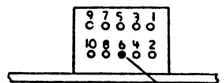


FOR LEADS IN A TRIANGULAR PATTERN

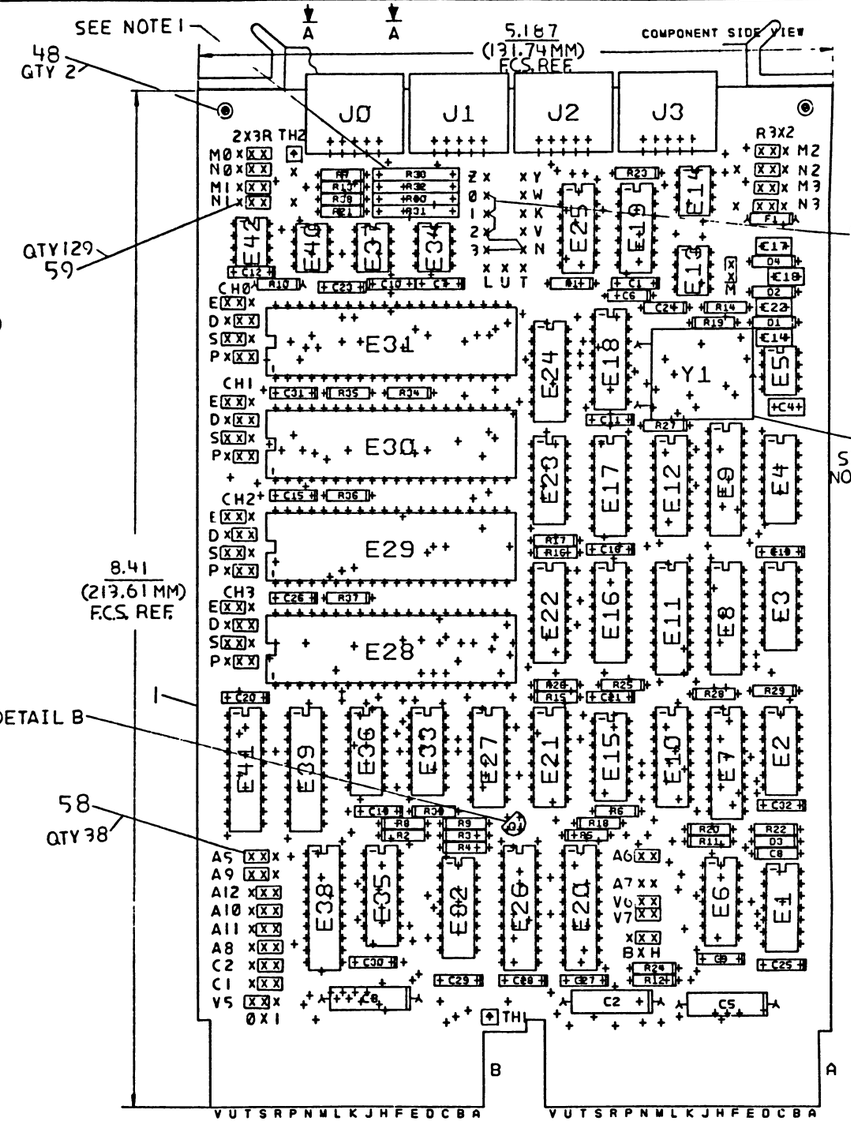
NOTE: DIFFERENCE

TO-92 PAT





DETAIL A-A
TYP 4 PLACES



CHK	DRAWN BY	ENGINEER	CHANGE NO	DATE	REV
JT	E.S. Fraser	T. Cavell	M8043-MK9	24 APR 84	L

CHK	DRAWN BY	ENGINEER	CHANGE NO	DATE	REV

NOTES:
1. R30-R33 ARE OPTIONAL.
2. CASE OF Y1 MUST BE INSULATED FROM PCB WITH ITEM 53.

STEP ±	↑ Y AXIS ___ STEP ___ TIMES
REPEAT	→ X AXIS 5.187 STEP 1 TIMES

ETCH REV. F1-P2

SIGNATURES	DATE
DRN. B.H. FRASER	
CHK'D.	
MECH. ENG.	
PROJ. ENG.	
PROD.	
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M8043-0	

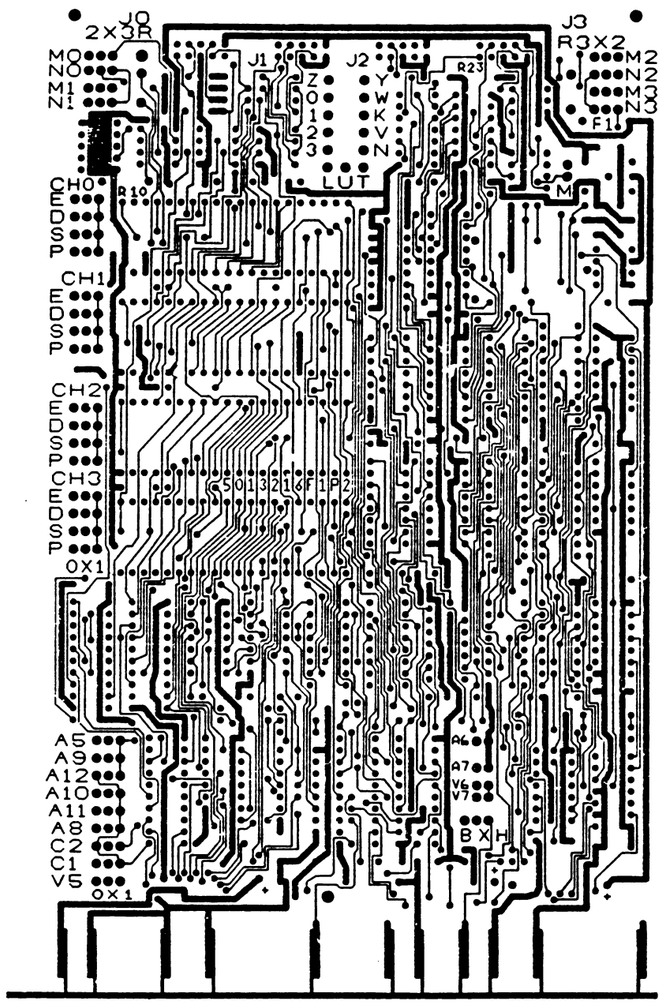
digital

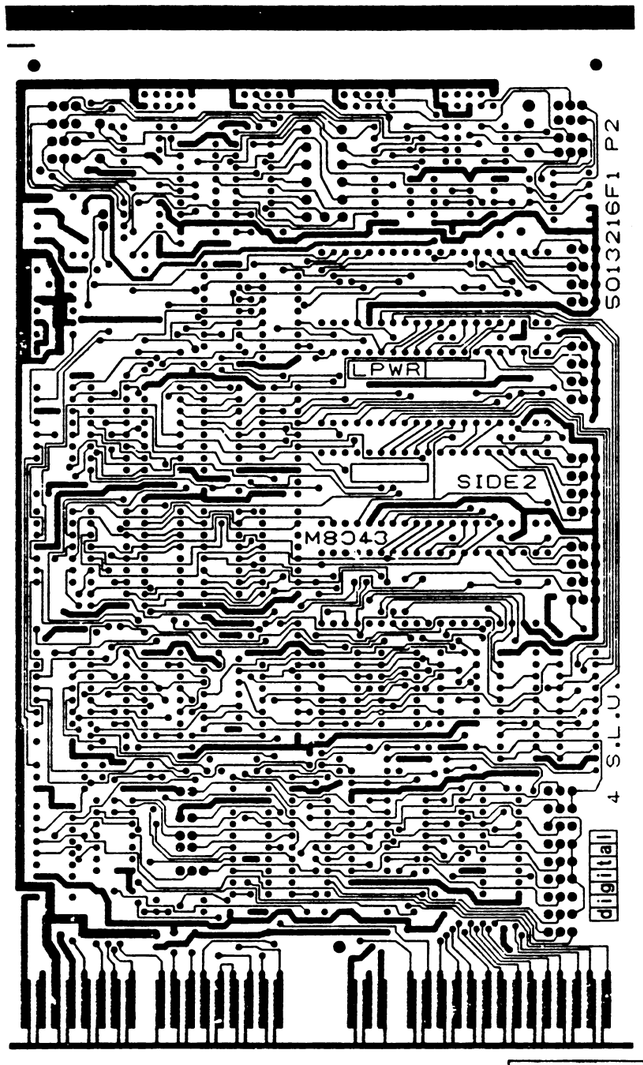
TITLE 4 SERIAL LINE PER CTLR.

SIZE	CODE	NUMBER	REV
D	UA	M8043-0-0	L

1 MS#302161

1934





DATE	ECO # AND REV	REV
	M8043-MK009	J
	21 MAR 84	
	CCAHILL	
	24-MAY-84	

digital

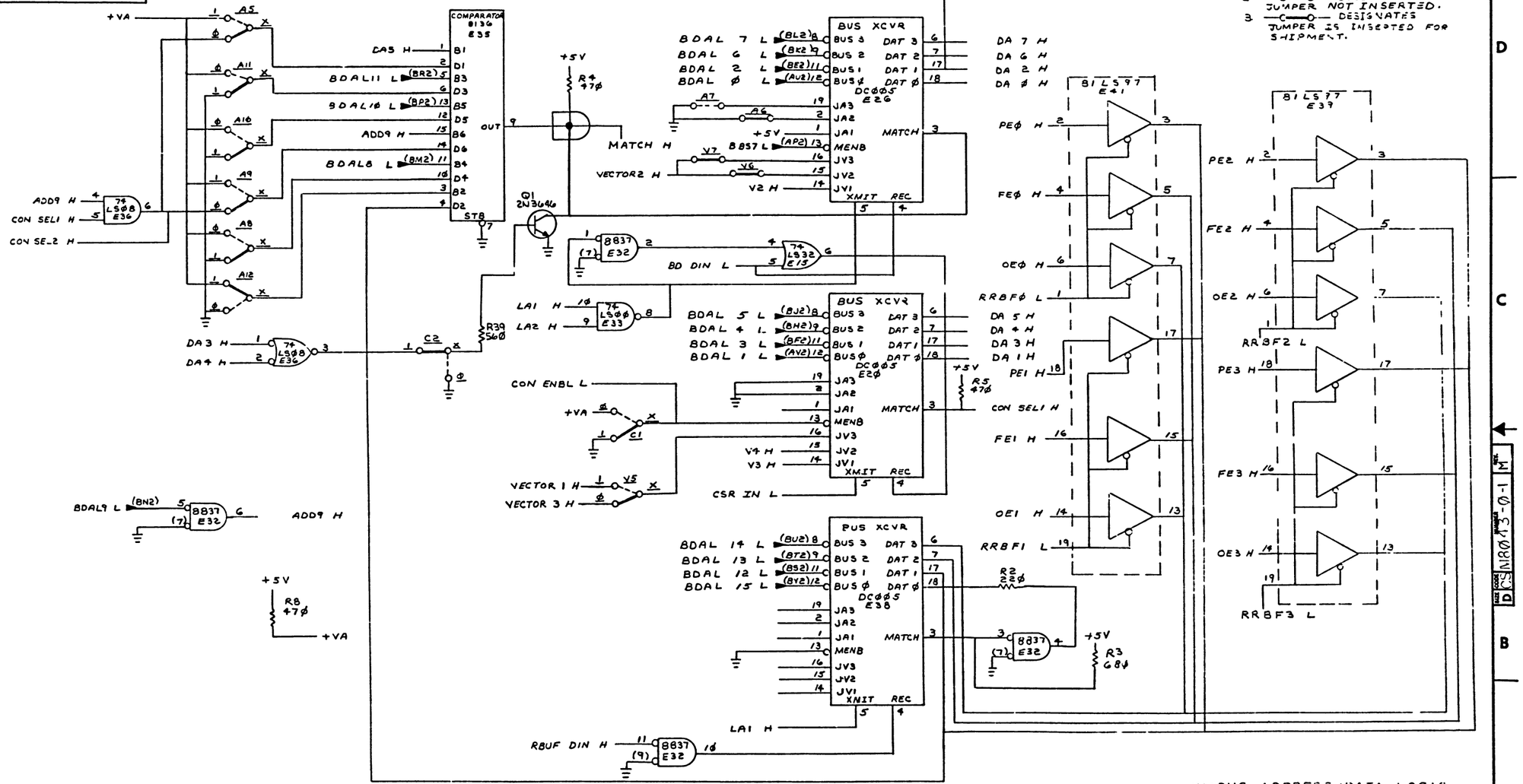
ETCH CUT DRAWING

DEC 5013216-0-0 J

D-UA-M8043-0-0 2/1

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NOTES:
1. UNDERLINED TERM DESIGNATES LABEL IN ETCH.
2. —o--o— DESIGNATES JUMPER NOT INSERTED.
3. —o—o— DESIGNATES JUMPER IS INSERTED FOR SHIPMENT.



REVISIONS			
CHK	CHANGE NO.	REV.	
[illegible]	M8043-MR001	D	
[illegible]	M8043-MR002	E	
[illegible]	M8043-MR003	F	
[illegible]	M8043-MR004	H	
[illegible]	M8043-MR005	J	
[illegible]	M8043-MR006	K	
[illegible]	M8043-AB0008	L	
[illegible]	M8043-1K0009	M	

KI:BUS ADDRESS/DATA LOGIC

DRN. E.Wilson	30 JAN 78	FIRST USED ON DLV11-J	digital		
CHK'D R.J.Cowles	26 Feb 78				
ENG. Thomas Joyce	2 MAR 78	TITLE 4 SERIAL LINE PER. CTLR.			
PROJ. ENG. Jim Joyce	27 MAR 78				
PROD. [illegible]	3/4/78				
NEXT HIGHER ASSY. G-DT-ME043-0		SIZE D	CODE CS	NUMBER M8043-C-1	REV - M
SCALE NONE					
SHEET 1 OF 7		DIST.			

M8243-0-1 M

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NOTES:
1. TO ENABLE HALT ON RECEIVING BREAK, CONNECT X TO H. TO ENABLE BOOT ON RECEIVING BREAK, CONNECT X TO B.

(SEE NOTE 1)

FE3 H — 8881 E6 — X — B (BA1) BDCOK H; H (AP1) BHALT L

BDMGI L (AR2)

BDMGO L (AS2)

BSYNC L (AJ2) — 8640 E1 — SYNC H

BD SEL L (16), BDOUT L (AE2) — 8640 E1 — 74 LS04 E2 — BD DOUT H

LA0 H — 7402 E3 — BD DOUT LB H

BD SEL L — 7402 E3 — 74 LS04 E2 — BD DIN L; BD DIN H

BDIN L (AH2) — 8640 E1 — 74 LS04 E2 — DIN L

D0Ø3 D3; R22 2.2K; C8 1000 PF

BD DIN H, BD DOUT H — 74 LS32 E4 — VECTOR1 H — 8640 E1 — 74 LS04 E2 — 8881 E6 — 16 (AF2) BRPLY L; RPLY L; RPLY H

REVISIONS		
CHK	CHANGE NO.	REV

K2: CONTROL AND HALT/ECCT LOGIC

TITLE	SIZE	CODE	NUMBER	REV.
4 SERIAL LINE PER. CTLR.	D	CS	M8Ø43-Ø-1	M
SCALE NONE — SHEET 2 OF 7 — DIST.				

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LATCH 74LS174 E21

MATCH H
DA1 H
DA2 H
DA3 H
CON SEL2 H
DA4 H
DAØ H
BD SEL L
SYNC H
SYNC H

D0 R0(1) D1 R1(1) D2 R2(1) D3 R3(1) D4 R4(1) D5 R5(1) CLR CLK

74 LS32 E15

74 LS32 E15

8837 E32 — BD SEL H

8837 E32 — LA1 L, LA1 H

BD SEL L
BD DOUT LB H

74 LSØ8 E36

LA2 H
LA1 H

74 LSØØ E33

+5V

R15 68Ø R16 68Ø R17 68Ø R 68Ø

RPLY H

3-TO-8 DECODER 74LS155 E27

LA4 H
LA3 H

FB3 FB2 FB1 FBØ FA3 FA2 FA1 FAØ

WXBF3 L
WXBF2 L
WXBF1 L
WXBFØ L
RRBF3 L
RRBF2 L
RRBF1 L
RRBFØ L

7402 E3

LA2 H
BD DIN L

RBUF DIN H
LA1 L

ADDR & LATCH 74LS259 E17

LA3 H
LA4 H
LA2 H

A B C — F0 F1 F2 F3 F4 F5 F6 F7 — DATA — C E

RDR ENBL PLSØ H
RDR ENBL PLS1 H
RDR ENBL PLS2 H
RDR ENBL PLS3 H
BRKØ H
BRK1 H
BRK2 H
BRK3 H

74 LS32 E15

74 LS08 E36

LA2 H
RPLY L
DAØ H

INITO L

74 LSØØ E33

BD DOUT LB H
LA1 L

3 TO-8 DECODER 74LS138 E12

LA3 H
LA4 H
LA2 H

SELA SELB SELC — D0 D1 D2 D3 D4 D5 D6 D7

LA1 H
BD DOUT LB H

EN

RINT ENBLØ STB L
RINT ENBL1 STB L
RINT ENBL2 STB L
RINT ENBL3 STB L
XINT ENBLØ STB L
XINT ENBL1 STB L
XINT ENBL2 STB L
XINT ENBL3 STB L

8-TO-1 MUPLX 74LS251 E22

R INT ENBLØ H
R INT ENBL1 H
R INT ENBL2 H
R INT ENBL3 H
X INT ENBLØ H
X INT ENBL1 H
X INT ENBL2 H
X INT ENBL3 H
LA3 H
LA4 H
LA2 H

D0 D1 D2 D3 D4 D5 D6 D7 A0 A1 A2 — OUTY OUTW — STB

DA6 H

LA1 L
BD DIN H

74 LSØØ E33

CSR IN L

RRBFØ L
RDR ENBL PLSØ H

74 LS86 E23

DRRØ L

RRBF1 L
RDR ENBL PLS1 H

74 LS86 E23

DRR1 L

RRBF2 L
RDR ENBL PLS2 H

74 LS86 E23

DRR2 L

RRBF3 L
RDR ENBL PLS3 H

74 LS86 E23

DRR3 L

8-TO-1 MUPLX 74LS251 E24

BRKØ H
BRK1 H
BRK2 H
BRK3 H
LA3 H
LA4 H
LA2 H

D0 D1 D2 D3 D4 D5 D6 D7 A0 A1 A2 — OUTY OUTW — STB

DAØ H

CSR IN L

8-TO-1 MUPLX 74LS251 E16

DRØ H
DR1 H
DR2 H
DR3 H
XRDYØ H
XRDY1 H
XRDY2 H
XRDY3 H
LA3 H
LA4 H
LA2 H

D0 D1 D2 D3 D4 D5 D6 D7 A0 A1 A2 — OUTY OUTW — STB

DA7 H

CSR IN L

REVISIONS

CHK	CHANGE NO.	REV

K3: ADDRESS LATCH AND REGISTER LOGIC

TITLE	SIZE	CODE	NUMBER	REV.
4 SERIAL LINE PER. CTLR.	D	CS	M8043-Ø-1	M

SCALE NONE | SHEET 3 OF 7 | DIST.

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+5V
R11 330
R24 680

DR0 H
DA6 H
BIAKI L (AM2)
BINIT L (AT2)
DIN L
DRI H

DC003 E7
RQSTA ENA ST
ENA DAT VEC RQSTB
BIAKI BIRQ
BINIT BIAKO
BDIN INITO
RQSTB VECTOR
ENB DAT ENB ST
ENA CLK ENB CLK

R INT ENBL0 H
INITO L
R INT ENBLI H

R INT ENBL0 STB L
R INT ENBLI STB L

DR2 H
R25 470
+5V
DR3 H

DC003 E11

R INT ENBL2 H
R INT ENBL3 H

R INT ENBL2 STB L
R INT ENBL3 STB L

XRDY0 H
R26 470
+5V
XRDY1 H

DC003 E9

X INT ENBL0 H
X INT ENBLI H

X INT ENBL0 STB L
X INT ENBLI STB L

XRDY2 H
R27 470
+5V
XRDY3 H

DC003 E8

X INT ENBL2 H
X INT ENBL3 H

X INT ENBL2 STB L
X INT ENBL3 STB L

+5V
R28 470
74LS04 E8
8881 E6
(AL2)
BIRQ L

256 X 4 ROM 82S129 E10
E1 A1 A2 A3 A4 A5 A6 A7 E2 A0
O1 O2 O3 O4
R29 470
R20 470
+5V
VECTOR2 H
V2 H
V3 H
V4 H
SEE TABLE BELOW
CON ENBL L

4049 E18
INITO H

74LS32 E4
VECTOR2 H
VECTOR1 H
VECTOR 3 H

+5V
R12 330
R6 680
(AN2)
BIAKO L

	CON ENBL L = 0				CON ENBL L = 1			
E1 0	VECTOR 2 H	V2 H	V3 H	V4 H	VECTOR 2 H	V2 H	V3 H	V4 H
A1 = 1	1	0	0	0	1	0	0	0
A1 · $\overline{E1}$ = 1	1	0	1	0	1	0	1	0
A2 = 1	1	0	0	1	1	0	0	1
A2 · A3 = 1	0	0	0	1	1	0	1	1
A4 = 1	1	1	0	0	1	1	0	0
A4 · A5 = 1	1	1	1	0	1	1	1	0
A6 = 1	1	1	0	1	1	1	0	1
A6 · A7 = 1	0	1	0	1	1	1	1	1
$\overline{E1}$ = 0 & A1-7 = 0	0	0	0	0	0	0	0	0

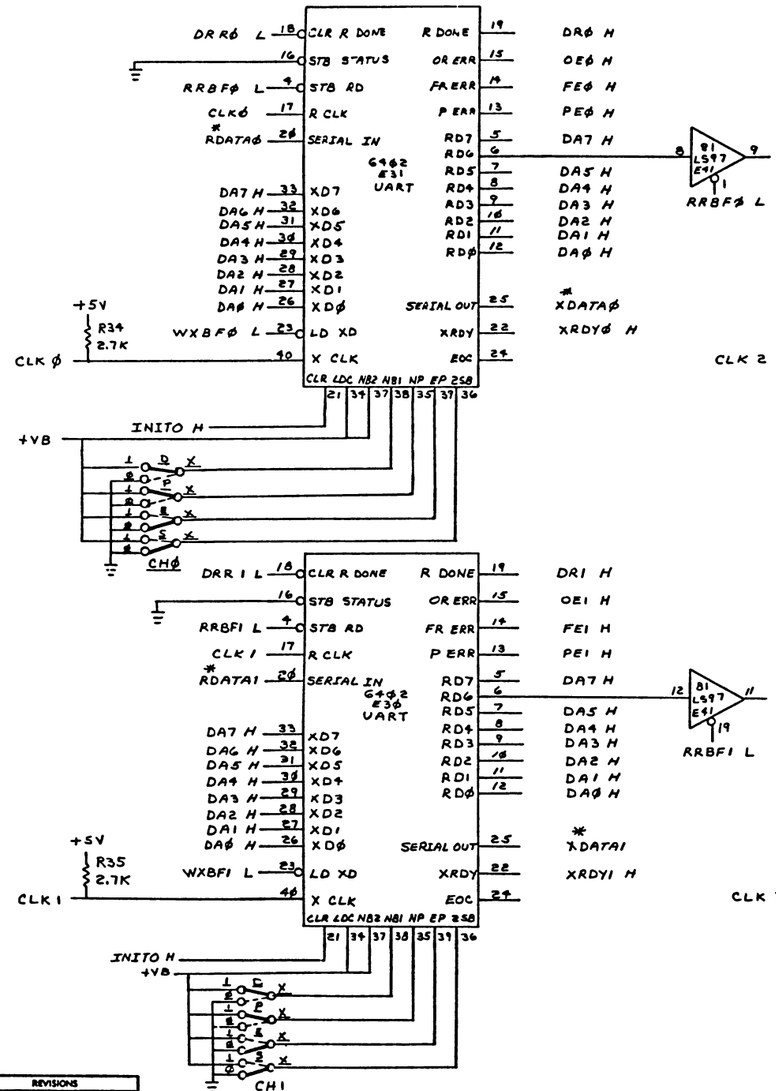
REVISIONS
CHK	CHANGE NO	REV

K4: INTERRUPT, VECTOR AND INIT LOGIC

TITLE	SIZE	CODE	NUMBER	REV.
4 SERIAL LINE PER. CTLR.	D	DCS	M8043-0-1	.M
SCALE NONE SHEET 4 OF 7	DIST.			

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NOTES:
* 5. Y HIGH = MARK = 1.
Y LOW = SPACE = Ø



LABEL	UART PARAMETER	X = Ø	X = 1	COMMENTS
D	NUMBER OF DATA BITS	7 BITS	8 BITS	LEAST SIGNIFICANT BITS ARE TRANSMITTED FIRST
S	NUMBER OF STOP BITS	1 BIT	2 BIT	
P	PARITY ENABLE BIT	PARITY GENERATION AND DETECTION ENABLED	PARITY BIT IS DELETED, PARITY ERROR = Ø.	
E	EVEN PARITY ENABLE	ODD PARITY ENABLED	EVEN PARITY ENABLED	ONLY WHEN P = 1.

K5; UART LOGIC

REVISIONS
CHK | CHANGE NO. | REV

TITLE 4 SERIAL LINE PER. CTLR.
SIZE D | CODE CS | NUMBER M8Ø43-Ø-1 | REV. M
SCALE NONE | SHEET 5 OF 7 | DIST.

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NOTES:
6. CLKØ-3 ARE WIREWRAP JUMPERED TO REQUIRED BAUD RATE.
7. JUMPER IS REMOVED FOR MFG. TESTING ONLY.
8. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE	GND	+5V	+12V	-12V
14 PIN DIP	7	14	—	—
16 PIN DIP	8	16	—	—
18 PIN DIP	9	18	—	—
28 PIN DIP	14	28	—	—
6402	3	1	—	—
MH002	*	—	*	—
8640	1	8	—	—
9636	4	—	8	5
9637	4	1	—	—
9638	4	1	—	—
4049	8	1	—	—

* SEE SCHEMATIC

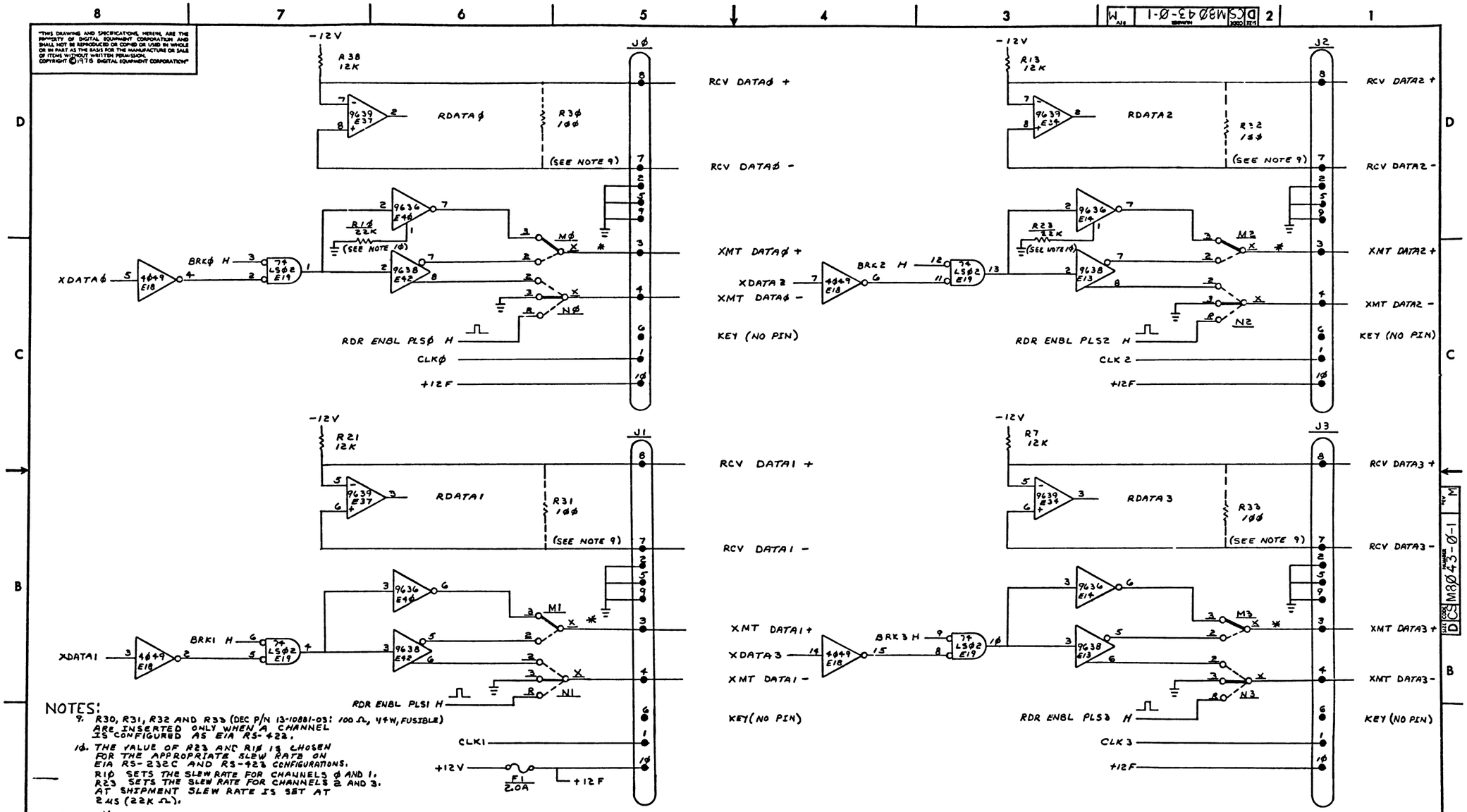
Y1 614 +KHZ
R19 1M
R18 2.2K
C6 100 PF
C24 33PF
4049 E18
74Ø2 E3
M (SEE NOTE 7)
74 LS04 E2
74 LS32 E4
COUNTER 74LS393 E25
1QD 1QC 1QB 1QA 2QD 2QC 2QB 2QA CLR1 CLR2 CLK2 CLK1
R1 22Ø
(SEE NOTE 6)
CLK3 CLK2 CLK1 CLKØ
1.5KB 3ØØB 6ØØB 1.2KB 2.4KB 4.8KB 9.6KB 19.2KB 38.4KB
+5V AA2, BV1, BA2
GRD AJ1, AM1, AT1; BJ1, BM1, BT1; BC2
C2 8Mf C3 8Mf C1 .Ø47 Mf C9 .Ø47 Mf C11 THRU C13 .Ø47Mf C15 .Ø47Mf C16 .Ø47Mf C19 THRU C21 .Ø47Mf C25 THRU C32 .Ø47Mf C7 .Ø47Mf
+12V (AD2)
GRD (AC2)
C5 8Mf C4 .47Mf C23 .Ø47Mf
MH ØØ2G E5
C18 .47Mf C14 .47Mf C22 .47Mf C17 .47Mf C1Ø .Ø47Mf
D4 DGG4 D2 DGG4 D1 DGG4
-12V +5V

K6: PWR DIST, BAUD RATE GEN & -12V CIRCUITRY

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
4 SERIAL LINE PER. CTLR.	D	DCS	M8Ø43-Ø-1	.M
SCALE NONE SHEET 6 OF 7	DIST.			

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NOTES:

9. R30, R31, R32 AND R33 (DEC P/N 13-10881-03: 100 Ω, ¼W, FUSIBLE) ARE INSERTED ONLY WHEN A CHANNEL IS CONFIGURED AS EIA RS-422.
10. THE VALUE OF R23 AND R10 IS CHOSEN FOR THE APPROPRIATE SLEW RATE ON EIA RS-232C AND RS-423 CONFIGURATIONS. R10 SETS THE SLEW RATE FOR CHANNELS Ø AND 1. R23 SETS THE SLEW RATE FOR CHANNELS 2 AND 3. AT SHIPMENT SLEW RATE IS SET AT 2 µS (22K Ω).
11. * V LOW = MARK = 1, V HIGH = SPACE = Ø

REVISIONS		
CHK	CHANGE NO.	REV

K7: LINE INPUT/OUTPUT LOGIC

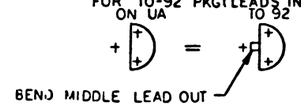
TITLE	SIZE	CODE	NUMBER	REV.
4 SERIAL LINE PER. CTLR.	D	CS	M8Ø43-Ø-1	M
SCALE NONE	SHEET 7 OF 7	DIST.		

DCS M8Ø43-Ø-1 M

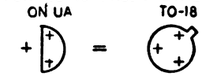
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NOTES:
1. PIN #6 OF J1 MUST BE CUT OUT. SEE DETAIL "A-A"
2. ITEM #46 IS PUT IN LOCATIONS PIN 2 THRU 7 OF J2
3. MFG. MAY OPTIONALLY PLACE TRANSIPADS (ITEM #49) UNDER Q4 & Q7
4. PLACEMENT OF Q1 THRU Q3, Q5 & Q6 IS:

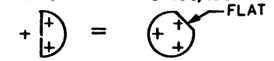
FOR TO-92 PKG (LEADS IN-LINE)



FOR TO-18 PKG. (METAL CAN)



FOR TO-105/106 PKG (ROUND TOP PLASTIC)



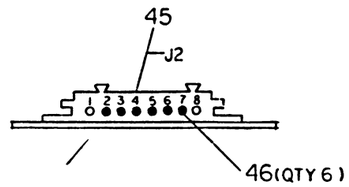
FOR LEADS IN TRIANGULAR PATTERN



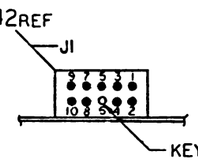
NOTE: DIFFERENCE



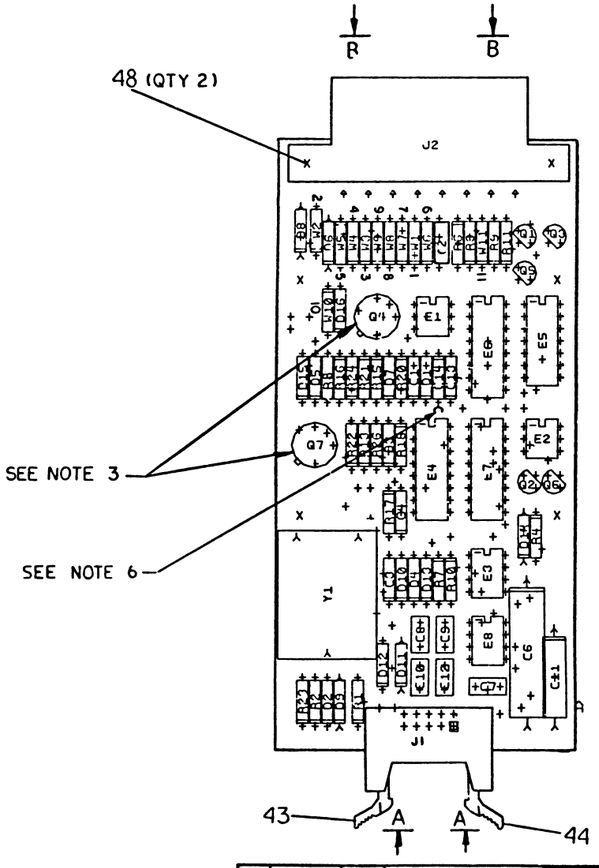
5. R8 IS ENGINEERING OPTIONAL COMPONENT.
6. C14 IS OPTIONAL. ONLY INSTALLED FOR ASR-33 USE



DETAIL "B-B"
(SEE NOTE #2)



DETAIL "A-A"
(SEE NOTE #1)



REVISIONS				
SYM	CHANGE NO.	REV.		
A	5413679-0-0	A	8 DEC 78	J. KING
B	5413679-0-0	B	27 JUL 79	J. KING
C	5413679-0-0	C	31 AUG 79	J. KING
D	5413679-0-0	D	26 SEP 79	J. KING
E	5413679-0-0	E	3 OCT 79	J. KING

DRN		FIRST USED ON
CH		DLVII-KB
ENG		TITLE
PROJ. ENG.		EIA-TO-20MA CONVERTER
PROD.		
NEXT HIGHER ASSY		
8-DD-5413679-0		
SCALE 2/1		
SHEET 1 OF 2		

digital

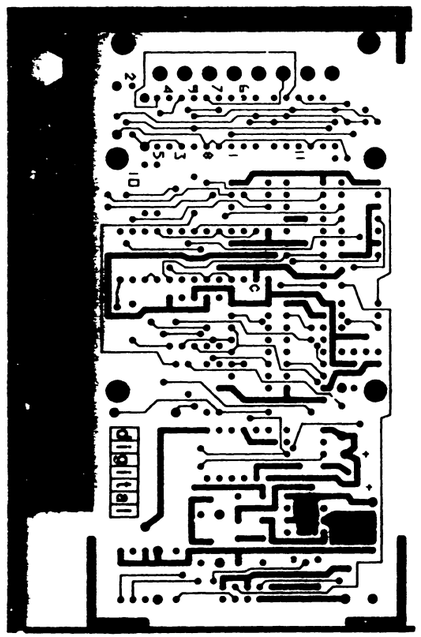
SIZE	CODE	NUMBER	REV
D	UA	5413679-0-0	D

DIST

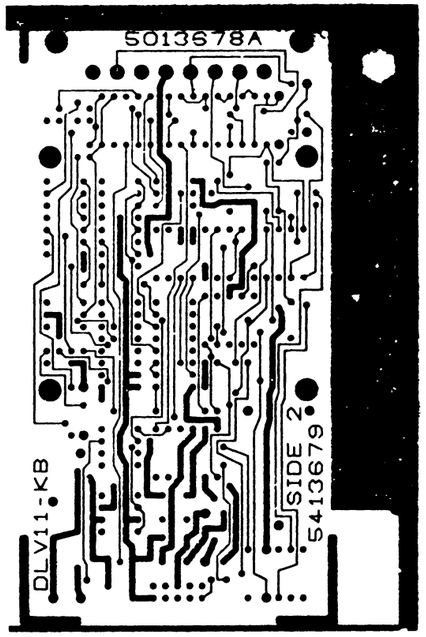
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L1

5013678A 5413679



L2



REVISIONS		
CHK	CHANG. NO	REV

TITLE	SIZE	CODE	NUMBER	REV
EIA-TO-20MA CONVERTER	D	UA	5413679-0-0	B
SCALE 2/1 SHEET 2 OF 2	DIST			

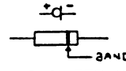
DUA5413679-0-0 B

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NOTES:
1. INSTALL C14 (DEC PN 10-12784), .047 μF ONLY WHEN CONNECTED TO ASR33 TELETYPE.
2. IC PWR AND GND PINNING

IC'S	GND	+5V	+12V	-12V
74LS02	7	14	—	—
4049	8	1	—	—
74C161	8	16	—	—
CD4520	8	16	—	—
9636	4	—	8	5

3. ON MCL1301 LOOK LIKE THIS



4. R8 IS ENGINEERING OPTIONAL COMPONENT ; NOT INSERTED.

J1 (2X5 PIN BERG)

J2 (MATE'N'LOK)

EIA IN — R1 3.0K — D1 1N750A 4.7V — 9636 E3 — R2 470 — E1 — R6 39K

EIA OUT

KEY (NO PIN)

RDR PLS H

+12V — R4 180 — W1 — W2 — CL OUT +

Q1 2N3906 — C2 680 pF — Q3 A05 — D6 IN4004 — W3 — W4 — W5 — CL OUT -

R3 180 — D5 MCL1301

R23 35.7 — Q4 2N3725 — D2 IN4370A 2.4V — -12V — D15 MCL1301

R16 180 — W6 — W7 — CL IN +

R9 220 — Q5 A05 — D8 IN4004 — R11 22 — W8 — W9 — W10 — CL IN -

+5V — E2 — R8

R22 35.7 — Q7 2N3725 — D3 IN4370A 2.4V — -12V — D16 MCL1301

R10 100 — R26 DEC 3646 — C14 .047μF — R20 1K — SEE NOTE 1 (OPTIONAL)

R21 9.1K — +5V — R15 10K — Q2 A55 — D9 IN4004 — -12V

D14 4M6.8AZ1 6.8V — +12V — +5V — C13 .22 MFD.

JUMPER CONFIGURATION	IN	OUT
PASSIVE 20MA RECEIVER	W7,W9	W6,W8,W10
ACTIVE 20MA RECEIVER	W6,W8,W10	W7,W9
PASSIVE 20MA TRANSMITTER	W2,W4	W1,W3,W5
ACTIVE 20MA TRANSMITTER	W1,W3,W5	W2,W4
110 BAUD ENABLE	W11	—
110 BAUD DISABLE	—	W11

D7 D664 — R13 22K — C1 .047μF — 4049 E4 — 74LS02 E3 — RDR +

RDR -

R17 2.2K — R18 1M — Y1 614.4KHz — C3 100pF — C9 33pF — 4049 E4 — R24 2.2K — +5V

74C161 E6 — CD4520 E7 — CLK1 — ENB1 — CLK2 — ENB2 — RES1 RES2 — W11

+12V — SIG GRD — 110 BAUD — C6 100μF — C7 .47μF

MM 4024 E8 — C8 .47μF — D10 D664 — D11 IN4732A 4.7V — D4 D664 — C12 .47μF — D13 D664 — D12 D664 — C9 .47μF — C10 .47μF — C11 15μF

REVISIONS			
DASH	CHANGE NO.	REV.	
-01	CS5413679-AB001	A	J. KING 10DEC78
-02	CS-13679-AB002	B	J. KING 4-24-79
-03	CS-13679-AB003	B	P. Montano 3-16-82
-04			J. CURTIS

DRN. S. Wilson 28-JUL-78
CHK'DR. [illegible] 28-JUL-78
ENG. [illegible] SEPT 78
PROJ. ENG. [illegible] SEPT 78
PROD. [illegible] 10/11/78
NEXT HIGHER ASSY. B-DD-5413679-0
SCALE NONE
SHEET 1 OF 1

FIRST USED ON DLV11-KB

digital

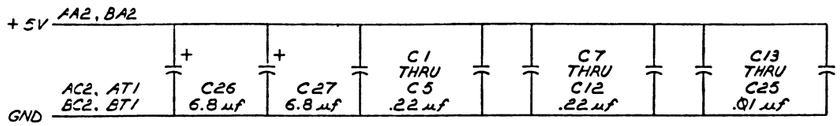
TITLE EIA-TO-20MA CONVERTER

SIZE D | CODE | NUMBER CS5413679-0-1 | REV B

DIST.

MR

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IC PIN LOCATIONS GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED BELOW		
IC TYPE	GND	+5V
I.C. DEC MM1 6330	8	16
I.C. DEC 8837	8	16
I.C. DEC 8641	8	16
I.C. DEC 8136	8	16
I.C. DEC 74175	8	16
I.C. DEC 74157	8	16
I.C. DEC 7384	1	8

NOTES:

1. THE JUMPERS ARE FACTORY SET FOR:
 ADDRESS = 16777X (ONLY W1 INSTALL).
 VECTOR = 300 (W15, 14 & 13 INSTALL).
 THE JUMPERS ARE ASSIGNED AS FOLLOWS:
 A = ADDRESS / V = VECTOR

A3 - W10	V3 - W15
A4 - W9	V4 - W14
A5 - W8	V5 - W13
A6 - W7	V6 - W12
A7 - W6	V7 - W11
A8 - W5	
A9 - W4	
A10 - W3	
A11 - W2	
A12 - W1	

JUMPER IN = LOGIC Ø.
JUMPER OUT = LOGIC 1.

REVISIONS		
ECN	CHANGE NO.	REV.
DJ	M7941-AR005	H
REVISED & REDRAWN		
J. CURTIS		
J. Curtis		J
M7941-AB069		
A. Feldman & S.L. Po		
J. CURTIS		

DRN.	5-8-75
CHK. D. Gilbert	5-1-75
ENG. J. CYR	6-12-75
PROJ. ENG. J. CYR	6-12-75
PROD. D. DE ROAE	6-12-75
NEXT HIGHER ASSY.	
D-UA-M7941-Ø-Ø	
SCALE	
SHEET 1 OF 4	

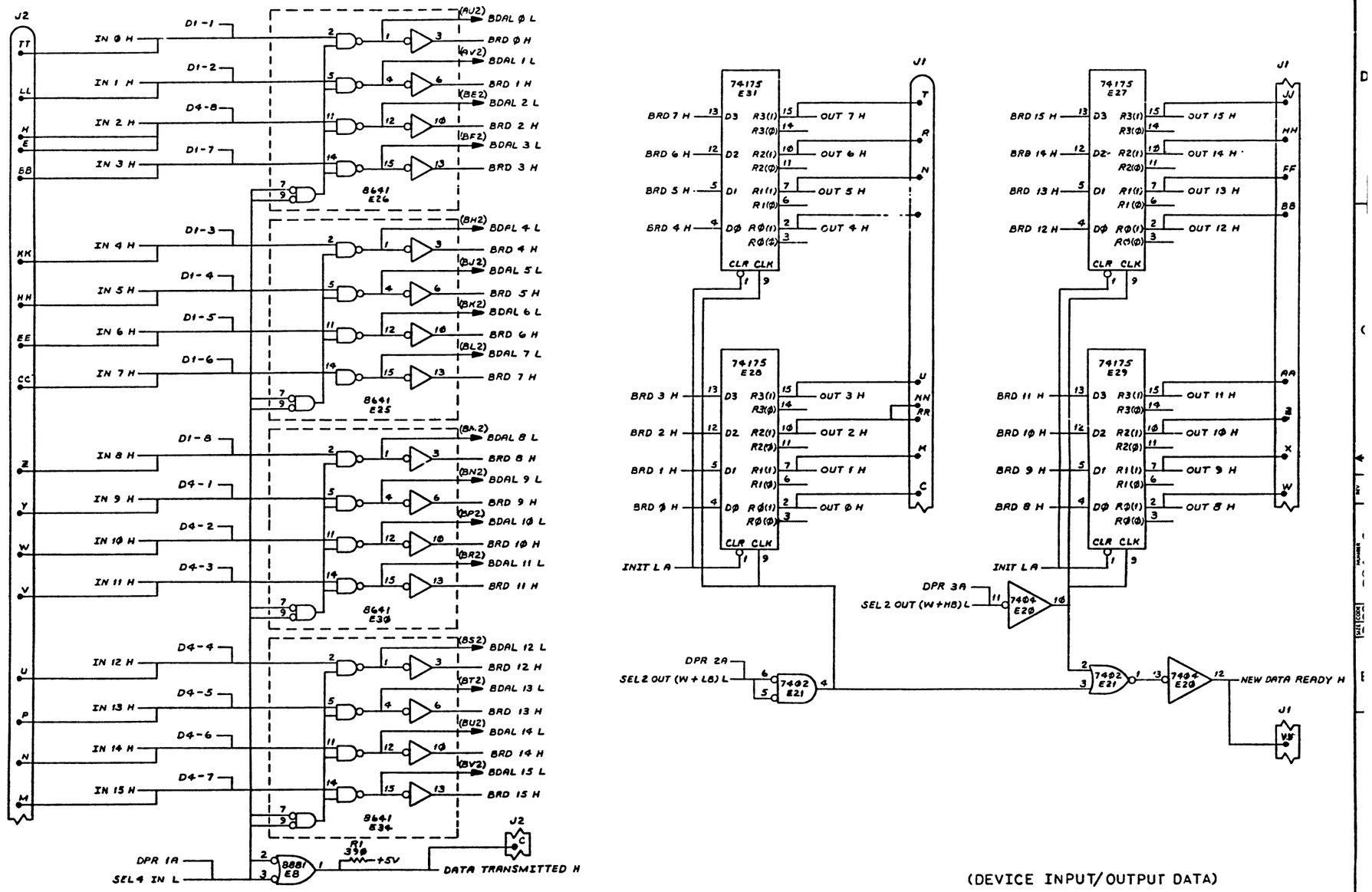
FIRST USED ON: LSI11

TITLE: PARALLEL LINE UNIT

SIZE	CODE	NUMBER	REV.
D	CS	M7941-Ø-1	J

DIST.

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(DEVICE INPUT/OUTPUT DATA)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
PARALLEL LINE UNIT	D	CS	M7941-Ø-1	J
SCALE —	SHEET 2 OF 4		DIST.	

DEC FORM NO. DRD 138

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BBS7 L (AF2) — 8837 E1

+5V — RP

BRD 12 H DPR 1B — W1 (A12)
BRD 11 H DPR 2B — W2 (A11)
BRD 10 H DPR 3B — W3 (A10)
BRD 9 H DPR 4B — W4 (A9)

8136 E12 — STB; B1 T1 B2 T2 B3 T3 B4 T4 B5 T5 B6 T6 — OUT 9 — DPR 11B

BRD 8 H DPR 5B — W5 (A8)
BRD 7 H DPR 6B — W6 (A7)
BRD 6 H DPR 7B — W7 (A6)
BRD 5 H DPR 8B — W8 (A5)
BRD 4 H DPR 9B — W9 (A4)
BRD 3 H DPR 10B — W10 (A3)

8136 E23 — STB; B1 T1 B2 T2 B3 T3 B4 T4 B5 T5 B6 T6 — OUT 9

BSYNC L (AJ2) — 8837 E1

INIT L B
BRD 2 H — A2
BRD 1 H — A1
BRD Ø H — BYTE
74175 E3

DPR 5A
BIAK I L (AM2) — 8837 E5
DIN H

+3V
7474 E10 IACK — INTEN A H
7408 E19
74H11 E11

IACK A
7474 E10 IACK — INTEN B H
8881 E8 — (AN2) DPR 6A — BIAK Ø L
74H11 E11
384 E3 — VECTOR H
VEC RQST B H
7402 E21

INIT L B
7408 E19
7474 E22 INT RQST — RQST B H
D3 D664 — +5V
J2

RQST A H
7408 E19
7474 E22 INT RQS
D2 D664 — +5V
J1

INT EN A H
INT EN B H
8881 E2 — (AL2) BIRQ L

BDIN L (AN2) — 8837 E1 — DIN H

BOUT L (AE2) — 8837 E1 — DOUT H
7402 E4
7404 E20
8837 E5
7402 E4
R3 47
8881 E8 — DPR 13A
C6 1000pf

BWTBT L (AK2) — 8837 E1

DPR 13B — 8837 E5
384 E9
DPR 12B RPLY L — 7402 E4
R2 100
8881 E2 — Ø SL1-1

MMI 6330 E13
D7 IN RPLY L
D6 SEL 4 IN L
D5 SEL 2 OUT (W+HB) L
D4 SEL 2 OUT (W+LB) L
D3 SEL 2 IN L
D2 SEL Ø OUT (W+LB) L
D1 SEL Ø IN L
D0
CE
A4 A3 A2 A1 A0

Ø SL3-1
7400 E19 — (SEL Ø + SEL 2) IN H
8837 E5 — - SEL Ø IN H
DPR 14B

VECTOR H — 8881 E2 — (AF2) BRPLY L

BINIT L (AT2) — 8837 E1 — 7404 E20 — INIT L A
INIT H
7402 E4 — INIT L B
7404 E20 — A INIT H (BERG 1) — J1
74H11 E11 — B INIT H (BERG 2) — J2

AR2 AS2

(SELECT & INTERRUPT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
PARALLEL LINE UNIT	D	CS	M7941-Ø-1	J
SCALE —	SHEET 3 OF 4	DIST.		

DEC FORM NO. DRD 12B

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74175 E7
BRD Ø H — D3 R3(1) — CSR Ø H
R3(Ø)
BRD 1 H — D2 R2(1) — CSR 1 H
R2(Ø)
BRD 5 H — D1 R1(1) — INT EN B H
R1(Ø)
BRD 6 H — DØ RØ(1) — INT EN A H
RØ(Ø)
CLR CLK
INIT L A

J2 M DD V1

DPR 7A
SEL Ø OUT (W+LB) L — 8837 E5

D1 D664: D1-1 … D1-8 — +5V
D4 D664: D4-1 … D4-8 — +5V

+5V — R4 330Ω — R5 680Ω — +3V

74157 E18
DPR 8A — W11 (V7) — B3 A3 f3
RQST A H — B2 A2 f2
DPR 9A — W12 (V6) — B1 A1 f1
DPR 10A — W13 (V5) — BØ AØ fØ
DPR 11A — W14 (V4)
STB SØ

74157 E16
DPR 12A — W15 (V3)
IACK A
VECTOR H

74157 E35
OUT 7 H — B3 A3 f3
OUT 6 H — B2 A2 f2
OUT 5 H — B1 A1 f1
OUT 4 H — BØ AØ fØ
STB SØ

74157 E17
OUT 3 H — B3 A3 f3
OUT 2 H — B2 A2 f2
OUT 1 H — B1 A1 f1
OUT Ø H — BØ AØ fØ
STB SØ

DPR 14A
SEL 2 IN L — 7404 E28

384 E9 — (SEL Ø·f SEL 2) IN H
384 E9 — VECTOR H

RQST B H — 8881 E8 — BV2 — BDAL 15 L
SEL Ø IN H
OUT 15 H — 8881 E32 — BU2 — BDAL 14 L
OUT 14 H — 8881 E32 — BT2 — BDAL 13 L
OUT 13 H — 8881 E32 — BS2 — BDAL 12 L
OUT 12 H — 8881 E32 — BR2 — BDAL 11 L
OUT 11 H — 8881 E24 — BP2 — BDAL 10 L
OUT 10 H — 8881 E24 — BN2 — BDAL 9 L
OUT 9 H — 8881 E24 — BM2 — BDAL 8 L
OUT 8 H — 8881 E24 — BL2 — BDAL 7 L
OUT 7 H — 8881 E33 — BK2 — BDAL 6 L
OUT 6 H — 8881 E33 — BJ2 — BDAL 5 L
OUT 5 H — 8881 E33 — BH2 — BDAL 4 L
OUT 4 H — 8881 E33 — BF2 — BDAL 3 L
OUT 3 H — 8881 E14 — BE2 — BDAL 2 L
OUT 2 H — 8881 E14 — AV2 — BDAL 1 L
OUT 1 H — 8881 E14 — AU2 — BDAL Ø L
OUT Ø H

E16: DPR 14A … DPR 1A — 33Ø 68Ø — +5V
E13: DPR 14B … DPR 1B — 33Ø 68Ø — +5V
DPR 4A (NO CONN.)

(BUS DATA IN LOGIC)

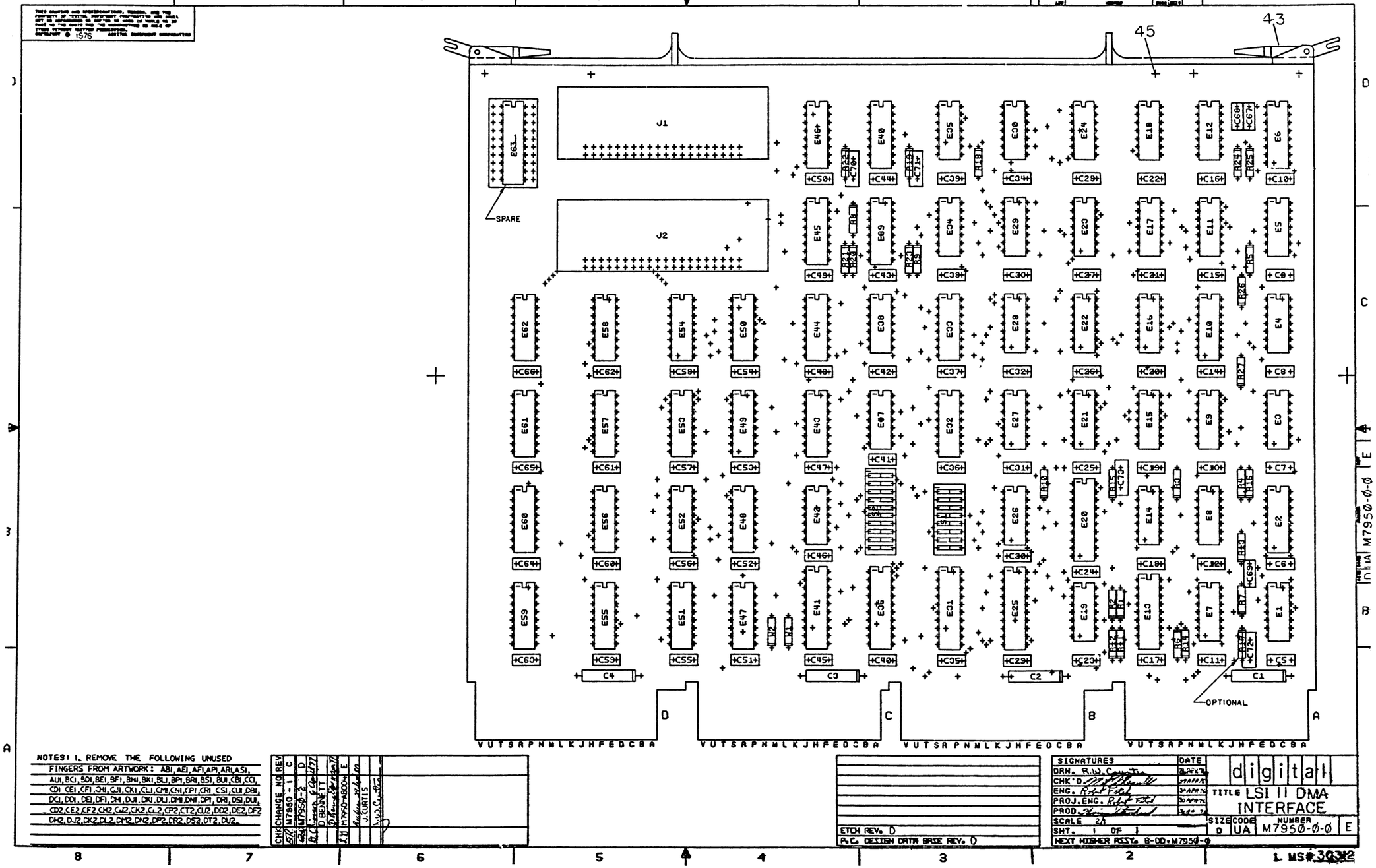
REVISIONS
CHK | CHANGE NO. | REV

TITLE PARALLEL LINE UNIT
SIZE D CODE CS NUMBER M7941-Ø-1 REV J
SCALE —//— SHEET 4 OF 4 DIST

DEC FORM NO. 3RD 135

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D UA M7950-0-0 E



NOTES: 1. REMOVE THE FOLLOWING UNUSED FINGERS FROM ARTWORK: AB1, AE1, AF1, AP1, AR1, AS1, AU1, BC1, BD1, BE1, BF1, BH1, BK1, BL1, BP1, BR1, BS1, BU1, CB1, CC1, CD1, CE1, CF1, CH1, CJ1, CK1, CL1, CM1, CN1, CP1, CR1, CS1, CU1, DB1, DC1, DD1, DE1, DF1, DH1, DJ1, DK1, DL1, DM1, DN1, DP1, DR1, DS1, DU1, CD2, CE2, CF2, CH2, CJ2, CK2, CL2, CP2, CT2, CU2, DD2, DE2, DF2 DH2, DJ2, DK2, DL2, DM2, DN2, DP2, DR2, DS2, DT2, DU2.

CHK	CHANGE NO	REV
	M7950-1	C
	M7950-2	D
D BENNETT		
J CURTIS	M7950-ABOOK	E

ETCH REV. D
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE
DRN. R.W.	
CHK'D	
ENG.	
PROJ. ENG.	
PROD.	
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-00: M7950-0	

digital

TITLE LSI 11 DMA INTERFACE

SIZE	CODE	NUMBER	
D	UA	M7950-0-0	E

1. MS#30342

M7950-0-0 E

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S1 VECTOR
S2 ADDRESS

BDAL 15 L … BDAL 14 L → BUS 3 … BUS Ø, DAT 3 … DAT Ø → DI DA 15 H … DI DA 14 H; DC ØØ3 E41; S2; +5V; JA 3 … JA 1, MEN B, JV 3 … JV 1, MATCH, XMIT, REC

BDAL 1Ø L … BDAL 13 L → BUS 3 … BUS Ø, DAT 3 … DAT Ø → DI DA 1Ø H … DI DA 13 H; DC ØØ3 E36; S2; JA 3 … JA 1, MEN B, JV 3 … JV 1, MATCH, XMIT, REC; S1

D4 XMIT ENB H; D4 REC ENB H

BDAL Ø7 L … BDAL ØØ L → BUS 3 … BUS Ø, DAT 3 … DAT Ø → DI DA Ø7 H … DI DA ØØ H; DC ØØ3 E31; S2; JA 3 … JA 1, MEN B, JV 3 … JV 1, MATCH, XMIT, REC; S1

D4 XMIT ENB H; D4 REC ENB H

BDAL Ø4 L … BDAL Ø1 L → BUS 3 … BUS Ø, DAT 3 … DAT Ø → DI DA Ø4 H … DI DA Ø1 H; DC ØØ3 E25; S2; +5V; BBST L; JA 3 … JA 1, MEN B, JV 3 … JV 1, MATCH, XMIT, REC; S1

D4 XMIT ENB H; D4 REC ENB H

+5V; R1 18Ø; R11 39Ø

DS READY(1) H; DI DA Ø6 H; DS CLK CSR LOW H; DI DIN L; BIAKI L; BINIT L; BDIN; DC ØØ3 E13; R@STA, A DATA, A CLK, BIAKI, BINIT, BDIN, B CLK, B DATA, R@STB, AST, BIRQ, BIAKO, INITO, VECTOR, VEC B, BST

+5V; R2 18Ø; R12 39Ø

DI IE (1) H; AL2 → BIRQ L; AN2 → BIAKO L; DI INIT H; DI INIT L

NOTES:
1. UNLESS OTHERWISE SPECIFIED THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
14 PIN DIP	14	7
16 PIN DIP	16	8
DC ØØ3	9	Ø
DC ØØ4	12	6
DC ØØ5	13	7

+5V; R15 82Ø; C73 18Ø pf; +5V; R3 27Ø

DL SYNC L; DI DA Ø2 H; DI DA Ø1 H; DI DA ØØ H; BWTBT L; BO OUT L; DI DIN L → DC ØØ4 E2Ø, ENEH, RXCX, B SYNC L, BRPLY L, SEL GL, BDAL 2 L, BDAL 1 L, BDAL Ø L, BWTBT L, BO OUT L, BDIN L, OUT HB, OUT LB, VECTOR H, INMD; DI SEL Ø L … DI SEL 6 L; DI OUT LB L; DI OUT HB L; DI INWD L; DI SRPLY H; DI SRPLY L; 7404 E8

R1Ø 27Ø → +5V

D4 SYNC(1) H; D4 DIN(1) H; DI SRPLY H → B641 E2 → A J2 B SYNC L; DI SYNC H; A H2 BDIN L; DI DIN H; A F2 BRPLY L; DI RPLY H; A R2 BDMGI L; DI DMGI H; 7404 E8; DI SYNC L; DI DIN L; DI RPLY L

R+ 18Ø; R13 39Ø; +5V

AA2, BA2, CA2, DA2; +5V; C1 THRU C4 6.8 µf; C5 THRU C66 .Ø1 µf

AC2, BC2, AJ1, BJ1, AM1, BM1, AT1, BT1, CT1, DT1

DI

DRN.		● FEB 76	FIRST USED ON: DRVII-B
CHK'D		30 APR 76	digital
ENG.		30 APR 76	TITLE: LSI-11 DMA INTERFACE
PROJ. ENG.		30 APR 76	
PROD.			
NEXT HIGHER ASSY			
8-DD-M795Ø-Ø-			SIZE C, CODE DCS, NUMBER M795Ø-Ø-1, REV. C
SCALE NONE			
SHEET 1 OF 6			D

REVISIONS			
ZONE	CHANGE NO.	REV.	
	ORIGINAL	C	
	MYKO AROON		
	J. CURTIS		

DRD 1000

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BUS ADDRESS

WORD COUNT

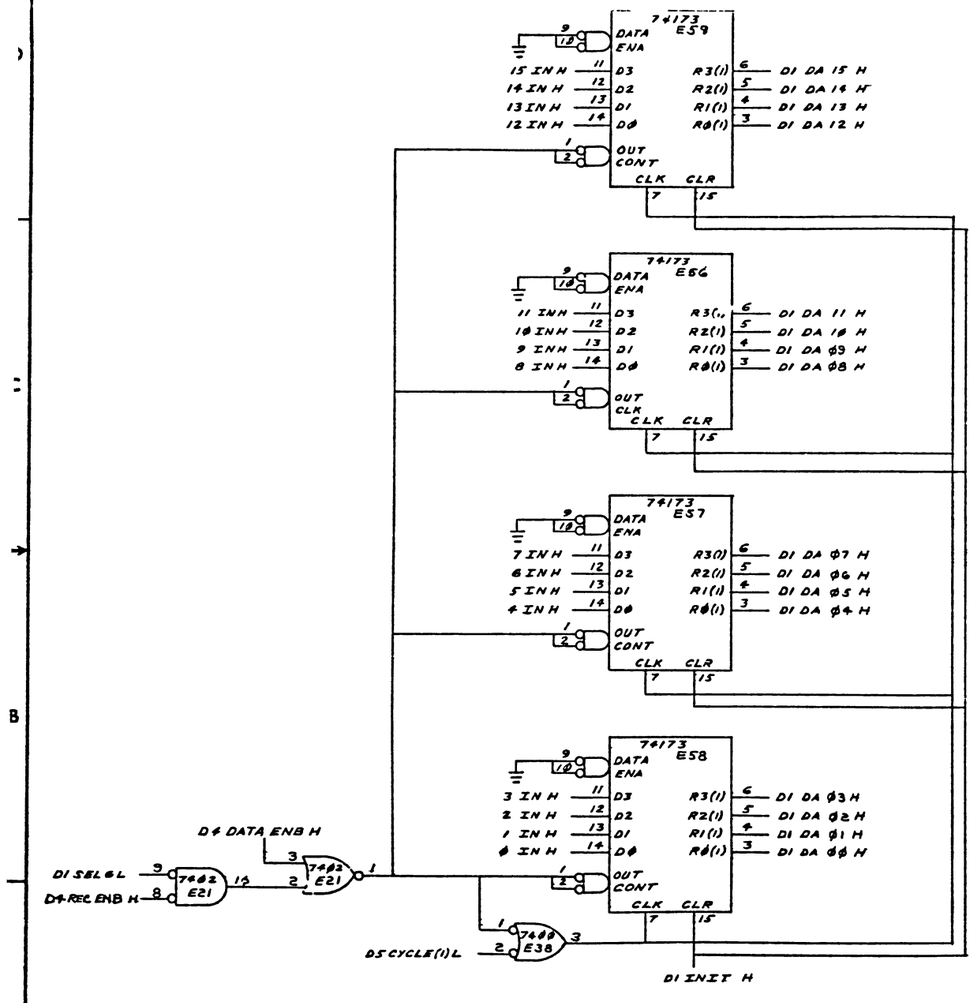
BAR WCR

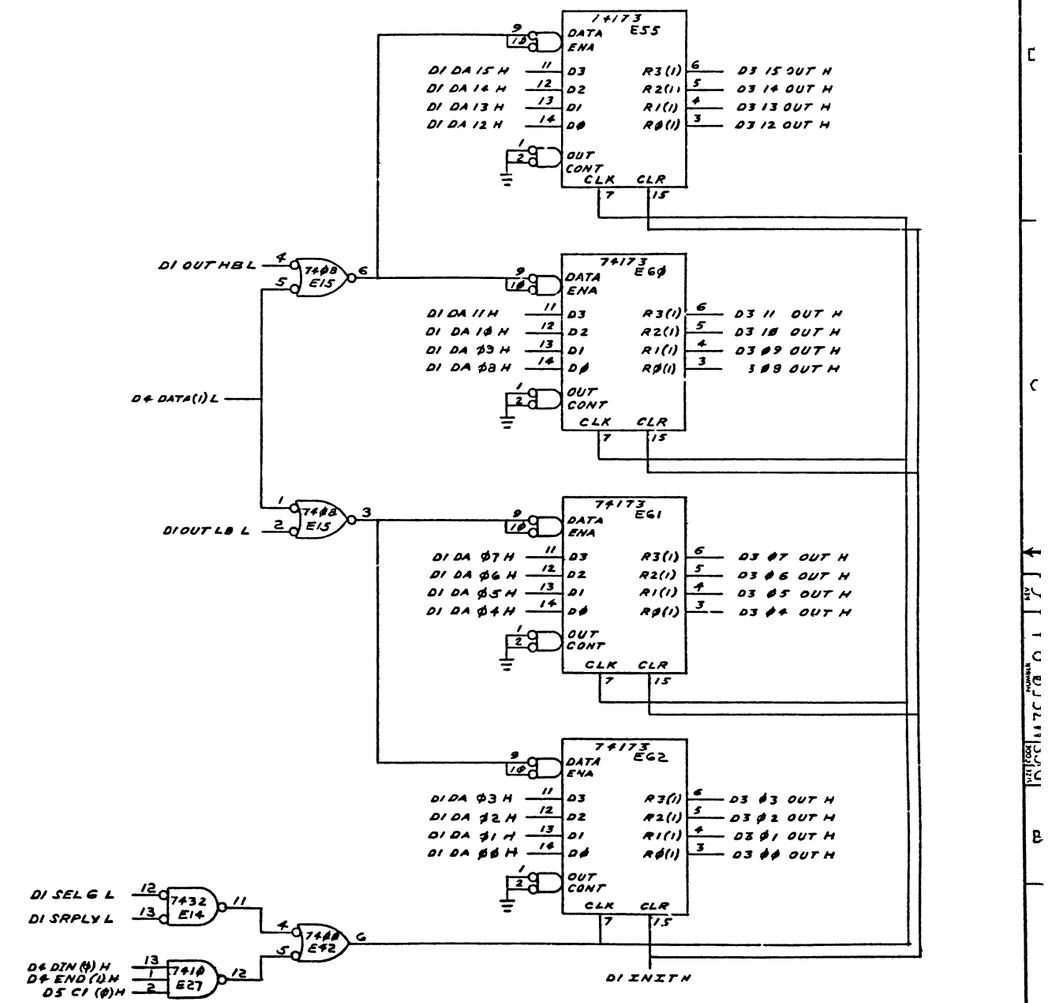
REVISIONS		
CHK	CHANGE NO	REV
	ORIGINAL	B

TITLE LSI-11 DMA INTERFACE			SIZE C	CODE LCSM7950-0-1	REV C
SCALE NONE	SHEET 2 OF 6		DIST.		

D2

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REVISIONS		
CHK	CHANGE NO.	REV
	ORIGINAL	B

DBR IN & OUT

D3

TITLE	LSI-11 DMA INTERFACE				
SIZE	CODE	NUMBER	REV.		
D	CS	M7950-0-1	C		
SCALE	NONE	SHEET 3 OF 6	DIST.		

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D5 DMA REQ H
D4 +3V H
8881 E7 → ANI → BDMR L
8881 E13 → BNI → B SACK L
TAKE GRANT 74S74 E23
SACK 74S74 E16
D4 SACK(Ø) H
D4 SACK(1) L
D1 INIT L
D4 CLR SACK L
+5V
RG 180
AS2
BDMG O L
D1 DMG I H
74132 E1
7404 E8
R16 820
CG9 180 PF
≥ 75 n s
R25 47K
CG7 100 PF
74123 E6
1545
D4 DAT IO (1) H
D4 END CYCLE L
D4 DAT IO(Ø) L
D5 SC (1) L
7427 E24
D5 READY(1) H
7450 E17
D4 CLR SACK L
DATIO 74S74 E23
D5 C Ø (1) H
D4 DIN (Ø) H
D4 DAT IO (Ø) L
D4 DAT IO (Ø) H
D1 INIT L
D4 NEX (1) L
7437 E23
7402 E18
D4 DOUT(1) H
D4 MASTER (1) L
D4 DATA (1) H
D5 C.I. (1) L
R24 47K
CG8 100 PF
MASTER 74S74 E12
SYNC 74S74 E11
DATA 74S74 E12
D4 SYNC(1) H
D4 DATA(1) L
D4 DATA ENB H
D4 CLK (1) H
D4 CLK (Ø) H
D4 MASTER (Ø) H
D4 ADDR ENB H
D4 SACK (1) L
D1 ~ RPLY L
D1 ~ SYNC L
D4 EN. CYCLE L
D4 DAT IO (Ø) L
D4 CLR CONTROL L
D4 CLK READY H
D4 SYNC(Ø) H
D4 CLR CONTROL L
D4 CLK (Ø) H
D4 DIN (1) H
D4 CLK IN H
D4 MASTER (Ø) H
D4 SYNC (Ø) H
D4 DIN (1) L
D4 DOUT (1) L
D4 DIN (Ø) L
D4 DOUT (Ø) L
D5 CYCLE (Ø) L
D4 DLY (Ø) L
D4 RUN L
D4 CLK OUT H
D4 END (1) H
D4 DLY (1) H
D4 DLY (Ø) L
D4 DLY (Ø) H
D4 DOUT(1) H
D4 SACK (Ø) H
D4 DLY (Ø) H
D1 ~ IN WD H
D4 DATA (1) H
D5 C1 (Ø) H
D1 ~ RPLY L
D5 C1 (Ø) L
D4 CLK (1) H
D4 SYNC (1) H
D4 DIN (1) H
D4 DIN (Ø) H
D4 CLK (Ø) H
D4 DOUT (1) H
D4 DOUT (Ø) L
D4 DATA ENB H
D4 END CYCLE H
D4 END CYCLE L
D4 RECENB H
D4 XMIT ENB H
D1 RPLY L
D4 NEX (1) H
D4 NEX (1) L
D1 DA 14 H
D5 LOAD CSR HIGH L
D1 INIT H
D4 +3V H
R5 270
R26 390
R27 820
RIT (OPTIONAL)
RT 270
C72 180 PF
110 n s
IAK
DMG

REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

BUS MASTER D4

TITLE LSI-11 DMA INTERFACE
SIZE D DCS M7950-0-1 REV. C
SCALE NONE SHEET 4 OF 6 DIST.

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D6 C1 H
DI INIT L
D6 CØ H
D6 AØØ H
D6 SINGLE CYCLE H
D5 CYCLE (1) L
D2 ADDR ENB L
D6 ATTN H
D4 CLR CONTROL L
D2 WCOFLO L
B POK H
D4 CLK READY H
DI DA ØØ H
D5 LOAD CSR LOW H
D6 WC INC ENB H
D5 CLK CSR HIGH H
DI DA 12 H
DI DA Ø8 H
D6 CYCLE REQUEST H
D5 LOAD CSR HIGH L
D6 BA INC ENB H
D4 DLY (1) H
DI INIT H
D4 +3V H
DI SEL 4 L
D4 REC ENB H
DI OUTHB L
DI CUT LB L
DI SPPLY L
INIT L
DI INIT H
D4 RUN L
D5 READY (1) H
D5 MAINT (1) L
D5 READ CSR L
DI DA Ø2 H
DI DA 11 H
D5 STATUS A H
D5 STATUS B H
D5 STATUS C H
D5 CYCLE (1) H
DI IE (1) H
D5 DMA REQ H
D5 CYCLE (Ø) L
D5 CLK CSR LOW L
D4 END CYCLE L
D5 LOAD CSR LOW L

D5 C1 (1) H
D5 C1 (1) L
D5 C1 (Ø) L
D5 C1 (Ø) H
D5 CØ (1) H
D5 CØ (1) L
D5 AØØ (1) H
D5 SC (1) L
D5 WC INC ENB L
D5 BA INC ENB L
D5 MAINT (1) H
D5 READY (1) H
D5 MAINT (1) L
D5 CYCLE (1) H
D5 CYCLE (Ø) L
D5 DMA REQ H
D5 LOAD CSR HIGH H
D5 LOAD CSR LOW L
D5 LOAD CSR LOW H
D5 CLK CSR LOW H
D5 CLK CSR LOW L
D5 INIT V2 H
D5 INIT H
D5 BUSY H
D5 READY H
D5 FNCT 3 H
D5 FNCT 2 H
D5 FNCT 1 H

DI DA Ø5 H
DI DA 14 H
DI DA 13 H
DI DA 12 H
DI DA Ø9 H
DI DA Ø8 H
DI DA Ø7 H
DI DA Ø6 H
DI DA Ø4 H
DI DA 1Ø H

R19 3.3K
R20 3.3K
R8 180
C70 560 PF
R22 3.3K
R23 3.3K
R9 330
C71 56ØPF
R21 3.3K

8837 E48
7437 E23
7437 E34
7402 E29
74175 E33
74175 E39
74175 E38
7474 E28
7400 E36
7427 E27
7404 E35
7402 E22
8097 E45
8097 E33
8097 E54
8097 E56
7432 E26
7432 E14
7432 E23
7402 E35
7402 E29
7404 E34
8097 E44
8097 E46
8097 E58
8556 E44
7400 E42

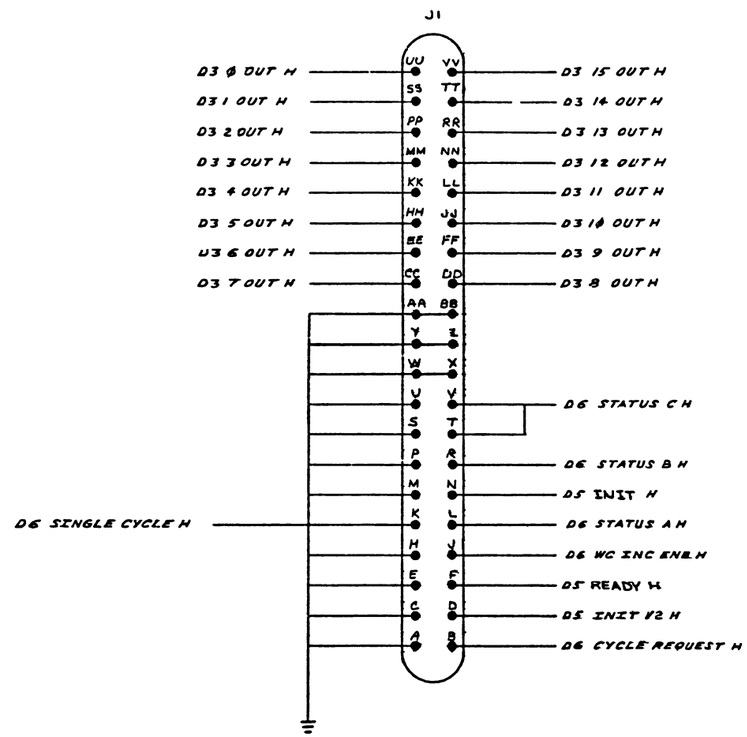
I/O SIGNALS

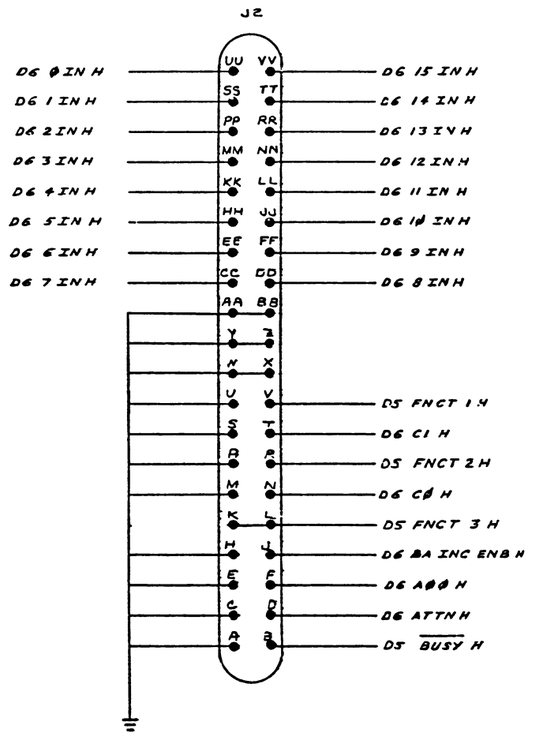
REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

TITLE	SIZE	CODE	NUMBER	REV.
LSI-11 DMA INTERFACE	C	CS	M7950-0-1	C
SCALE NONE	SHEET 5 OF 6	DIST.		

D5

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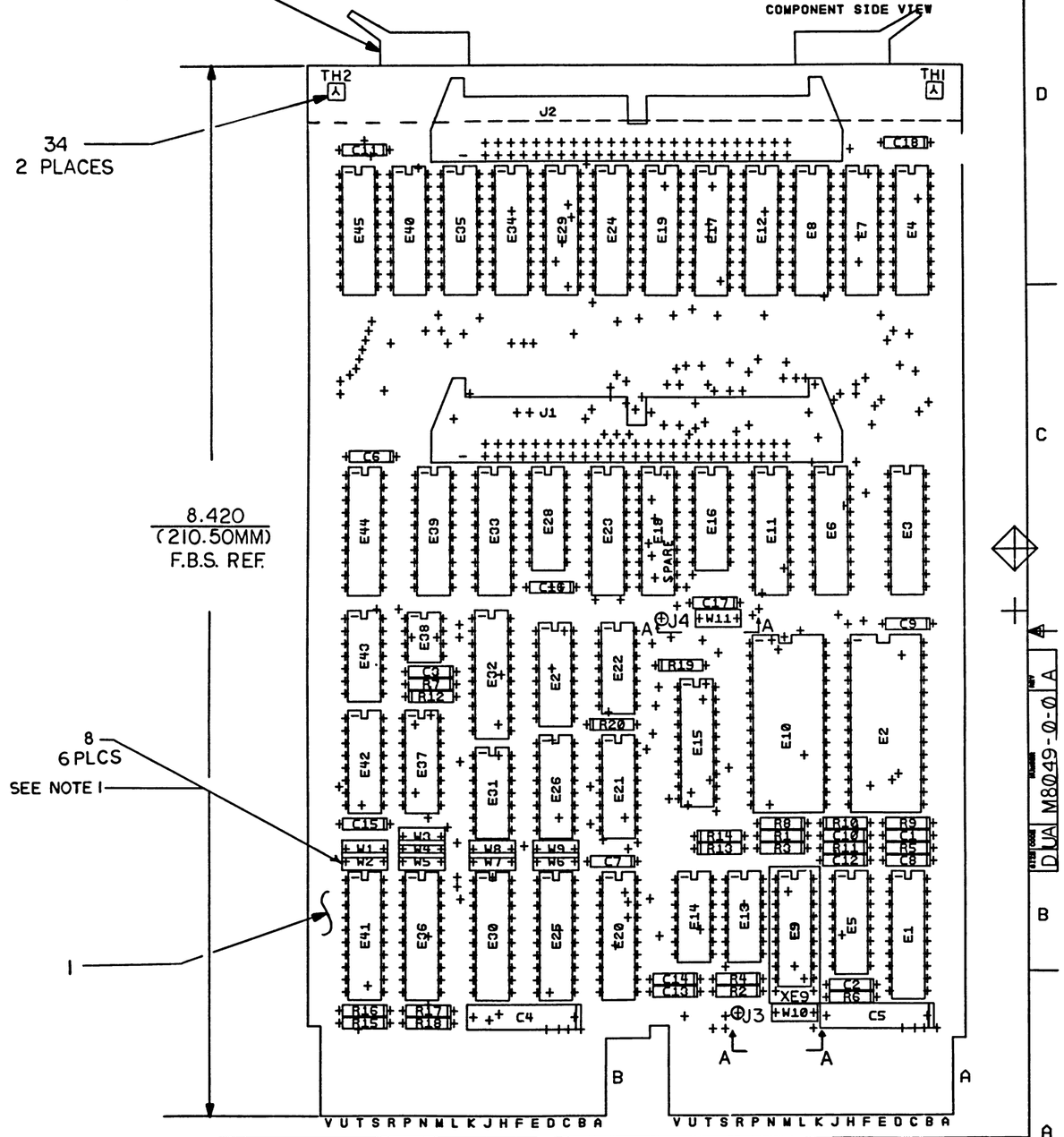
REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

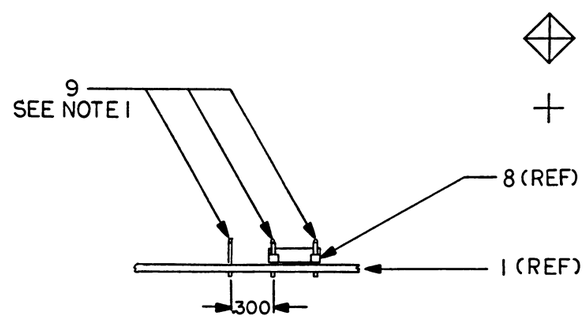
PIN ASSIGNMENT D6

TITLE LSI-11 DMA INTERFACE			SIZE D	CODE CS
SCALE NONE	SHEET 6 OF 6	DIST	NUMBER M7950-0-1	REV. C

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COMPONENT SIDE VIEW





VIEW A-A

NOTES:
1. ITEM#8 (W2, W7-W11) MOUNT ON ITEM#9 (STRIP CONNECTOR POSTS) #9 IN VIEW A-A ARE SINGLE ELEMENTS OF ITEM#9 TO BE MOUNTED AS SHOWN

STEP E	↑ Y AXIS ____ STEP — TIMES	
REPEAT	→ X AXIS .5 250 STEP 1 TIMES	

CHK	CHANGE NO	REV

ETCH REV. B

SIGNATURES	DATE
DRN. Mary Bassa	6/14/79
CHK'D	6-28-79
MECH.ENG. Richard Hallman	7-26-79
PROJ.ENG. Richard Hallman	7-26-79
PROD.	8-7-79

digital

TITLE: DRVII J

SCALE 2 1 | SIZE D | CODE UA | NUMBER M8049-0-0 | REV A

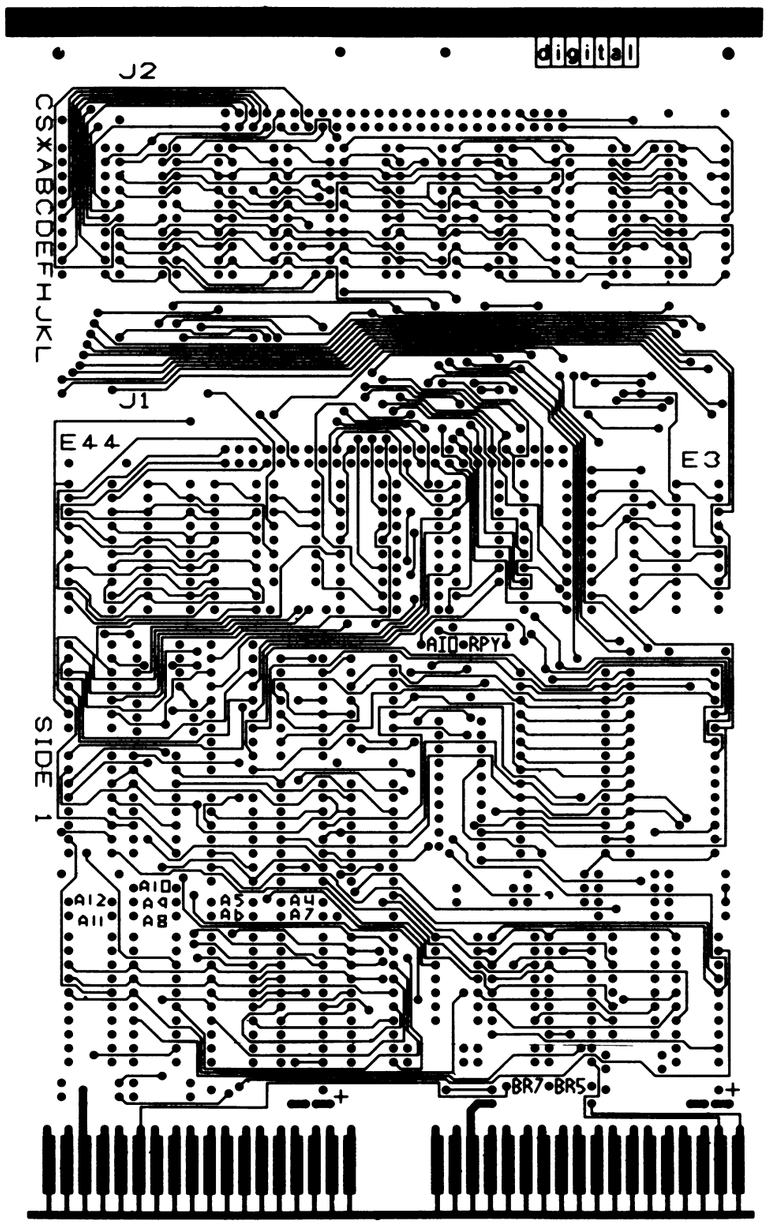
SHT. 1 OF 5

NEXT HIGHER ASSY. B-DD-M8049-0

MS# 30-12868

D UA M8049-0-0 A

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
DRV 11 - J	D	UA	M8049-0-0	A
SCALE 2/1 SHEET 2 OF 5	DIST			

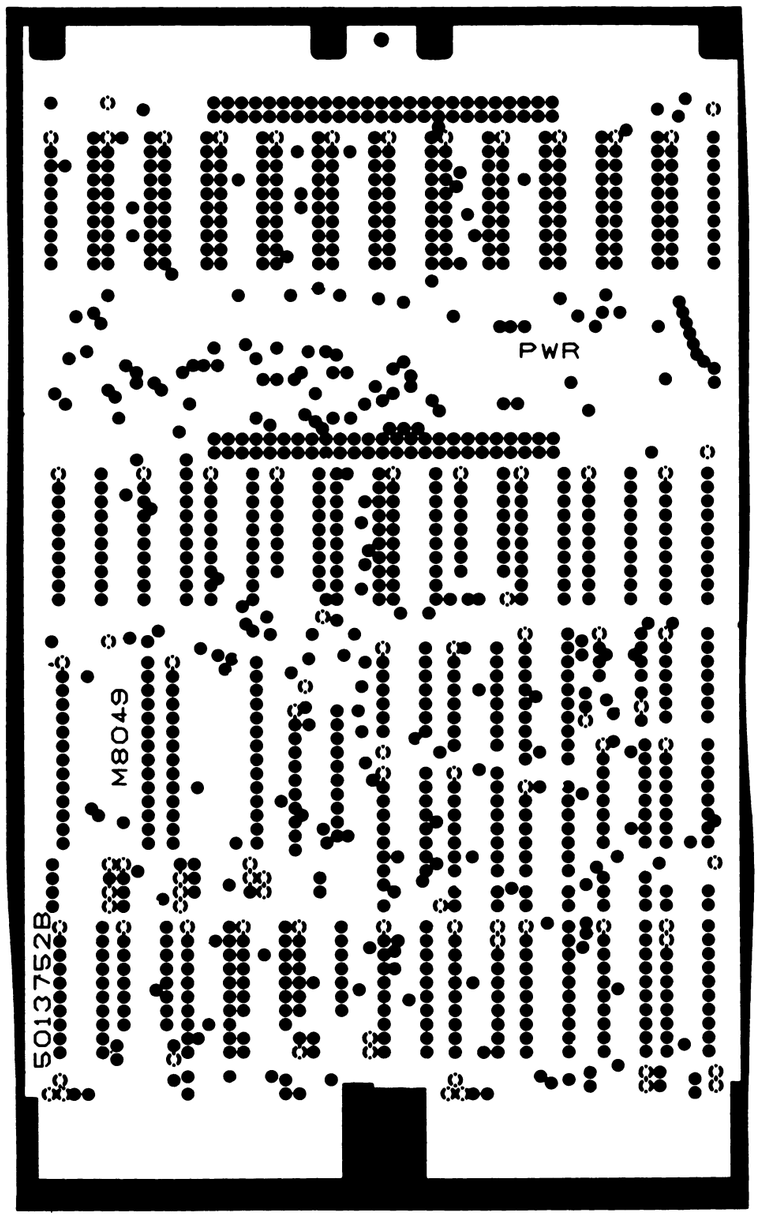
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
DRV 11-J	D	UA	M8049-0-0	A
SCALE 2/1 SHEET 3 OF 5	DIST			

SIZE D CODE UA NUMBER M8049-0-0 REV A

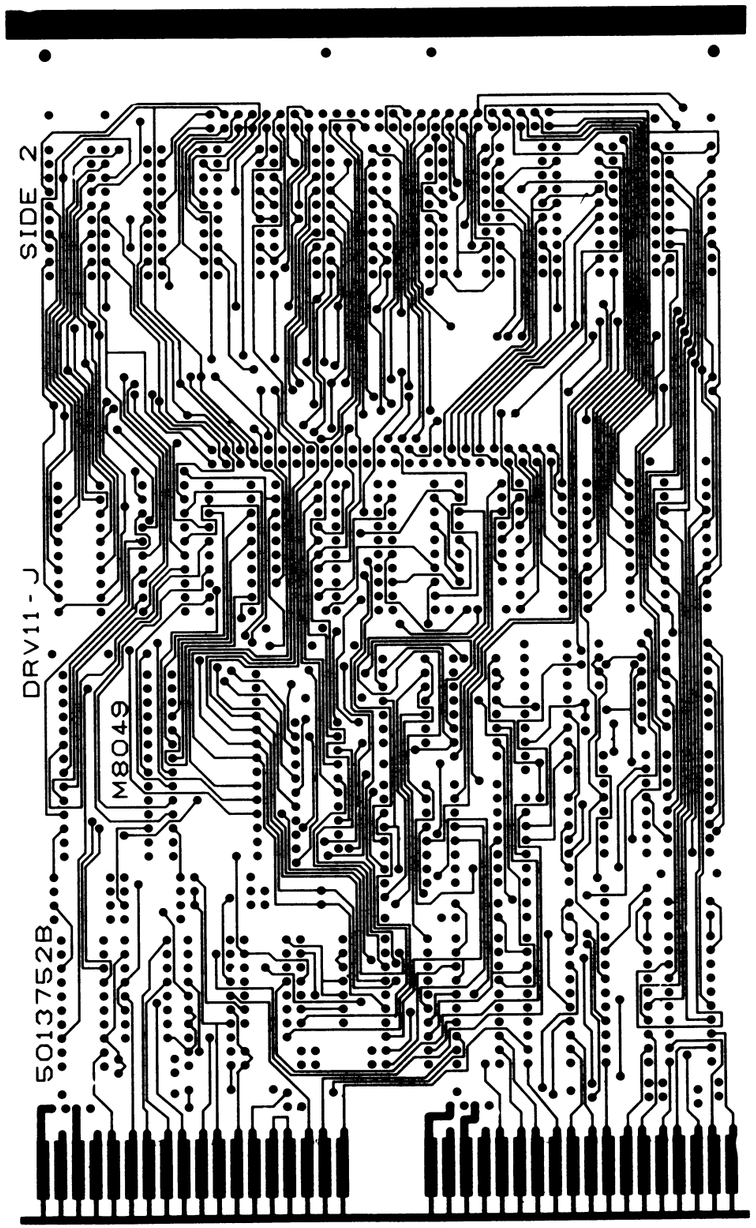
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
DRV 11 - J	D	UA	M8049-0-0	A
SCALE 2/1 SHEET 4 OF 5	DIST			

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
DRV11-J	D	UA	M8049-0-0	A
SCALE 2/1	SHEET 5 OF 5	DIST		

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BDAL 15 L
BDAL 12 L
BDAL 11 L
BDAL 14 L
BV2 BS2 BR2 BU2
BUS 3 BUS 2 BUS 1 BUS 0
DAT 3 DAT 0 DAT 2 DAT 1
DC005 E41
+5V
W1 A12
W2 A11
JA3 JA2 JA1 MEN B JAV 3 JAV 2 JAV 1
MATCH
D4 CSR15
XMIT REC
D3 XHB
D4 XMIT (1) L
DI TSD15 DI TSD14 DI TSD13 DI TSD12 DI TSD11 DI TSD10 DI TSD9 DI TSD8
74LS374 E44
D3 D2 D1 D0 D4 D7 D6 D5 OC CLK
R3(1) R2(1) R1(1) R0(1) R4(1) R7(1) R6(1) R5(1)
D6 BXMIT L
D4 WRT DBB
J1
B I/O 15 B I/O 14 B I/O 13 B I/O 12 B I/O 11 B I/O 10 B I/O 9 B I/O 8
74LS244 E33
DB1 DB2 DB3 DA1 DA4 DB4 DA2 DA3 OC1 OC2
YB1 YB2 YB3 YA1 YA4 YB4 YA2 YA3
D3 RD B L

BDAL 10 L
BDAL 9 L
BDAL 8 L
BDAL 13 L
BP2 BN2 BM2 BT2
DC005 E36
W3 A10
W4 A9
W5 A8
D5 V9
D5 V8
R16 18K
R15 18K
R14 18K
R17 18K
+5V

BDAL 7 L
BDAL 6 L
BDAL 5 L
BDAL 1 L
BL2 BK2 BJ2 AV2
DC005 E30
W6 A7
W7 A6
W8 A5
D5 V7
D5 V6
D5 V5
R13 18K
R19 18K
R20 18K
R18 18K
+5V
D3 XLB

BDAL 4 L
BDAL 3 L
BDAL 2 L
BDAL 0 L
BH2 BF2 BE2 AU2
DC005 E25
W9 A4
+5V
BBS7 L
AP2
D5 V4
D5 V3
D5 V2
DI MATCH H

74LS374 E35
D0 D7 DI D6 D3 D5 D2 D4 OC CLK
R0 (1) R7 (1) R1 (1) R6 (1) R3 (1) R5 (1) R2 (1) R4 (1)
J1
B I/O 7 B I/O 6 B I/O 5 B I/O 4 B I/O 3 B I/O 2 B I/O 1 B I/O 0
74LS244 E34
DA1 DB4 DB3 DA2 DB1 DA3 DB2 DA4 OC1 OC2
YA1 YB4 YB3 YA2 YB1 YA3 YB2 YA4
D3 RD B L

AR2 BDMGI L
AS2 BDMGO L

NOTE
1. OPTIONAL INSTALLATION OF W10 AND W11 IS BETWEEN J3 AND W10 GND TERMINAL AND J4 AND W11 GND TERMINAL.

REVISIONS			
CHK	CHANGE NO.	REV.	
[illegible]	M8049 - ML0101	B	12-Feb
	M8049-ML0087	C	30 NOV 78
	511 Control		

R. HULTMAN

DRN	[illegible]	3 JAN 79
CHK'D	[illegible]	3 JAN 79
ENG.	[illegible]	[illegible]
PROJ. ENG.	[illegible]	[illegible]
PROD.	[illegible]	2-2-79
NEXT HIGHER ASSY.		
B-DD-M8049-0		
SCALE		
SHEET 1 OF 6		

FIRST USED ON 11-03

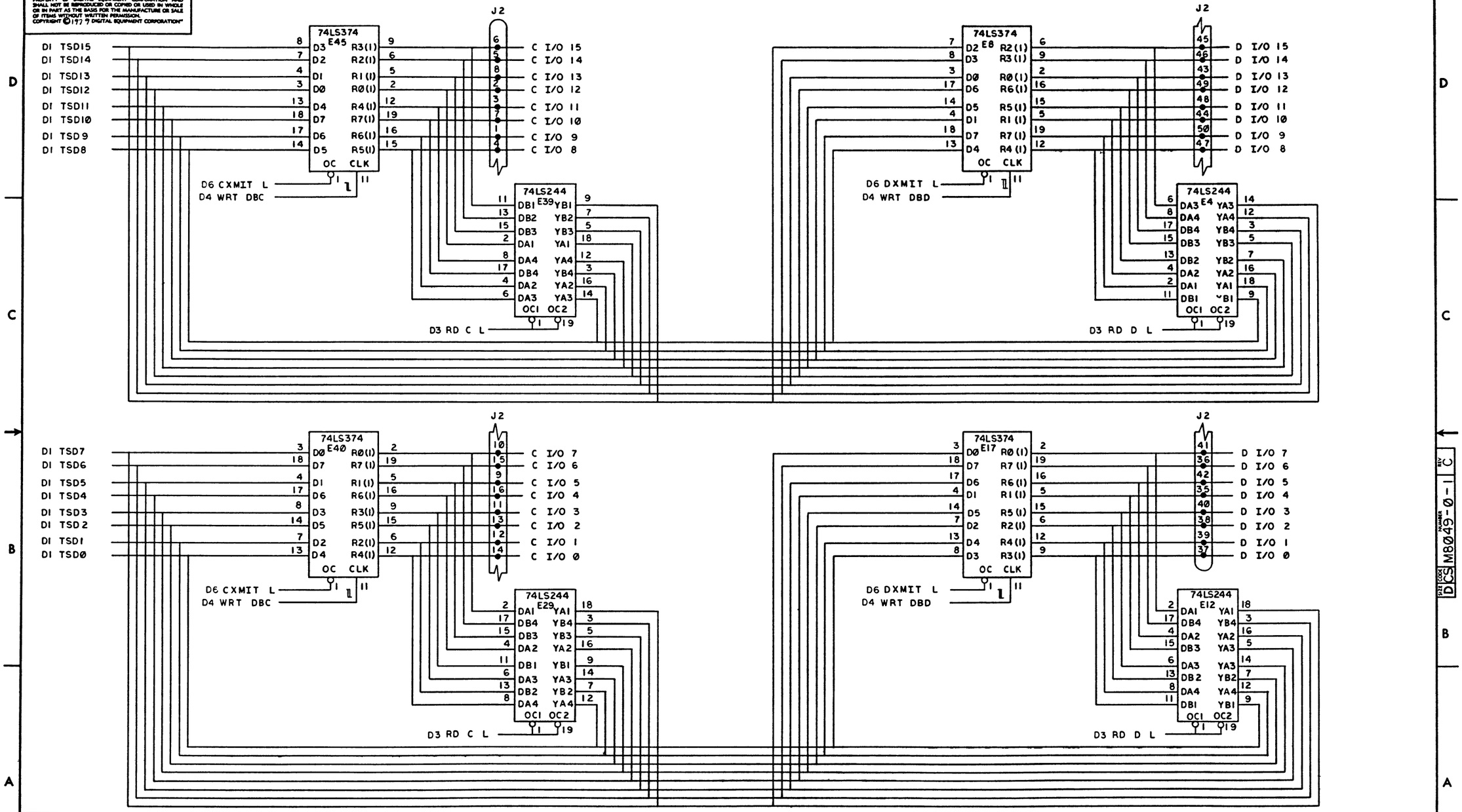
digital

TITLE
DRVII-J
(D1)

SIZE	CODE	NUMBER	REV.
D	CS	M8049-0-1	C

DIST.

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
DRV11 – J (D2)	D	CS	M8049-0-1	C
SCALE — SHEET 2 OF 6	DIST.			

DEC FORM NO. DRD 138

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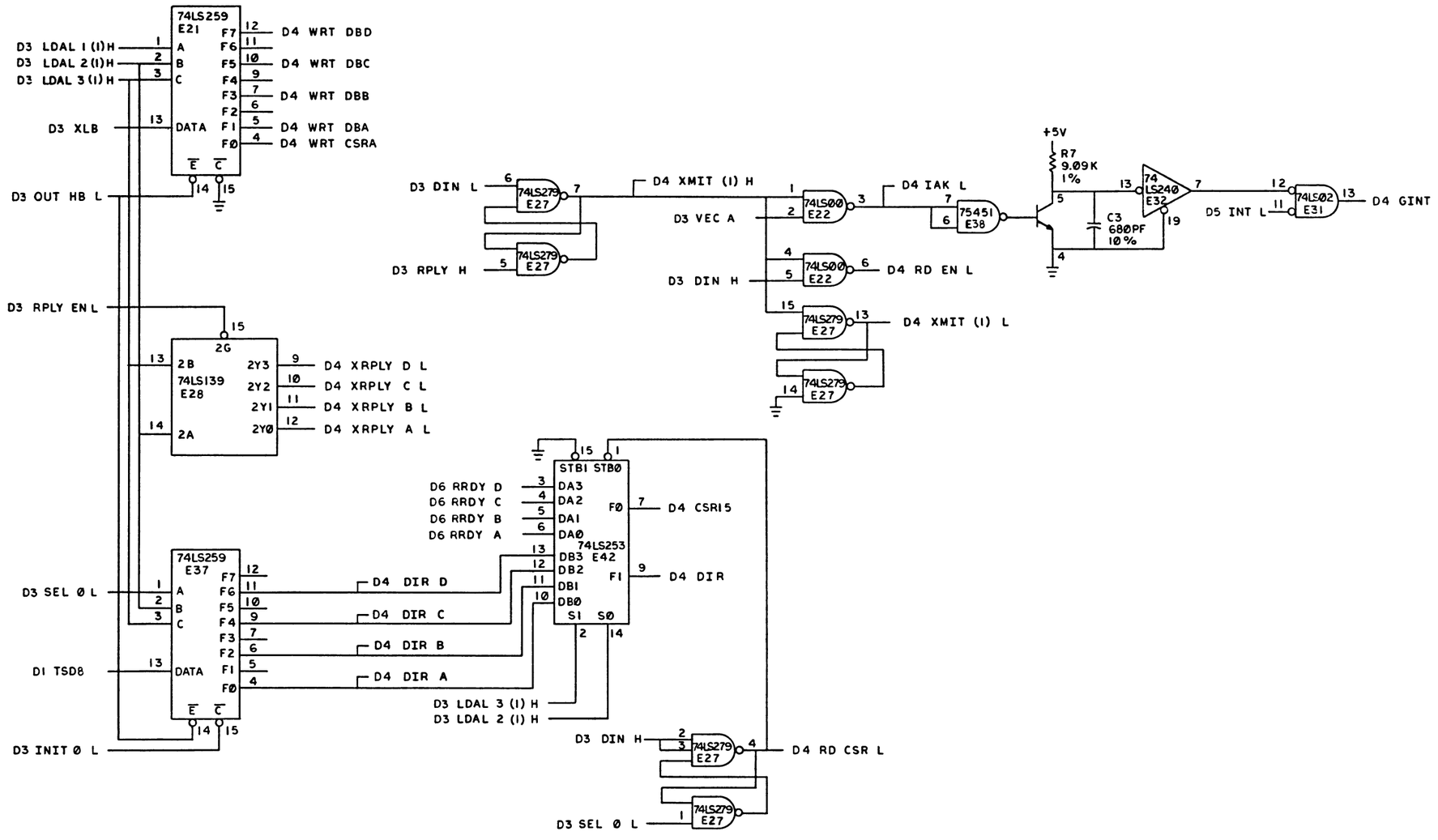
C1 220 PF
R5 4.64K,1%
+5V
DI MATCH H
DC004 E4
ENB
RXCX
VEC A
VECTOR
BRPLY
BWTBT L
AK2
WTBT EI
SEL 6
D3 SEL Ø L
BDOUT L
AE2
DOUT
SEL 4
D3 SEL 2 L
DIN
SEL 2
SEL Ø
SYNC
DI TSDØ
DAL Ø
OUT HB
D3 OUT LB L
DAL 2
OUT LB
D3 OUT HB L
DAL 1
INWD
R6 4.64K 1%
C2 220PF
+5V
8641 E5
D3 RPLY H
AF2
BRPLY L
D3 RPLY H
D5 PAUSE
74LS175 E26
DØ
RØ(I)
RØ(Ø)
DI TSDI
DI
RI (I)
D3 LDAL 1 (I) H
RI (Ø)
DI TSD2
D2
R2 (I)
D3 LDAL 2 (I) H
R2 (Ø)
D3 LDAL 2 (I) L
DI TSD3
D3
R3 (I)
D3 LDAL 3 (I) H
R3 (Ø)
CLK
CLR
74LS139 E28
D3 LDAL 2(I)H
1A
1Y0
D3 RD D L
1Y1
D3 RD C L
D3 LDAL 3(I) H
1B
1Y2
D3 RD B L
1G
1Y3
D3 RD A L
D3 DIN H
74 LS279 E27
D3 SEL 2 L
74 LS279 E27
+5V
R2 330
R4 680
J3
BPI
BIRQ7 L
BR7
NOTE 1
W10 AAI
BR5
BIRQ5 L
8641 E5
AJ2
BSYNC L
AH2
BDIN L
D3 DIN H
D2 DIN L
D5 PAUSE
74 LS04 E13
74 LS04 E13
IC SOCKET XE9
D4 GINT
DI TSD9
AL2
BIRQ4 L
ABI
BIRQ6 L
D4 WRT CSRA
AN2
BIAKO L
BINIT L
AT2
D3 INIT Ø L
BIAKI L
AM2
D3 VEC A
R1 330
R3 680
+5V
R12 4.7K
D3 IE
75451 E38
D3 LDAL 3 (I) H
D3 LDAL 2 (I) H
74LS02 E31
D3 SEL Ø L
74LS02 E31
74 LS240 E32
D3 CSØ L
74LS02 E31
74 LS240 E32
D3 CS1 L
74LS00 E22
D3 XLB
74 LS04 E13
D3 XHB
D4 DIR
74 LS04 E13
D3 XHB
D3 RPLY H
74LS51 E14
D3 RPLY EN L
D4 XMIT (I) H
D3 SEL 2 L
74LS51 E14

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE	CODE	NUMBER	REV.
DRVII-J (D3)		D	CS	M8049-Ø-1	C
SCALE	SHEET 3 OF 6	DIST.			

DEC FORM NO. 11313

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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
DRVII-J (D4)	D	CS	M8049-0-1	C
SCALE —	SHEET 4 OF 6	DIST.		

DEC FORM NO. 5180 1/78

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SPARES

74LS04 E13: 11 → 10

E18: 1 2 3 4 5 6 7 8 9 10 / 20 19 18 17 16 15 14 13 12 11

74LS244 E11: A I/O 7 (17) DB4 YB4 (3) → 9519A E10 IRQ7 (25) DB7 (4) → D1 TSD7
A I/O 6 (11) DB1 YB1 (9) → IRQ6 (24) DB6 (5) → D1 TSD6
A I/O 5 (2) DA1 YA1 (18) → IRQ5 (23) DB5 (6) → D1 TSD5
A I/O 4 (15) DB3 YB3 (5) → IRQ4 (22) DB4 (7) → D1 TSD4
A I/O 3 (13) DB2 YB2 (7) → IRQ3 (21) DB3 (8) → D1 TSD3
A I/O 2 (8) DA4 YA4 (12) → IRQ2 (20) DB2 (9) → D1 TSD2
A I/O 1 (6) DA3 YA3 (14) → IRQ1 (19) DB1 (10) → D1 TSD1
A I/O 0 (4) DA2 YA2 (16) → IRQ0 (18) DB0 (11) → D1 TSD0
OC1 OC2: 1, 19

D3 CS0 L → RD (3), WR (2), CS (1), CD (27)
GINT (17) → R8 4.7K → +5V
IAK (26), RIP (12), PAUSE (15) → 74LS04 E13: 9 → 8 → D5 PAUSE
EI (13), EO (16)

74LS244 E15: D3 IE (15) DB3 YB3 (5) → D5 V9
D4 DIR (17) DB4 YB4 (3) → D5 V8
D6 RRPLY A (6) DA3 YA3 (14)
D6 RRPLY B (4) DA2 YA2 (16)
D6 RRPLY C (8) DA4 YA4 (12)
D6 RRPLY D (2) DA1 YA1 (18)
DB1 YB1 (9), DB2 YB2 (7)
OC1 OC2: 1, 19 → D4 RD CSR L

E16: +5V → 16 → 180Ω → 390Ω → 8

74LS244 E6: A I/O 15 (17) DB4 YB4 (3)
A I/O 14 (11) DB1 YB1 (9)
A I/O 13 (13) DB2 YB2 (7)
A I/O 12 (15) DB3 YB3 (5)
A I/O 11 (2) DA1 YA1 (18)
A I/O 10 (8) DA4 YA4 (12)
A I/O 9 (6) DA3 YA3 (14)
A I/O 8 (4) DA2 YA2 (16)
OC2 OC1: 19, 1

NOTE 1
W11: RPY — AIO (J4)

E16: +5V → 16 → 180Ω → 390Ω → 8

9519A E2: IRQ7 (25) DB7 (4) → D1 TSD7
IRQ6 (24) DB6 (5) → D1 TSD6
IRQ5 (23) DB5 (6) → D1 TSD5
IRQ4 (22) DB4 (7) → D1 TSD4
IRQ3 (21) DB3 (8) → D1 TSD3
IRQ2 (20) DB2 (9) → D1 TSD2
IRQ1 (19) DB1 (10) → D1 TSD1
IRQ0 (18) DB0 (11) → D1 TSD0
RD (3) ← D4 RD EN L
WR (2) ← D3 OUT LB L
CS (1) ← D3 CSI L
CD (27) ← D3 LDAL 2 (1) L
PAUSE (15), RIP (12), IAK (26), GINT (17)
EI (13), EO (16)

R11 4.7K → +5V; IAK → D4 IAK L
R10 4.7K → +5V
74LS00 E22: 9, 10 → 8
R9 4.7K → +5V
74LS240 E32: 11 → 9 → D5 INT L

74LS244 E20: DA1 YA1 (18) → D5 V9
DB4 YB4 (3) → D5 V8
DA2 YA2 (16) → D5 V7
DB3 YB3 (5) → D5 V6
DA3 YA3 (14) → D5 V5
DB2 YB2 (7) → D5 V4
DA4 YA4 (12) → D5 V3
DB1 YB1 (9) → D5 V2
OC1 OC2: 1, 19 ← D4 IAK L

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
DRV11-J (D5)	D	CS	M8049-0-1	C
SCALE —	SHEET 5 OF 6	DIST.		

REV C | SIZE D | CODE CS | NUMBER M8049-0-1

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74LS374 E7
D6 TSD15 D6 TSD14 D6 TSD13 D6 TSD12 D6 TSD11 D6 TSD10 D6 TSD9 D6 TSD8
CLK OC
R2(1) R3(1) R0(1) R6(1) R5(1) R1(1) R7(1) R4(1)
J1 45 46 43 49 48 44 50 47
A I/O 15 A I/O 14 A I/O 13 A I/O 12 A I/O 11 A I/O 10 A I/O 9 A I/O 8

74LS244 E3
DA3 DA4 DB4 DB3 DB2 DA2 DA1 DB1
YA3 YA4 YB4 YB3 YB2 YA2 YA1 YB1
D6 TSD15 D6 TSD14 D6 TSD13 D6 TSD12 D6 TSD11 D6 TSD10 D6 TSD9 D6 TSD8
OC1 OC2

+5V AA2, BA2
C4, C5 6.8UF 10%
C6–C18 .047UF -20 +80
AC2, BC2 AT1, BT1

74LS374 E24
D6 TSD7 D6 TSD6 D6 TSD5 D6 TSD4 D6 TSD3 D6 TSD2 D6 TSD1 D6 TSD0
CLK OC
R0(1) R7(1) R6(1) R1(1) R5(1) R2(1) R4(1) R3(1)
D4 WRT DBA
J1 41 36 42 35 40 38 39 37
A I/O 7 A I/O 6 A I/O 5 A I/O 4 A I/O 3 A I/O 2 A I/O 1 A I/O 0

74LS244 E19
DA1 DB4 DA2 DB3 DA3 DB2 DA4 DB1
YA1 YB4 YA2 YB3 YA3 YB2 YA4 YB1
D6 TSD7 D6 TSD6 D6 TSD5 D6 TSD4 D6 TSD3 D6 TSD2 D6 TSD1 D6 TSD0
OC1 OC2
D3 RD A L

D4 DIR A
D4 XRPLY A L
D4 XRPLY B L
D4 DIR B
74LS241 E23
J1 29 31 33 27 18 24 22 20
E16 180Ω 390Ω +5V
74LS240 E32
D6 RRDY A
D6 RRPLY A
D6 RRPLY B
D6 RRDY B
74LS00 E43
D6 BXMIT L

D4 DIR C
D4 XRPLY C L
D4 XRPLY D L
D4 DIR D
74LS241 E23
J2 20 22 18 24 27 31 33 29
E16 180Ω 390Ω +5V
74LS240 E32
D6 RRDY C
D6 RRPLY C
D6 RRPLY D
D6 RRDY D
74LS00 E43
D6 CXMIT L
D6 DXMIT L

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
DRV11-J (D6)	D	CS	M8049-0-1	C
SCALE	SHEET 6 OF 6	DIST.		

DEC FORM NO. DRD 130

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M7948-0-0 D UA J

10.44 (265.18 MM) REF

6 30 COMPONENT SIDE VIEW

5 4 27(QTY 8)

J1

8.41 (213.61 MM) REF.

NOTES

STEP E	↑ Y AXIS ___ STEP = TIMES
REPEAT	→ X AXIS ___ STEP = TIMES

CHK	CHANGE NO	REV
	M7948-MK6	J

M. DENSMORE 7/4/83
J. CURTIS

ETCH REV. F-P1
FLP1

SIGNATURES	DATE
DRN. M DENSMORE	6/30/83
CHK D	7/4/83
MECH.ENG.	9-1-83
PROJ.ENG.	9-1-83
PROD.	9-1-83
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M7948-0	

digital

TITLE LS11-
FOUNDATION MODULE

SIZE	CODE	NUMBER	REV
D	UA	M7948-0-0	J

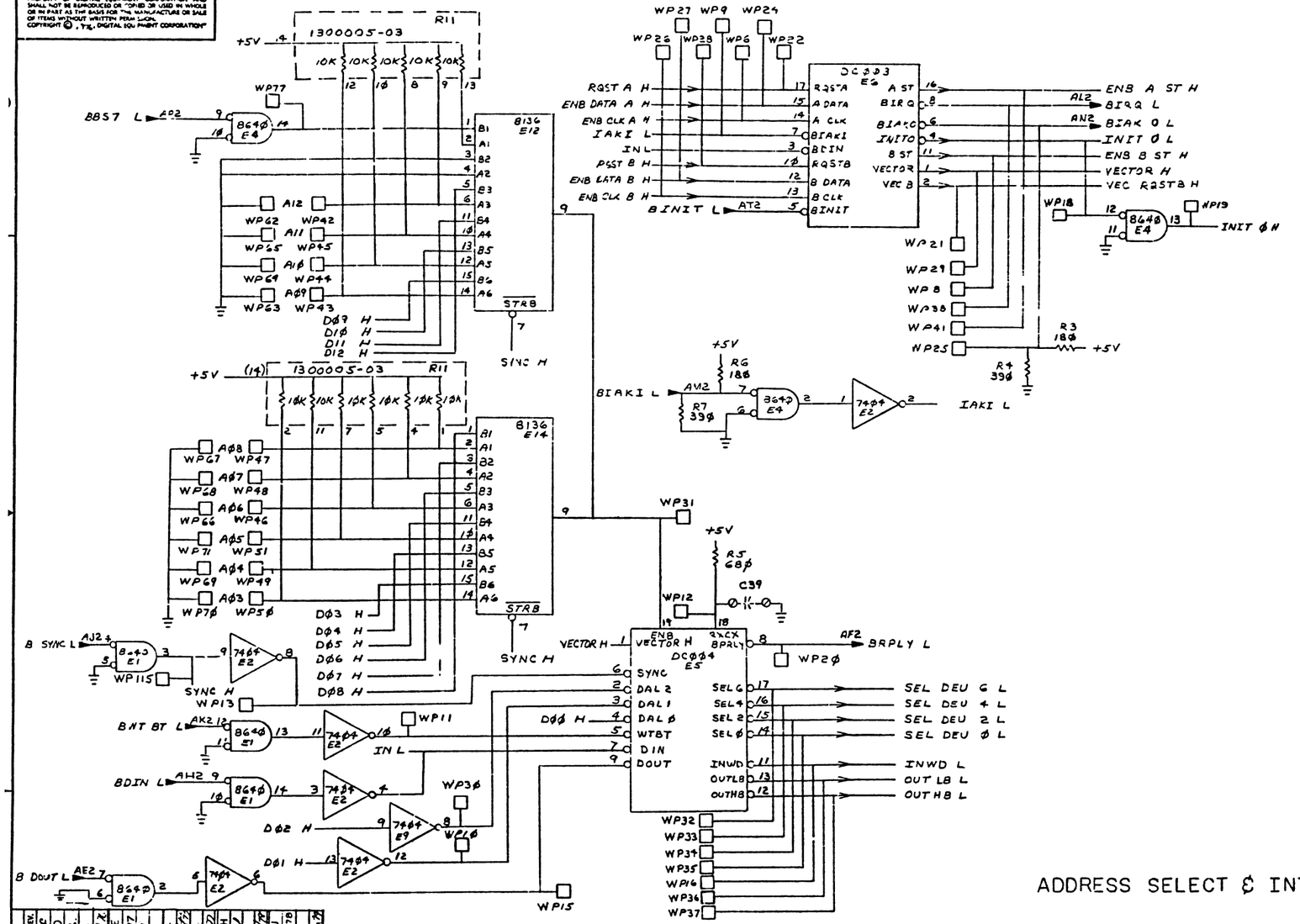
MK 1 WO# 302049

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NOTES:

1. CAPACITOR C39 IS OPTIONAL DO NOT INSERT.
2. ☐ INDICATES WIRE WRAP PINS
3. UNLESS OTHERWISE SPECIFIED THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	Vcc	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
IC DEC 8640	8	1
IC DEC DC003	18	9
IC DEC DC004	20	10



ADDRESS SELECT & INTERRUPT CONTROL LOGIC

REVISIONS			
CHK	CHANGE NO.	REV.	
	ORIGINATED	C	
JW	M7948-0003I	D	
H.Stevenson 6-4-76			
A.TUINESSEN			
JW	M7948-0003K	E	
R.Pitch 25 Aug 77			
JW	M7948-0003	F	
S.TAFLIS			
E.L. S. Emery 11 Nov 77			
JW	M7948-MK004	H	
R.Gilbert 4 Aug 78			
R. SALLEY			
JW	M7948-MK005	J	
H. Stevenson 29 DEC 78			
B. GINSBERG			

DRN		NUMBER
CHK		
ENG		
PROJ. ENG		
PROD		
NEXT HIGHER ASSY.		
B-DD-M7948-Ø		
SCALE NONE		
SHEET 1 OF 3		

FIRST USED ON DRV11-P

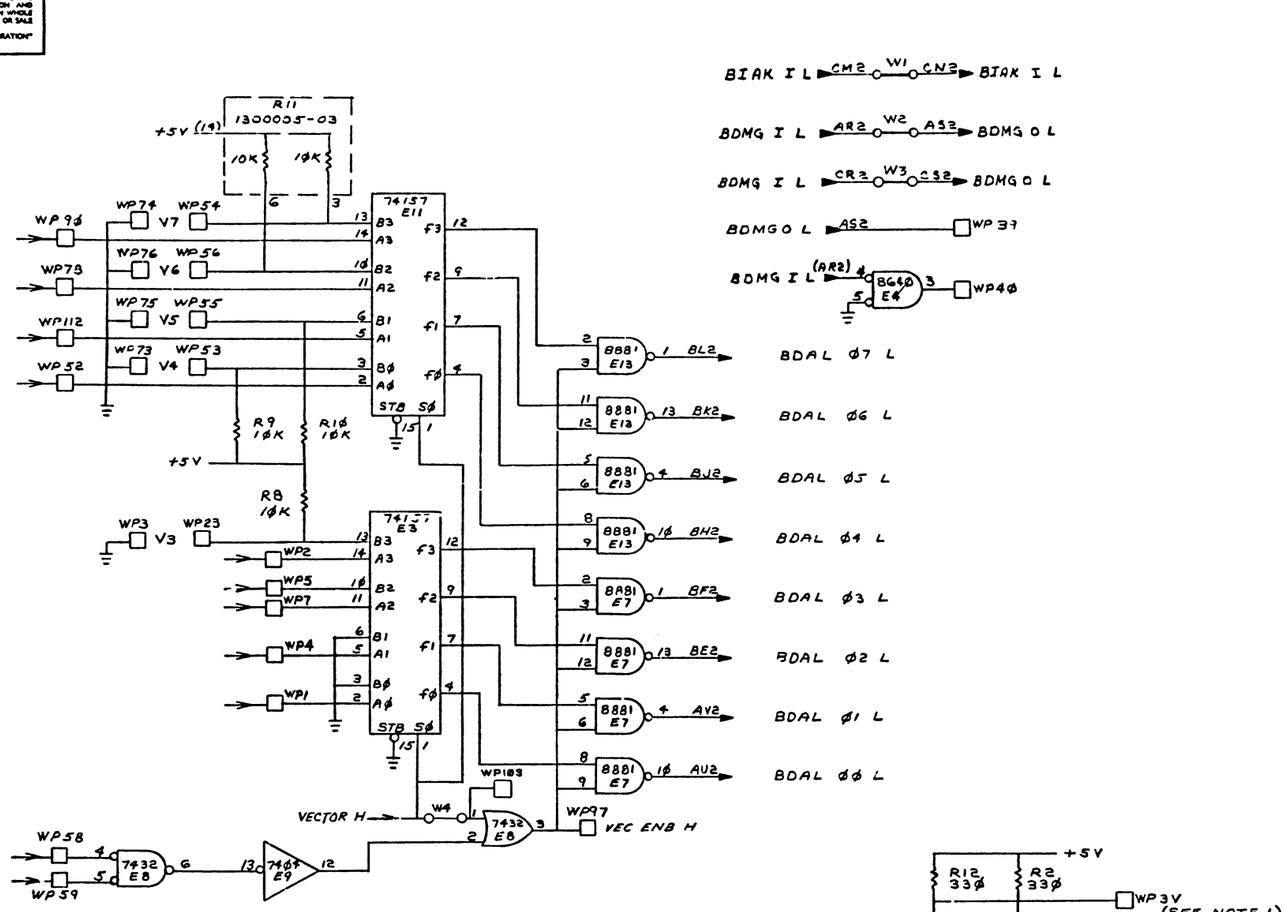
digital

TITLE LSI-11 FOUNDATION MODULE

SIZE	CODE	NUMBER	REV.
D	CS	M7948-Ø-1	J

DIST.

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NOTE:
1. 3V WIRE WRAP PINS ARE NOT COMMON
2. □ INDICATES WIRE WRAP PINS
USE BERG WIRE WRAP PINS ONLY
DEC PART NO. 9009217
BERG PART NO. 75404-028

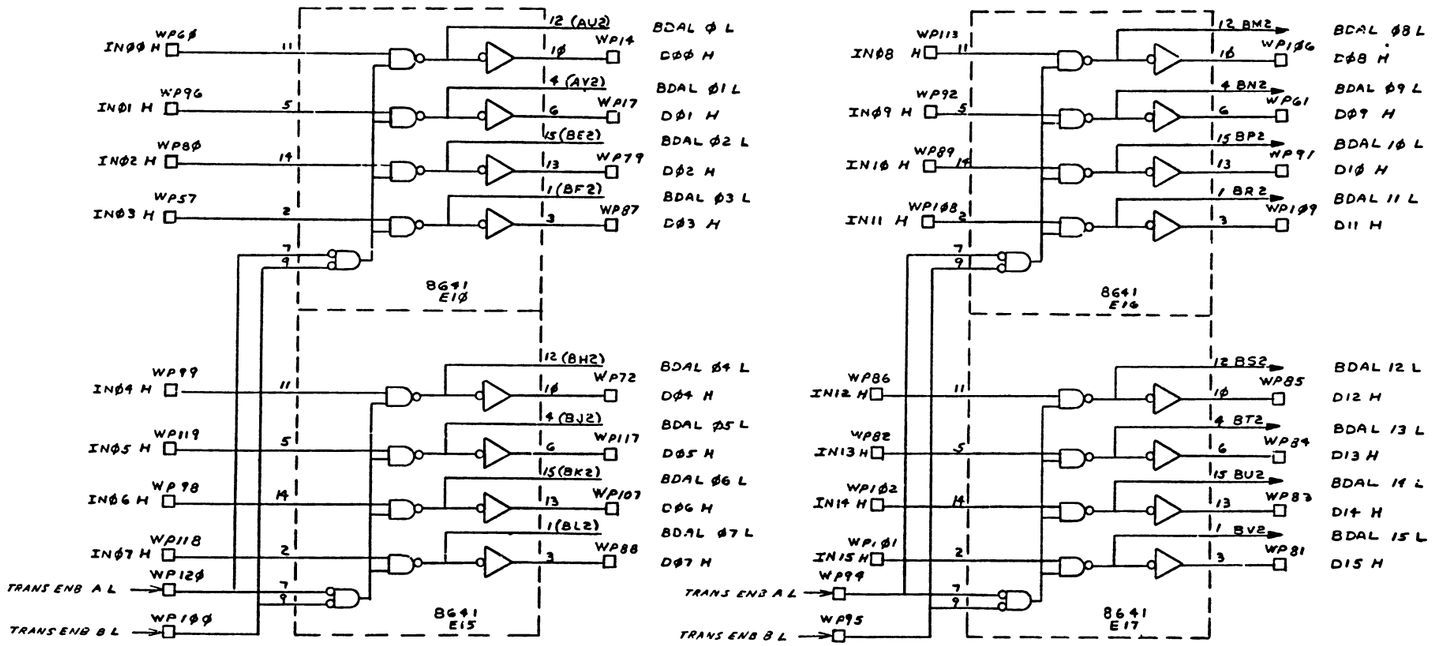
CSR & VECTOR SELECT LOGIC & I/O CONNECTOR

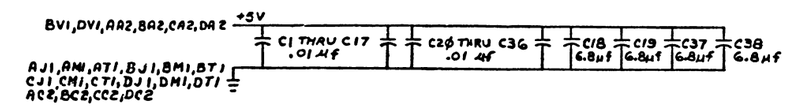
REVISIONS		
CHK	CHANGE NO	REV

TITLE LSI-11
FOUNDATION MODULE
SCALE
SHEET 2 OF 3
SIZE D | CODE CS | NUMBER M7948-Ø-1 | REV. J
DIST.

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☐ INDICATES WIRE WRAP PINS



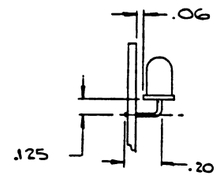


INPUT/OUTPUT DATA LINES

REVISIONS												
SYMBOL	CHANGE NO	DATE										

TITLE	SIZE	CODE	NUMBER	REV.
LSI-11 FOUNDATION MODULE	D	CS	M7948-Ø-1	J
SCALE ⟷ SHEET 3 OF 3	DIST			

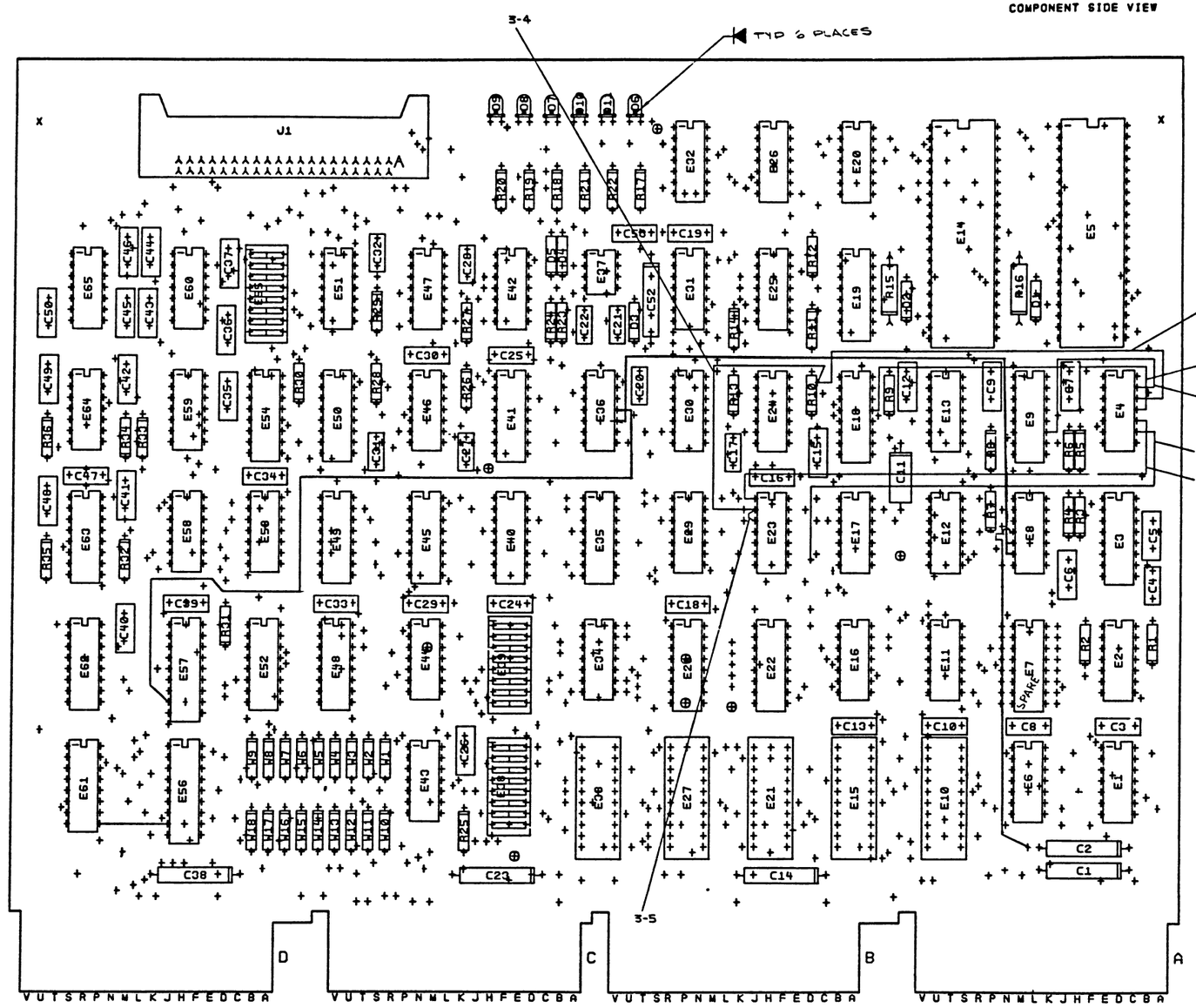
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SUGGESTED LED MTG
TYPICAL 6 PLACES

ECO #3
ETCH CUT SIDE 2:
3-1. BETWEEN THE PTH FROM E18 PIN 1 SIDE 1, AND E23 PIN 6.
WIRE ADDS SIDE 1:
3-2. FROM THE PTH CONNECTED TO E23 PIN 6 AND TO E4 PIN 9.
3-3. FROM THE PTH (NEAR THE BODY OF R10) TO E4 PIN 12.
3-4. FROM THE PTH (NEAR THE BODY OF R10) TO E23 PIN 2.
3-5. FROM E23 PIN 2 TO E23 PIN 3.
3-6. FROM E23 PIN 1 TO E4 PIN 10.
3-7. FROM E18 PIN 13 TO E4 PIN 11.
3-8. FROM E9 PIN 11 TO E4 PIN 13.

COMPONENT SIDE VIEW



NOTES: WITHOUT INK

CHK	CHANGE NO	REV
CW	M7951-00001	D
CV	M7951-00003	E
KA	M7951-00003	E
DE	M7951-00004	F
RH	M7951-00004	F
RH	M7951-M0006	H

ETCH CUT-SIDE 1
1. FROM AL2 TO E56-8

WIRE ADDS
1. CONNECT E61-9 TO E56-8
2. " E57-8 TO E36-11
3. " E36-10 TO E8-9&6
4. " E8-4 TO FEEDTHRU NEXT TO C2 WHICH CONNECTS TO AL2

(CONT. IN UPPER LEFT CORNER)

ETCH REV.	E-P1
P.C. DESIGN DATA BASE REV.	E

SIGNATURES	DATE
DRN. [illegible]	11/4/76
CHK'D. [illegible]	11/4/76
ENG. [illegible]	11/10/76
PROJ.ENG. [illegible]	11/10/76
PROD.	
SCALE 2/1	
SHT. 1 OF 7	

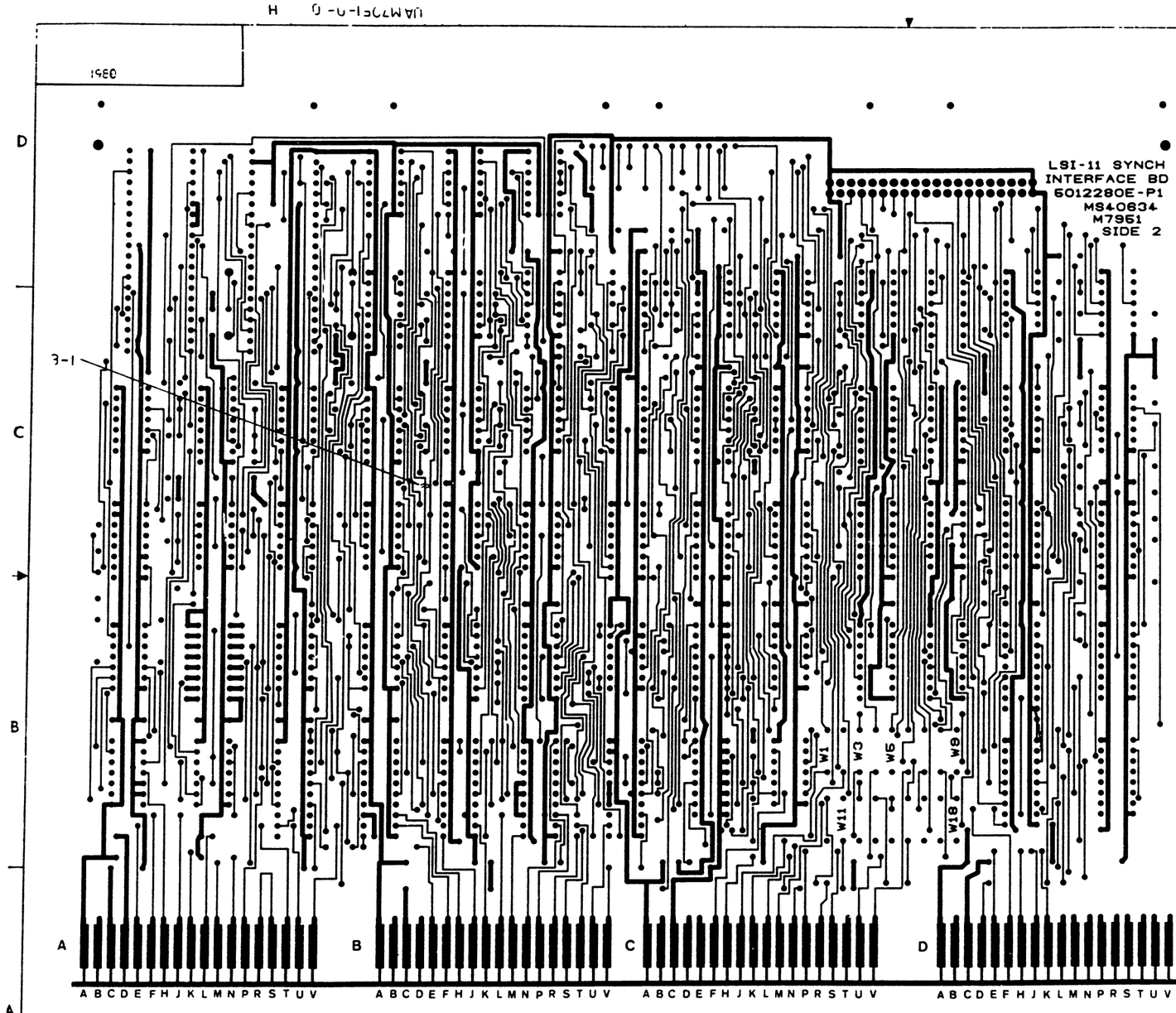
digital

TITLE LSI SYNC INTERFACE BOARD

SIZE	CODE	NUMBER	REV
D	UA	M7951-0-0	H

NEXT HIGHER ASSY. 8-00-M7951-0

MS# 40634



NOTES:

1. REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE2, LAYER 2:
 A CONNECTOR-B
 B CONNECTOR-B,D
 C CONNECTOR-B,D,E,T
 D CONNECTOR-B,L,M,N,P,R,S,T,U

WITHOUT INK

VIEWED FROM SIDE 2

LSI SYNC INTERFACE BOARD

DUA M7951-0-0 H

SCALE 2/1

8 7 6 5 4 3 2 1

REWORK INSTRUCTIONS WITH INK

ETCH CUTS

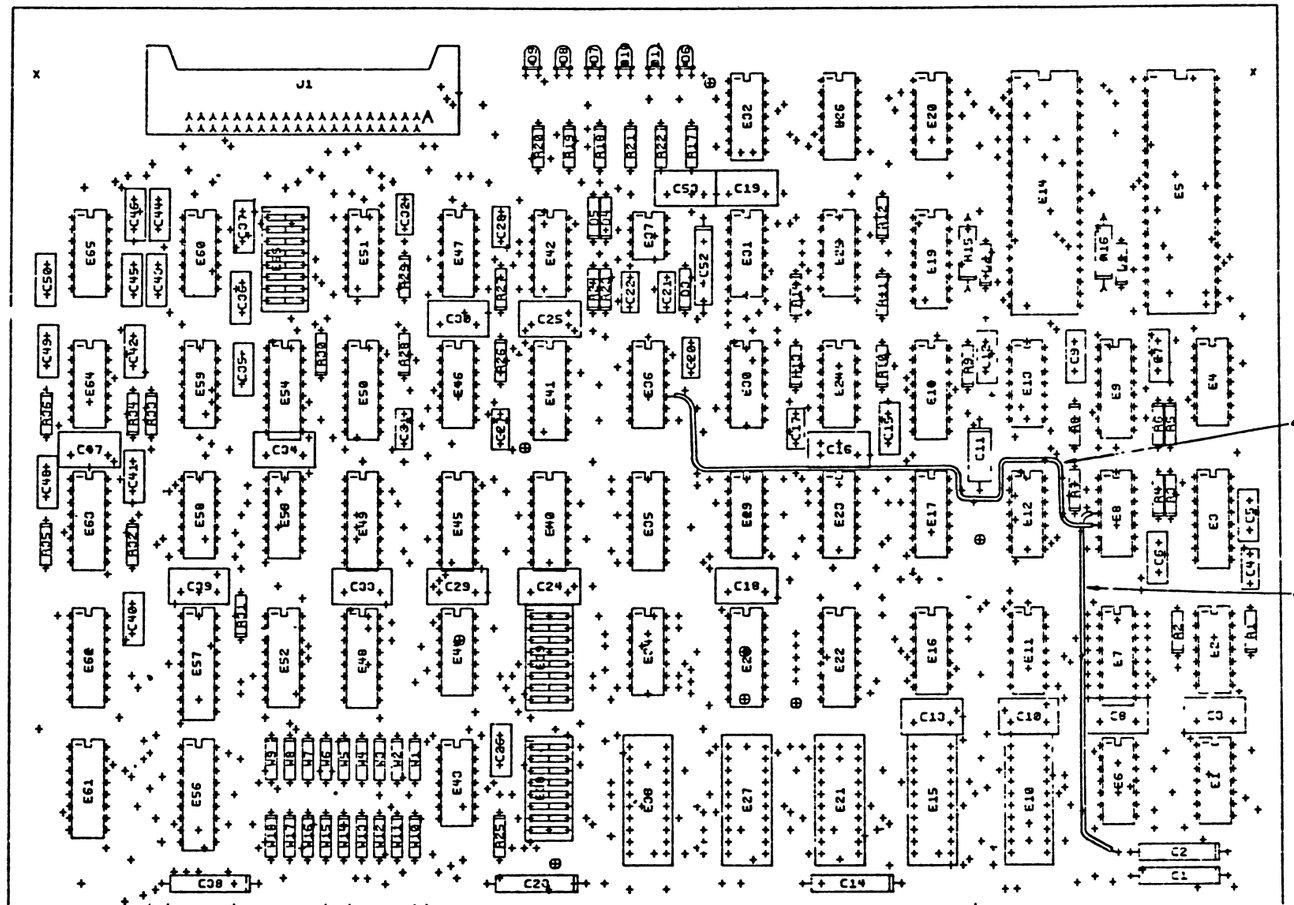
4-1 FROM AL2 TO E56-8 (SIDE 1)

4-2 BETWEEN PTH FROM E18-1, SIDE1 AND E23-6 (SIDE2)

WIRE ADDS SIDE 1:

4-3 FROM E8-9 TO PTH TO LEFT OF C2 THAT CONNECTS TO AL2

4-4 FROM E8-5 TO E36-10



WITH INK

REVISIONS		
CHK	CHANGE NO	REV

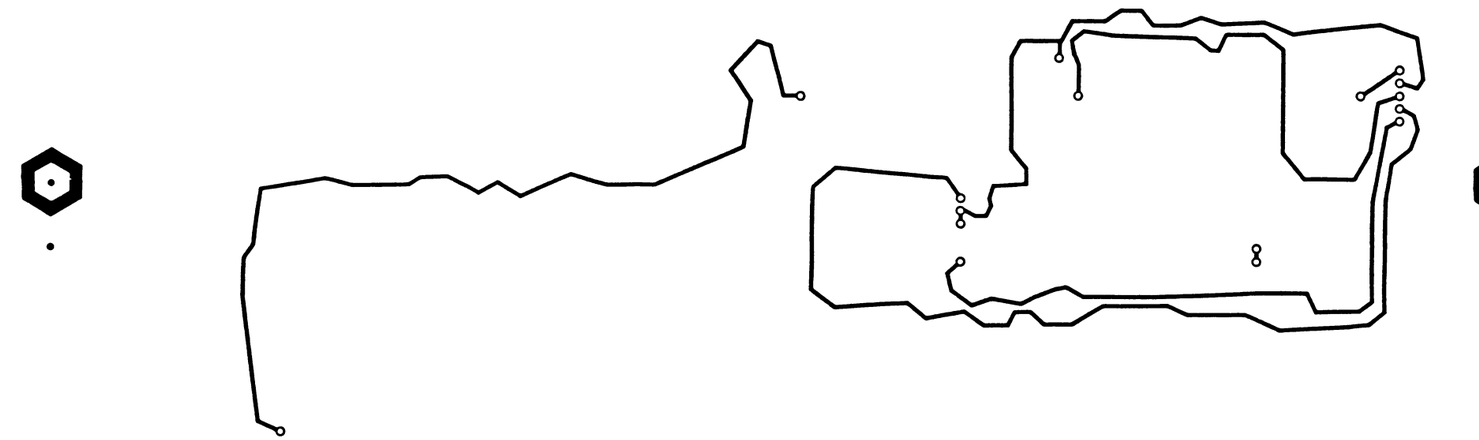
TITLE	SIZE	CODE	NUMBER	REV
LSI SYNC INTERFACE BOARD	D	UA	M7951-Ø-Ø	H
SCALE 2/1	SHEET 4 OF 7	DIST		

DUA M7951-0-0 H

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M7951
5012280D

COPPER INK REV A·P2



INK
REV A·
P2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI SYNC INTERFACE BOARD	D	UA	M7951-Ø-Ø	H
SCALE 2/1 SHEET 5 OF 7	DIST			

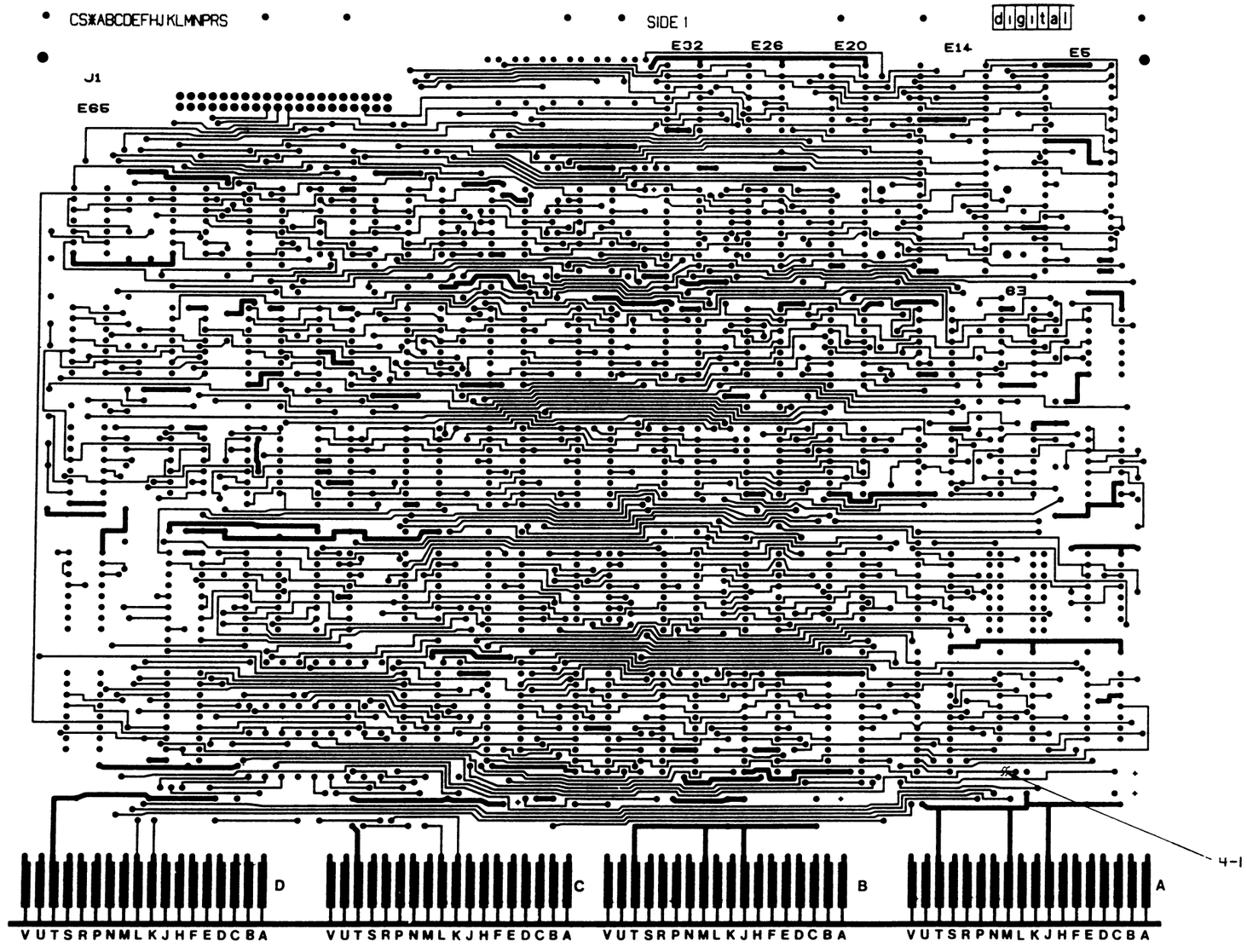
DUA M7951-Ø-Ø H

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M7951
5012280E-P1
MS40634

CS*ABCDEFHJKLMNPRS

SIDE 1



WITH INK

VIEWED FROM SIDE 1

NOTES:

1. REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 1, LAYER 1:
 A CONNECTOR-B,C,D,E,F,H,K,L,N,P,R,S,U
 B CONNECTOR-B,C,D,E,F,H,K,L,N,P,R,S,U
 C CONNECTOR-B,C,D,E,F,H,J,M,N,P,R,S,U
 D CONNECTOR-B,C,D,E,F,H,J,M,N,P,R,S,U

REVISIONS		
CHK	CHANGE NO	REV

TITLE	LSI SYNC INTERFACE BOARD
SIZE	D
DUA	M7951-0-C
REV	H
SCALE	2/1
SHEET	6 OF 7

DUA M7951-0-0 H

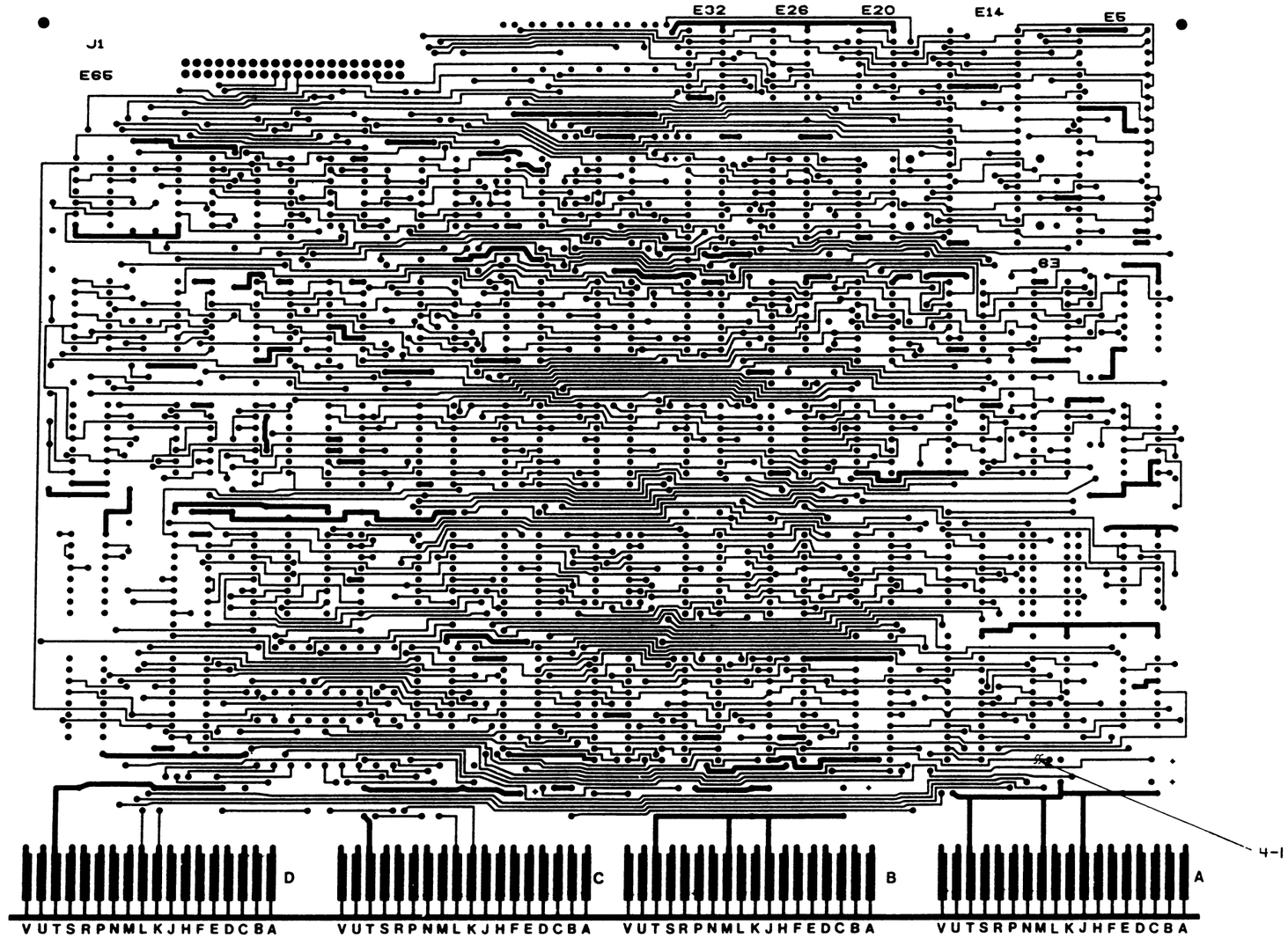
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M7951
5012280E-P1
MS40634

CS*ABCDEFHJKLMNPRS

SIDE 1

digital



NOTES:

1. REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 1, LAYER 1:
 A CONNECTOR - B,C,D,E,F,H,K,L,N,P,R,S,U
 B CONNECTOR - B,C,D,E,F,H,K,L,N,P,R,S,U
 C CONNECTOR - B,C,D,E,F,H,J,M,N,P,R,S,U
 D CONNECTOR - B,C,D,E,F,H,J,M,N,P,R,S,U

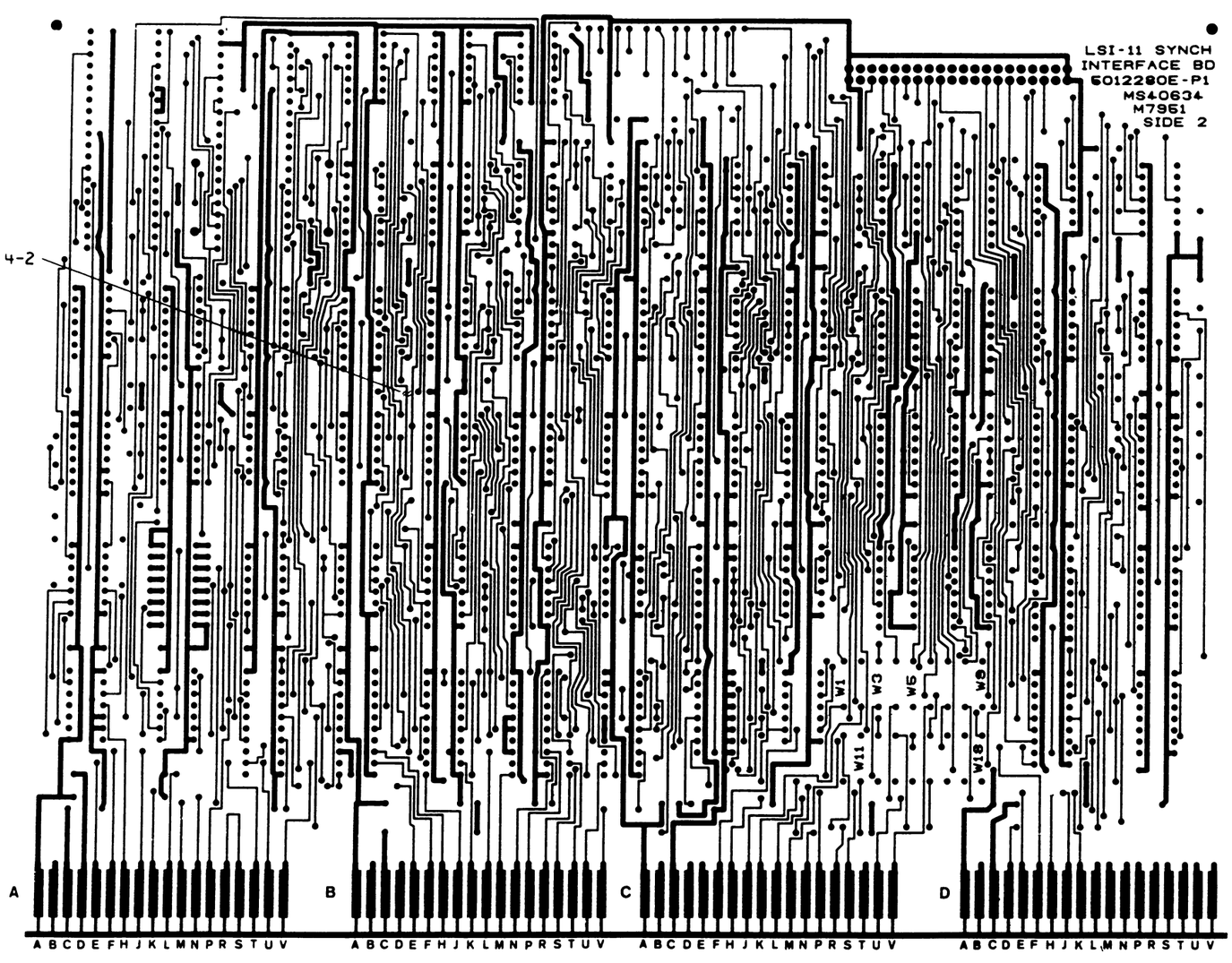
WITH INK

VIEWED FROM SIDE 1

REVISIONS		
CHK	CHANGE NO	REV

TITLE	LSI SYNC INTERFACE BOARD
SCALE	2/1
SHEET	6 OF 7
SIZE	D
DWG NO	DUA M7951-0-C
REV	H

DUA M7951-0-0 H



NOTES:

1 REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE2, LAYER 2:
A CONNECTOR-B
B CONNECTOR-B,D
C CONNECTOR-B,D,E,T
D CONNECTOR-B,L,M,N,P,R,S,T,U

WITH INK

VIEWED FROM SIDE 2

REVISION HISTORY		
A F	ECO NUMBER	REV

TITLE	DOCUMENT NUMBER			
	SIZE	CODE	NUMBER	REV
LSI SYNC INTERFACE BOARD	D	UA	M7951-0-0	H
	SCALE 2/1		SHEET 7 OF 7	

DUA M7951-0-0 H

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DI BDAL 15 L
DI BDAL 12 L
DI BDAL 11 L
DI BDAL 14 L
BV2 BS2 BR2 BU2
DI/D2 QDL 15 N
DI/D2 QDL 12 N
DI/D2 QDL 11 N
DI/D2 QDL 14 N
BUS 3 BUS 2 BUS 1 BUS Ø
DAT 3 DAT 2 DAT 1 DAT Ø
DCØØ5 E33
+5V
JA 3 JA 2 JA 1
MATCH
MEM B
JAV 3 JAV 2 JAV 1
XMIT REC
BUS XCVR
E38-1 E38-2
(HI2) (AI1)
DI BBS7 L
AP2
DI DTI SEL Ø L
DI DTI SEL 2 L
DI DTI SEL 4 L
NAND E43
DI EN GDL TO BDAL N
DI ~ INWDB N

DI BDAL Ø4 L
DI BDAL Ø3 L
DI BDAL Ø2 L
DI BDAL Ø1 L
BN2 BF2 BE2 AV2
DI/D2 GDL Ø4 N
DI/D2 GDL Ø3 N
DI/D2 GDL Ø2 N
DI/D2 GDL Ø1 N
DCØØ5 E15
E35 E39-1 E39-2
(AØ4) (AØ3)
E33 E39-7 E39-8
1Ø (VØ4)
9 (VØ3)
DG EN UPPER VEC H
(VØ2)
DI EN GDL TO BDAL N
DI ~ INWDB N

DI BDAL 1Ø L
DI BDAL Ø9 L
DI BDAL Ø8 L
DI BDAL 13 L
BP2 BN2 BM2 BT2
DI/D2 GDL 1Ø N
DI/D2 GDL Ø9 N
DI/D2 GDL Ø8 N
DI/D2 GDL 13 N
DCØØ5 E27
E38 E38-3 E38-4 E38-5
(AØ1) (AØ9) (AØ8)
E39-3 14 (VØ8)
DG EN VEC TO BUS H
DI EN GDL TO BDAL N
DI ~ INWDB N

DI BDAL Ø7 L
DI BDAL Ø6 L
DI BDAL Ø5 L
DI BDAL ØØ L
BL2 BK2 BJ2 AV2
DI/D2 GDL Ø7 N
DI/D2 GDL Ø6 N
DI/D2 GDL Ø5 N
DI/D2 GDL ØØ N
DCØØ5 E21
E38 E38-6 E38-7 E38-8
(AØ7) (AØ6) (AØ5)
E35 E39-4 E39-5 E39-6
(VØ7) (VØ6) (VØ5)
DI EN GDL TO BDAL N
DI ~ INWDB N

DG SYNC L
DCØØ4 E1Ø
SYNC BREF
DAL 2 DAL 1 DAL Ø
SEL 6 SEL 4 SEL 2 SEL Ø
AF2
DI BREPLY L
DI SEL 6 L
DI SEL 4 L
DI SEL 2 L
DI SEL Ø L
DI/D2 GDL ØØ L
DI BWTBT L
DI BDOUT L
DG DIN L
DG EN VEC TO BUS H
DI INIT N
WTBT DOUT DIN VECTOR
AK2 BE2
OUT LB OUT HB INWD
ENB RXCX
DI OUTLB L
DI OUTHB L
DI INWD L
DI BINIT L
AT2
NAND E1
NAND E12
DI INIT L
+5V
R4 3.83K
C6 22ØØ pf
D3 CLR H
8881 E8
DI LD TXDBUF (1) H
DI LD PARCSR (1) H
8242 E24
DI INWDB N
DI INWDB L
NAND E16

+5V
R8 1Ø K
C7 1ØØ pf
DI SEL 6 L
DI OUTLB L
DI LD TXCSR HB H
DI SEL 4 L
DI OUTHB L
DI LD TXCSR HB L
DI SEL Ø L
DI LD RXCSR HB H
NAND E6
NAND E23
NAND E12
DI LD TXDBUF (1) H
DI LD TXDBUF (Ø) H
D4 +3V

+5V
R6 1Ø K
C7 15Ø pf
DI OUTHB L
DI OUTLB L
DI SEL 2 L
DI LD PARCSR (1) N
DI LD PARCSR (Ø) N
D4 +3V

DI SEL 4 L
DI INWDB L
DI SEL 2 L
DI SEL Ø L
NAND E11
DI DTI SEL 4 H
DI DTI SEL 4 L
DI DTI SEL 2 L
DI DTI SEL Ø L

REVISIONS

REV.	CHANGE NO.	BY
U	7951-00006	C. VALENTINE
E	M7951-00003	D. LUCKER
F	M7951-00004	R. HARRINGTON
H	M7951-MKOU	J. CURTIS

DRN.	Keith Cook	9 OCT 77
CHK'D.	[illegible]	13 JAN 78
ENG.	[illegible]	13 JAN 78
PROJ. ENG.	[illegible]	13 JAN 78
PROD.	[illegible]	13 JAN 78
NEXT HIGHER ASSY.		
	D-UA-M7951-0-2	
SCALE		
SHEET	1 OF 6	

FIRST USED ON: DUVII

digital

TITLE: LSI-11 SYNC INTF (DI)

SIZE	CODE	NUMBER	REV
D	CS	M7951-0-1	H
DIST			

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D1 INWDB L

LEGEND
SEL 0 : A0, B0 SELECTED
SEL 2 : A1, B1 SELECTED
SEL 4 : A2, B2 SELECTED
SEL 6 : (NOT USED)

E35 74LS253
- D3 DATA SET CH (L) N
- D4 RX ERR H
- D5 DNA N
- D3 RING N
- D4 OVRN ERR N
- D5 MAINT DATA (L) N
- → D1/D2 QDL 15 N
- → D1/D2 QDL 14 N

E41 74LS253
- D3 CLR TO SD N
- D4 FRM ERR N
- D5 SS CLK (L) N
- D3 CARRIER N
- D4 PAR ERR N
- D5 MS Ø1 (L) N
- → D1/D2 QDL 13 N
- → D1/D2 QDL 12 N

E50 74LS253
- D4 REC ACT (L) N
- D4 MS ØØ (L) N
- D3 SEC REC DAT N
- D4 RX INP N
- → D1/D2 QDL 11 N
- → D1/D2 QDL 10 N

E49 74LS253
- D3 DATA SET RDY N
- D4 STRIP SYNC (L) N
- D3 MSTRST (L) N
- → D1/D2 QDL Ø9 N
- → D1/D2 QDL Ø8 N

E12 74LS04
- D1 SEL 4 L → 13 → 12
- D1 SEL 2 L → 11 → 10

E40 74LS253
- D4 RX DONE (L) N
- D4 RX DBØ7 N
- D5 TK DONE N
- D4 RX INTEB (L) N
- D4 RX DBØ6 N
- D5 TK INTEB (L) N
- → D1/D2 QDL Ø7 N
- → D1/D2 QDL Ø6 N

E43 74LS253
- D4 DATA SET INTEB (L) N
- D4 RX DBØ5 N
- D5 DNA INTEB (L) N
- D4 SCH SYNC (L) N
- D4 RX DBØ4 N
- D5 SEND (L) N
- → D1/D2 QDL Ø5 N
- → D1/D2 QDL Ø4 N

E48 74LS253
- D3 SEC TX (L) N
- D4 RX DBØ3 N
- D5 HALF DUP (L) N
- D3 RTS (L) N
- D4 RX DBØ2 N
- → D1/D2 QDL Ø3 N
- → D1/D2 QDL Ø2 N

E54 74LS253
- D3 DTR (L) N
- D4 RX DBØ1 N
- D4 RX DBØØ N
- D5 BREAK (L) N
- → D1/D2 QDL Ø1 N
- → D1/D2 QDL ØØ N

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	LSI-11 SYNC INTF (D2)	SIZE	CODE	NUMBER	REV.
		D	CS	M7951-0-1	H
SCALE	SHEET 2 OF 6	DIST.			

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D3 EIA RING N [22] — SEE NOTE 1 — J1 X — W1 → CN2 — 1489A E4A — C44 470 pf

D3 EIA CLR TO SD N [5] — J1 T — W2 → CJ2 — 1489A E4B — C35 470 pf — 74LS04 E5A — R29 1KΩ — C32 .01 uf — 8242 E4C — D3 CLR TO SD N

D3 EIA CARRIER N [8] — J1 BB — W3 → CK2 — 1489A E4B — C34 470 pf — 74LS04 E5A — R27 100Ω — C28 .01 uf — 8242 E4C — D3 CARRIER N

D3 EIA DATA SET RDY N [6] — J1 Z — W12 → CP2 — 1489A E4B — C37 470 pf — 74LS04 E5A — R26 1KΩ — C27 .01 uf — 8242 E4C — D3 DATA SET RDY N

D3 EIA SEC REC N [12] — J1 JJ — E55-3 — W4 → CL2 — 1489A E4B — C46 470 pf — 74LS04 E5A — R28 1KΩ — C31 .01 uf — 8242 E4C — D3 SEC REC N

D3 EIA SERIAL DATA IN L [3] — J1 J — W5 → CF2

D3 EIA TRS CLK N [15] — J1 N — W10 → CL2

D3 EIA REC CLK N [17] — J1 R — W6 → CV2

[GND] [1] — J1 A

[SIG GND] [7] — J1 B

[GND] [7] — J1 UU

[GND] [1] — J1 VV

+5V — R9 1.5K — C11 10 uf — 74LS02 E2B — D4 +3V — D3 RING DLY N — 74LS74 E4 — +3V

D3 RING N — 74LS32 E2B — R13 100Ω — C17 .01 uf ≈ 2 uS — 8242 E2C — R11 1K +5V

D5 SS CLK (Ø) N — D5 MS Ø1 (1) N — 1488L E3I — R32 7.5K — E55-7 — J1 L — D3 EIA CLK EXT L [24]

D6 SKC H — 1488L E3I — E55-5 — W15 → DD2

D1 W DTI SEL Ø N — 74LS74 E3A — D4 DATA SET CH (1) N — D3 CLR L

D5 SERIAL DATA OUT H — D5 MSØØ (Ø) N — 74LS04 E3C — D3 TTL DATA OUT L — 74LS04 E3D — 1488L E3I — J1 F — D3 EIA XMIT DATA L [23] — W16 → DE2

74LS175 E52 — D3 R3(1) 15 — R3(Ø) 14 — D2 R2(1) 10 — R2(Ø) 11 — DI R1(1) 7 — R1(Ø) 6 — DØ R0(1) 2 — R0(Ø) 3 — CLK CLR

D1/D2 GDL Ø3 H — D3 SEC TX (1) N — D3 SEC TX (1) L

D1/D2 GDL Ø2 H — D3 RTS (1) N — D3 RTS (1) L

D1/D2 GDL Ø1 H — D3 DTR (1) N — D3 DTR (1) L

D1 LD RXCSR LB H

E55-6 — W7 → DF2 — J1 RR — D3 EIA DATA RATE SEL H [23]

E55-2 — W17 → DH2 — J1 FF — D3 EIA SEC X MIT H [11]

1488L E5J — W8 → DJ2 — J1 V — D3 EIA REQ TO SD H [4]

1488L E5J — W18 → DK2 — J1 DD — D3 EIA DATA TERM RDY N [24]

+5V — R10 10K — C15 470 pf — D1 LD TXCSR NB L — D1/D2 GDL Ø8 H — 74LS20 E1B (3 US) — D3 MSTRST (1) N — D3 MSTRST (1) L — D5 +3V

D1 INIT L — 74LS37 E1G — D3 CLR N — 74LS37 E1G — E55-1 — D3 OPT CLR L — D3 CLR L — R31 10K — +5V

NOTES:
1. NUMBERS IN SQUARES ARE PIN # AT MODEM CONNECTOR END OF INTERFACE CABLE.
2. DL -12V (A) SUPPLIES E14-16 AND E3J-16. DL -12V (B) SUPPLIES E5-16 AND E53-1.

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 SYNC INTF. (D3)	D	CS	M7951 - 0 - 1	H
SCALE — SHEET 3 OF 6	DIST			

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D4 +3V
D4 SCN SYNC (1) N
D4 SYNC (1) N
D5 ~RX CLK L
D4 SYNC (Φ) N
D4 DATA RDY L
D4 ~MDET L
D4 REC ACT (1) L
D4 +3V
EG1
332Ω
680Ω
+5V
D4 REC ACT (Φ) H
D4 FIRST IN (1) N
D4 ~MATCH N
D4 FIRST IN (Φ) N
E55-4
R12 10K
D4 SYNC INTR (Φ) L
D4 REC ACT (1) L
D4 SCN SYNC (1) N
(RXCSR BITS 6,5,1)
74LS175 E28
D1/D2 QDL Φ6 N
D1/D2 QDL Φ5 N
D1/D2 QDL Φ4 N
D3 CLR L
D1 LD RXCSR LB N
D4 RX INTEB (1) N
D4 RX INTEB (1) L
D4 DATASET INTEB (1) H
D4 DATASET INTEB (1) L
D4 SCN SYNC (1) H
D4 SCN SYNC (1) L
+5V
RA 10K
D5 MSYN (1) H
D5 MSYN (Φ) H
D5 MAINT DATA (1) H
D4 SERIAL DATA IN H
D3 ETA SERIAL DATA IN L
D5 MAINT Φ1 OR 10 H
D4 RX INP N
D5 MSYN (1) H
D5 MSYN (Φ) H
D5 SERIAL DATA OUT N
.047 47Ω/A
D5 RX CLK N
D3 CLR H
D1/D2 QDL Φ8 N
D5 PARITY INHIBIT N
D1/D2 QDL 11 N
D1/D2 QDL 10 N
D1/D2 QDL 13 N
D1/D2 QDL 13 N
D1/D2 QDL 12 H
D4 +3V
D1 LD PARCSR (1) H
D4 SYNC INTR (1) N
D4 SYNC INTR (Φ) N
D3 CLR L
D5 CLR STATE L
D1 LD PARCSR (1) L
D1/D2 QDL Φ7 N
D1/D2 QDL Φ6 N
D1/D2 QDL Φ5 N
D1/D2 QDL Φ4 N
D1/D2 QDL Φ3 N
D1/D2 QDL Φ2 N
D1/D2 QDL Φ1 N
D1/D2 QDL ΦΦ N
+5V
D6 -12V (A)
D4 RX DB Φ7 N
D4 RX DB Φ6 N
D4 RX DB Φ5 N
D4 RX DB Φ4 N
D4 RX DB Φ3 N
D4 RX DB Φ2 N
D4 RX DB Φ1 N
D4 RX DB ΦΦ N
D4 OVRN ERR N
D4 PAR ERR N
D4 FRM ERR N
D4 +3V
D1/D2 QDL Φ8 N
D1 LD RXCSR HB N
D4 STRIP SYNC (1) H
D4 STRIP SYNC (Φ) H
D3 CLR L
D2/D3 ~QDL 13 L
D1 LD PARCSR (1) N
D4 ISOC (1) N
D4 ISOC (Φ) H
D3 CLR L
D4 SYNC (1) L
D4 ISOC (1) N
C12 12pf
R33 10K +5V
.047 47Ω/A
R36 100
D4 DATA RDY N
D4 DATA RDY L
D4 +3V
D4 FIRST IN (1) N
D4 REC ACT (1) H
D4 REC ACT (Φ) N
D4 SCN SYNC (Φ) N
D3 CLR H
R35 10K +5V
C48 62pf
R25 100
D4 MDET N
C26 330 pf
D4 MATCH N
D4 MATCH L
D4 +3V
D4 STRIP SYNC (1) H
D4 RST CHAR L
D4 DATA RDY N
D4 REC ACT (1) N
D4 RX DONE (1) N
D1 ~DIAG SEL 2 H
D3 CLR L
D4 RX ERR H
D4 RX ERR L

REVISIONS		
CHK	CHANGE NO	REV

TITLE	LSI-11 SYNC INTF (D4)			
SIZE	CODE	NUMBER		REV.
D	CS	M7951-0-1		7
SCALE		SHEET 4 OF 6	DIST.	

MK

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MAINT MODE SELECTION		
MSØ1	MSØØ	MODE
Ø	Ø	NORMAL (EIA)
Ø	1	LOOP-INTERNAL (TTL)
1	Ø	LOOP-EXTERNAL (EIA)
1	1	CTP-SYS TEST (TTL)

D3 EIA RCV CLK N — 74ØØ E25 — C52 47Ø Pf — 74LS14 E5I

D5 MSØØ (Ø) N — 74LS1Ø E26 — D5 SYS TST CLK L
D5 MSØ1 (1) N
D5 MSØØ (1) N — 74LS1Ø E25

D5 MSØØ (Ø) N — 74LS1Ø E26 — D5 RX CLK N
D5 HALF DUP (Ø) L — 74LS2Ø E29
D5 SEND (Ø) L

D5 SS CLK (1) N — 74LS2Ø E32
D5 MS ØØ (1) N

D5 TX CLK N — 74LS1Ø E26

D3 EIA TRS CLK N — 74ØØ E25 — C43 47Ø Pf — 74LS14 E5J — D5 MS ØØ (Ø) N — 74LS2Ø E32

D5 SEND (1) N — TFC
D3 CLR N — CTS
D1/D2 GDL ØB N — MR
D1/D2 GDL Ø9 L — 74LS2Ø E3Ø — D5 PARITY INHIBIT N — EPE
PI
CS2
CSI
MS2
MSI
WL2
WLI
CRL
THRL
DAR
T8
F8
T7 SYNC/
F7 ASYNC
T6
F6
T5
F5
T4
F4
T3
F3
T2
F2
T1
F1
VSS
VGG
VDD
CD
TRO
TCO
DD — D5 EOC L
TNRE
DA
PTM82B
E5

D1/D2 GDL 14 N
D1/D2 GDL 13 N
D1/D2 GDL 12 N
D1/D2 GDL 11 N
D1/D2 GDL 1Ø N
D1 LD PARCSR (1) L
D1 LD TXDBUF (1) L
D5 RST DMA L
D1/D2 GDL Ø7 N
D1/D2 GDL Ø6 N
D1/D2 GDL Ø5 N
D1/D2 GDL Ø4 N
D1/D2 GDL Ø3 N
D1/D2 GDL Ø2 N
D1/D2 GDL Ø1 N
D1/D2 GDL ØØ N

(TXCSR HIGH BYTE; MAINT CTRL)

74LS175 E19

D3 R3(1) — D5 MAINT DATA (1) N
R3(Ø) — D5 MAINT DATA (Ø) N
D2 R2(1) — D5 SS CLK (1) N
R2(Ø) — D5 SS CLK (Ø) H
D1 R1(1) — D5 MS Ø1 (1) N
R1(Ø) — D5 MS Ø1 (Ø) H
D0 R0(1) — D5 MS ØØ (1) N
R0(Ø) — D5 MS ØØ (Ø) H
CLR CLK

D3 CLR L
D1 LD TXCSR HB N

(TXCSR 6,5,4,3,Ø)

74LS174 E22

D5 RS(1)
D4 R4(1) — D5 TX INTEB (1) N
D3 R3(1) — D5 DMA INTEB (1) N
D2 R2(1) — D5 SEND (1) N
D1 R1(1) — D5 HALF DUP (1) N
D0 R0(1) — D5 BREAK (1) H
CLR CLK

D3 CLR L
D1 LD TXCSR LB N

D1 ~ DIT SEL 4 N — 8881 E8 — R7 10K — +5V — D5 RST DMA L
D4 +3V — 74LS74 E4 — D5 EN RST DMA (1) N
D1 DIT SEL 4 N
D5 DMA N
DA — 74LS08 E13

TNRE — 74LS08 E13 — D5 TX DONE N

+5V — D7-12V (B)

D2 ~ INWDB L — 74LS02 E64 — ≈6Ø NS
D1 DIT SEL 2 L — R34 10Ø — C42 6ØØ Pf — 74LS27 E59
D4 DATA RDY L — 74LS02 E64
D4 REC ACT (Ø) L — 74LS02 E64
D4 RST CHAR L — 74LS02 E64

+5V — R32 10K — C40 .02 Pf — 74LS221 E62 — D5 CLR STA.DR L
D4 +3V
(TO RCVR ON D4)

D5 BREAK (Ø) L — 74LS04 E34 — 74LS02 E44 — D5 SERIAL DATA OUT N

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
LSI-11 SYNC. INTF. (D5)	D	CS	M7951-2-1	H
SCALE —	SHEET 5 OF 6	DIST		

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MAINTENANCE INDICATORS

D3 RING H — 74LS04 E47 — D6 — R17 330Ω — +5V
D3 CLR TO SEND H — 74LS04 E47 — D11 — R22 330Ω
D3 DATA SET RDY H — 74LS04 E47 — D10 — R21 330Ω
D3 CARRIER H — 74LS04 E47 — D7 — R18 330Ω
D3 SERIAL DATA OUT H — 74LS04 E47 — D8 — R19 330Ω
D3 SERIAL DATA IN H — 74LS04 E47 — D9 — R20 330Ω

INTERRUPT CONTROL

+5V — E67 330Ω — 680Ω — AH2 — D6 BIAKI L
D4 R.X. DONE (I) H
D3 CLR L
D5 TX DONE (I) H
D4 RX INTEB (I) H
D5 TX INTEB (I) H
DC023 E36 — RQSTA, ENA ST, BIAKI, VECTOR, BINIT, INITO, BDIN, ENB ST, RQSTB, VEC RQSTB, ENA DAT, BIRQ, ENB DAT, BIAKO, ENA CLR, ENB CLR
74LS32 E44 — 74LS04 E2 — D6 EN VEC TO BUS H
E67 330Ω — 680Ω — +5V — 74LS04 E2 — 8881 E28 — AH2 — D6 BIRQ L
D6 ESYNC L — AH2 — 8L40 E1 — 74LS04 E2
+5V — E61 330Ω — 680Ω — D3 DATA SET CH (I) H
D3 CLR L
D5 DMA H
D4 DATA SET INTEB (I) H
D5 DMA INTEB (I) H
DC023 E37 — RQSTA, ENA ST, BIAKI, IEC RQST B, BINIT, VECTOR, BDIN, BIRQ, RQSTB, ENB ST, ENA DAT, INITO, ENB DAT, BIAKO, ENA CLR, ENB CLR
74LS32 E11 — D6 EN UPPER VEC H
E61 330Ω — +5V — AH2 — D6 BIAKO L
D6 BDIN L — AH2 — 8L40 E1 — 74LS04 E2 — D6 SYNC L, D6 DIN L

+12V TO -12V POWER CONVERTER (CHARGE PUMP)

+5V — R3 1.5K — C5 .22Ø pfd — 74LS20 E3 — CK EN — D6 6ØØ KC N
74LS04 E2
+5V — R1 1K — +5V — R2 1K — 74LS04 E2 — R24 22Ø — MH CO02L E37 — C21 .47 uf — D5 DL4A — D3 DL4A — R15 82 — D6 -12V (A)
AD2 — +12V — C33 .047 uf — C32 6.8 uf — C12 6.8 uf — R23 22Ø — MH CO8L E37 — C22 .47 uf — R16 82 — C20 .47 uf — D6 -12V (B) — D1 IN759A — D2 IN759A
C4 .1 ufd (VCO) — 74LS20 E3 — CK EN — 10 — D6 5KC H
R5 1K

M SPARE JUMPERS: CK1, WA9, CL1, DK1, WA9, DL1
E DMA I/O BYPASS: AE2, AS2, CE2, WA8, CS2
BIAK I/O BYPASS: CH2, WA1, CH2

+5V
C1, C14, C23, C38 6.8 ufd
C3, C8, C10, C13, C16, C18, C19, C24, C25, C29, C30, C33, C34, C39, C37 .047 uf

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
LSI-11 SYNC INTF (D6)	D	CS	M7951-0-1	7
SCALE — SHEET 6 OF 6	DIST.			

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C | 0-0-M7957 | UA | D

10.44
(265.17MM)
REF

COMPONENT SIDE VIEW

8.41
(213.61MM)
REF

62
61
8 PLACES

TH2 TH1

NOTES:
1. E77 IS A SPARE LOCATION.

STEP E	↑ Y AXIS ____ STEP ___ TIMES
REPEAT	→ X AXIS ____ STEP ___ TIMES

CHK	CHANGE NO	REV
	M7957-MK0001	C
	R. PLATT	
	BARRINGTON	

ETCH REV. D-P1

SIGNATURES		DATE
DRN.	N. LANDRY	6-1-77
CHK'D.	W. SMITH	6-14-77
MECH.ENG.	W. SMITH	8-10-77
PROJ.ENG.	W. SMITH	8-10-77
PROD.		8-10-77
SCALE 2/1		
SHT. 1 OF 1		
NEXT HIGHER ASSY. B-DD-M7957-0		

digital

TITLE: ASYN MUX

SIZE	CODE	NUMBER	REV
D	UA	M7957-0-0	C

DUA M7957-0-0 C

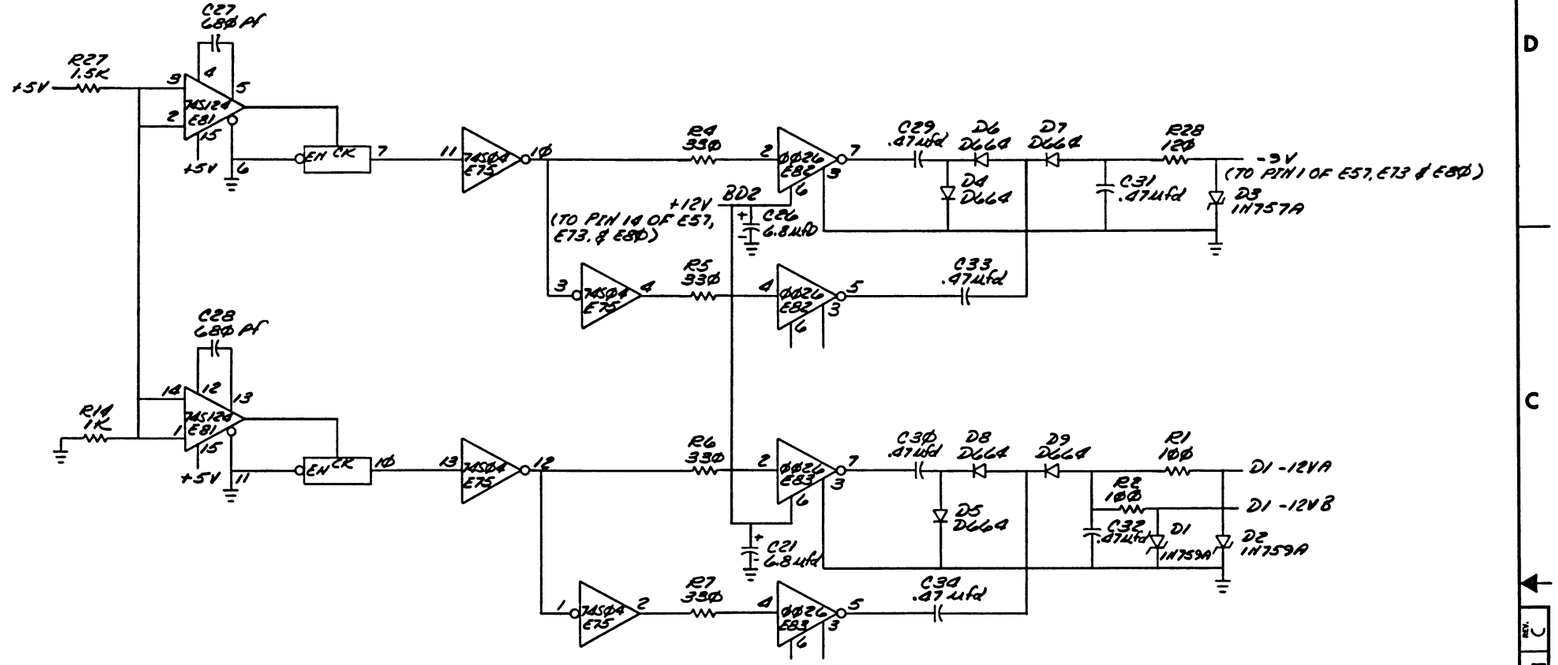
WO# 301716

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BERG PINNING CHART

A	GROUND
B	EIA XMIT DATA Ø0
C	EIA RECEIVED DATA Ø0
D	EIA DATA TERM RDY Ø0
E	EIA RING Ø0
F	EIA FORCED BUSY Ø0
N	EIA REQ TO SEND Ø0
J	
K	GROUND
L	EIA CARRIER Ø0
M	GROUND
N	EIA XMIT DATA Ø1
P	EIA RECEIVED DATA Ø1
R	EIA DATA TERM RDY Ø1
S	EIA RING Ø1
T	EIA FORCED BUSY Ø1
U	EIA REQ TO SEND Ø1
V	
W	GROUND
X	EIA CARRIER Ø1
Y	EIA CARRIER Ø2
Z	GROUND
AA	
BB	EIA REQ TO SEND Ø2
CC	EIA FORCED BUSY Ø2
DD	EIA RING Ø2
EE	EIA DATA TERM RDY Ø2
FF	EIA RECEIVED DATA Ø2
HH	EIA XMIT DATA Ø2
JJ	GROUND
KK	EIA CARRIER Ø3
LL	GROUND
MM	
NN	EIA REQ TO SEND Ø3
PP	EIA FORCED BUSY Ø3
RR	EIA RING Ø3
SS	EIA DATA TERM RDY Ø3
TT	EIA RECEIVED DATA Ø3
UU	EIA XMIT DATA Ø3
VV	GROUND

CLOCK ADDRESS D C B A	BAUD RATE	PERIOD (USEC)
Ø Ø Ø Ø	50	1250.00
Ø Ø Ø 1	75	833.33
Ø Ø 1 Ø	110	568.18
Ø Ø 1 1	134.5	464.68
Ø 1 Ø Ø	150	416.67
Ø 1 Ø 1	300	208.33
Ø 1 1 Ø	600	104.17
Ø 1 1 1	1200	52.08
1 Ø Ø Ø	1800	34.72
1 Ø Ø 1	2000	31.25
1 Ø 1 Ø	2400	26.04
1 Ø 1 1	3600	17.36
1 1 Ø Ø	4800	13.02
1 1 Ø 1	7200	8.68
1 1 1 Ø	9600	6.51
1 1 1 1	INVALID	



(CHARTS)

REVISIONS			
	CHANGE NO.	CHK	REV.
1	M7957-MK0011	[illegible]	C

R. HARRINGTON

DRN	[illegible]	FIRST USED ON DZV11
CHK	[illegible]	digital
ENG.	[illegible]	TITLE ASYN MUX (D1)
PROJ. ENG.	[illegible]	
PROD.	[illegible]	
NEXT HIGHER ASSY.	D-UA-M7957-Ø-Ø	SIZE D CODE CS NUMBER M7957-Ø-1 REV. C
SCALE	—	
SHEET	1 OF 14	DIST.

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NOTE:
DEVICE ADDRESS IS DETERMINED BY SWITCH PACK E30. SWITCH CLOSED (ON) FOR QBUS LOGICAL ONE (LOW).

(ADDRESS BIT 07)
(ADDRESS BIT 06)
(ADDRESS BIT 05)
E30 E30-6 E30-7 E30-8
BDAL 00 L
BDAL 07 L
BDAL 06 L
BDAL 05 L
AV2 BL2 BK2 BJ2
DC005 E19
BUS 0 DAT 0
BUS 1 DAT 1
BUS 2 DAT 2
BUS 3 DAT 3
JA 1 JA 2 JA 3 MATCH
MEN8
JAV 1 JAV 2 JAV 3
XMIT REC
D2 DEVICE DATA BUS 00
D2 DEVICE DATA BUS 07
D2 DEVICE DATA BUS 06
D2 DEVICE DATA BUS 05
74LS04 E47
D2 ODD PARITY L
D2 PARITY ENABLE L
BBS7 L
D5 VECTOR BIT 07 H
D5 VECTOR BIT 06 H
D5 VECTOR BIT 05 H
D4 READ L
D4 READ DEVICE H

(ADDRESS BIT 12)
(ADDRESS BIT 11)
E30 E30-1 E30-2
BDAL 15 L
BDAL 14 L
BDAL 12 L
BDAL 11 L
BV2 BU2 BS2 BR2
DC005 E37
+5V
D2 DEVICE DATA BUS 15
D2 DEVICE DATA BUS 14
D2 DEVICE DATA BUS 12
D2 DEVICE DATA BUS 11
D2 DEVICE SELECT H

(ADDRESS BIT 04)
(ADDRESS BIT 03)
E30 E30-9 E30-10
BDAL 01 L
BDAL 04 L
BDAL 03 L
BDAL 02 L
AV2 BN2 BF2 BE2
DC005 E29
D2 DEVICE DATA BUS 01
D2 DEVICE DATA BUS 04
D2 DEVICE DATA BUS 03
D2 DEVICE DATA BUS 02
D5 VECTOR BIT 04 H
D5 VECTOR BIT 03 H
D5 VECTOR BIT 02 H

(ADDRESS BIT 10)
(ADDRESS BIT 09)
(ADDRESS BIT 08)
E30 E30-3 E30-4 E30-5
BDAL 13 L
BDAL 10 L
BDAL 09 L
BDAL 08 L
BT2 BP2 BN2 BM2
DC005 E29
D2 DEVICE DATA BUS 13
D2 DEVICE DATA BUS 10
D2 DEVICE DATA BUS 09
D2 DEVICE DATA BUS 08
D5 VECTOR BIT 08 H

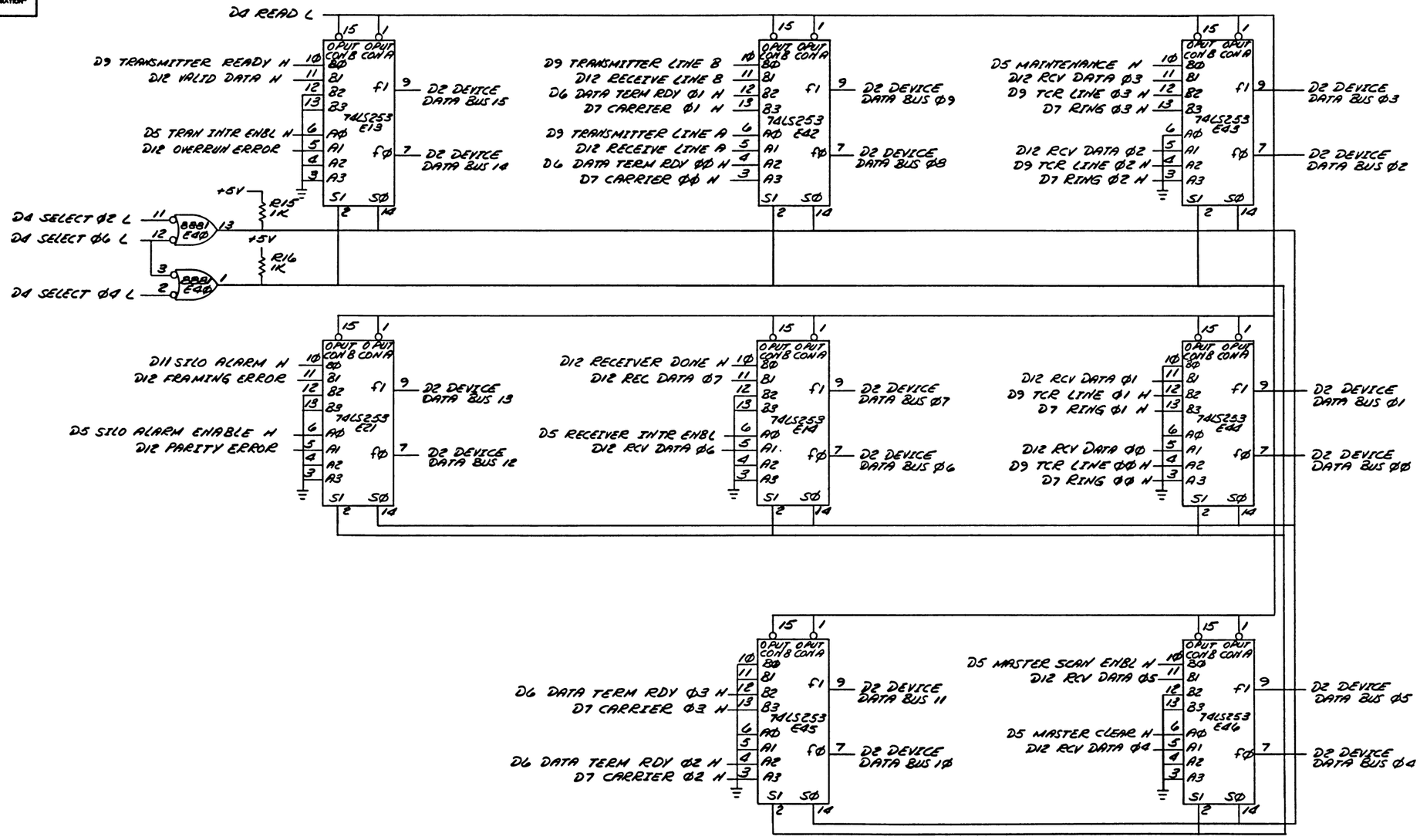
(TRANSCEIVERS)

REVISIONS		
CHK	CHANGE NO	REV

TITLE: ASYN MUX (D2)		SIZE: D	CODE: CS	NUMBER: M7957-0-1
SCALE: —	SHEET 2 OF 14	DIST.		REV. C

DCS M7957-0-1 REV C

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(OUTPUT DATA MULTIPLEXERS)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D3)	D	CS	M7957 - Ø - 1	C
SCALE —	SHEET 3 OF 14	DIST.		

SIZE D CODE CS NUMBER M7957-Ø-1 REV C

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C3 100 pf R21 5.6K +5V

74LS20 E48 — 10, 9, 6, 7, 5, 12, 5, 6, 11 — +3V

74LS04 E72 — 13, 12 — R18 1K +5V — E79 50 NS — R19 1K

D4 LOAD IN PROGRESS L

D5 CLEAR REPLY H

74LS08 E71 — 74LS08 E69 — 74LS08 E23 — D4 LD LPR REGISTER L

+5V — 74LS74 E50

74LS27 E49 — 74LS32 E59

74LS02 E36 — D4 LD TDR REGISTER N

74LS02 E38 — D4 LD BREAK REGISTER N

74LS02 E37 — D4 LD TCR HIGH BYTE N

74LS02 E59 — D4 LD TCR LOW BYTE N

74LS02 E39 — D4 LD CSR HIGH BYTE N

74LS02 E39 — D4 LD CSR LOW BYTE N

74LS02 E38 — D4 READ RCV BUFFER N

74LS21 E41 — 74LS02 E38 — D4 READ DEVICE N

D4 READ L
D4 SELECT Ø2 L
D4 SELECT Ø4 L
D4 SELECT Ø6 L

8881 E40 — 10 AF2 BRPLY L

R20 3.83K C5 220 pf +5V +5V R17 1K

D2 DEVICE SELECT N

74LS04 E72

BSYNC L	AJ2	6	SYNC
D2 DEVICE DATA BUS Ø2		2	DAL 2
D2 DEVICE DATA BUS Ø1		3	DAL 1
D2 DEVICE DATA BUS Ø0		4	DAL Ø
BWTBT L	AK2	5	WTBT
BDOUT L	AE2	9	DOUT
D5 DATA IN L		7	DIN
D5 VECTOR TO BUS H		1	VECTOR

DC005 E12 — ENB, RXCK, BRPLY 8, SEL 6 17, SEL 4 16, SEL 2 15, SEL Ø 14, OUT HB 12, OUT LB 13, INWD 11

(ADDRESS SELECT & DECODE)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	ASYN MUX (D4)	SIZE D	CODE CS	NUMBER M7957-Ø-1
SCALE	SHEET 4 OF 14	DIST		REV. C

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NOTE:
VECTOR ADDRESS IS DETERMINED BY SWITCH PACK E2. SWITCH CLOSED (ON) FOR QBUS LOGICAL ONE (LOW).

R29 330Ω +5V
BIAK I L — AH2 — R11 680Ω

R10 330Ω +5V
AH2 — BIAK O L — R12 680Ω

D12 RECEIVER DONE N — 74LS08 E71 — D11 SILO ALARM H — 74LS32 E59 — DS RECEIVER INTR ENBL

BDIN L — AH2 — BCAD E1 — 74LS04 E48 — D5 DATA IN L

D9 TRANSMITTER READY H
D2 DEVICE DATA BUS Ø6
D2 DEVICE DATA BUS 14

DC ØD3 E11
RQSTA — ENA ST — DS RECEIVER INTR ENBL
BIAKI — BIRQ — AL2 — BIRQ L
BINIT — BIAKO
BDIN — INITO
RQSTB — VECTOR
ENA DAT VEC RQST
ENB DAT ENB ST — DS TRAN INTR ENBL N
ENA CLK — ENB CLK

D4 LD CSR LOW BYTE N
D4 LD CSR HIGH BYTE N

+5V — R30 470Ω — R31 470Ω — D5 VECTOR TO BUS H

E2
E2-1 — D5 VECTOR BIT Ø8 N
E2-2 — D5 VECTOR BIT Ø7 H
E2-3 — D5 VECTOR BIT Ø6 H
E2-4 — D5 VECTOR BIT Ø5 H
E2-5 — D5 VECTOR BIT Ø4 H
E2-6 — D5 VECTOR BIT Ø3 H
D5 VECTOR BIT Ø2 N

+3V — D2 DEVICE DATA BUS 12 — D4 LD CSR HIGH BYTE N — 74LS74 E70 — D5 SILO ALARM ENABLE N — D5 SILO ALARM ENABLE L

74LS175 E52
D2 DEVICE DATA BUS Ø5 — D3 R3(1) — R3(Ø) — D5 MASTER SCAN ENBL H — D5 MASTER SCAN ENBL L
D2 DEVICE DATA BUS Ø4 — D1 R1(1) — R1(Ø)
D2 DEVICE DATA BUS Ø3 — DØ R0(1) — R0(Ø) — D5 MAINTENANCE H
CLR CLK — D4 LD CSR LOW BYTE N

AR2 — AS2
CR2 — WIØ — CS2 — JUMPER INSTALLED ONLY IN M927Ø BACKPLANE.
CM2 — WI1 — CN2 — JUMPER INSTALLED ONLY IN M927Ø BACKPLANE.

C6 680pf — R22 5.6K — +5V — D5 MASTER CLEAR H
MXSC E61 2.9 MXSC
+3V
BINIT L — AT2 — BCAD E1 — 74LS04 E48 — D5 MODEM CLEAR L
D5 CLEAR REPLY N
MXS37 E63 — D5 INITIALIZE N
MXS37 E63 — D5 INITIALIZE L

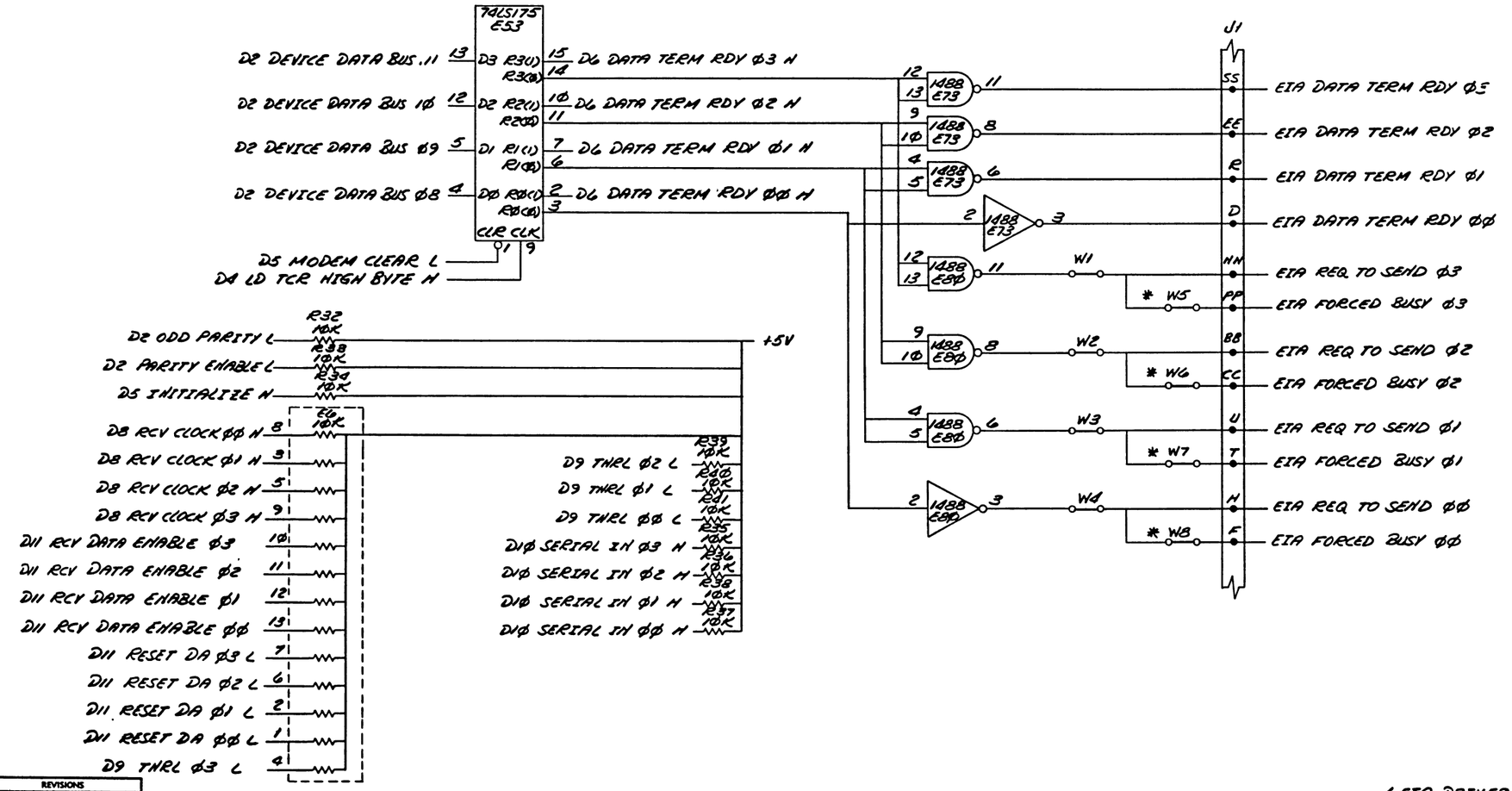
(CSR, INTR, INITIALIZE)

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE	CODE	NUMBER	REV.
ASYN MUX	(D5)	D	CS	M7957-Ø-1	C
SCALE	SHEET 5 OF 14	DIST.			

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NOTE:
* FOR 103E AND 113B MODEMS WITH THE FORCED BUSY OPTION, THIS JUMPER MUST BE INSTALLED TO ALLOW REQUEST TO SEND TO CONTROL FORCED BUSY. (ON = BUSY) IF OPTION IS NOT INSTALLED, REMOVE THIS JUMPER.

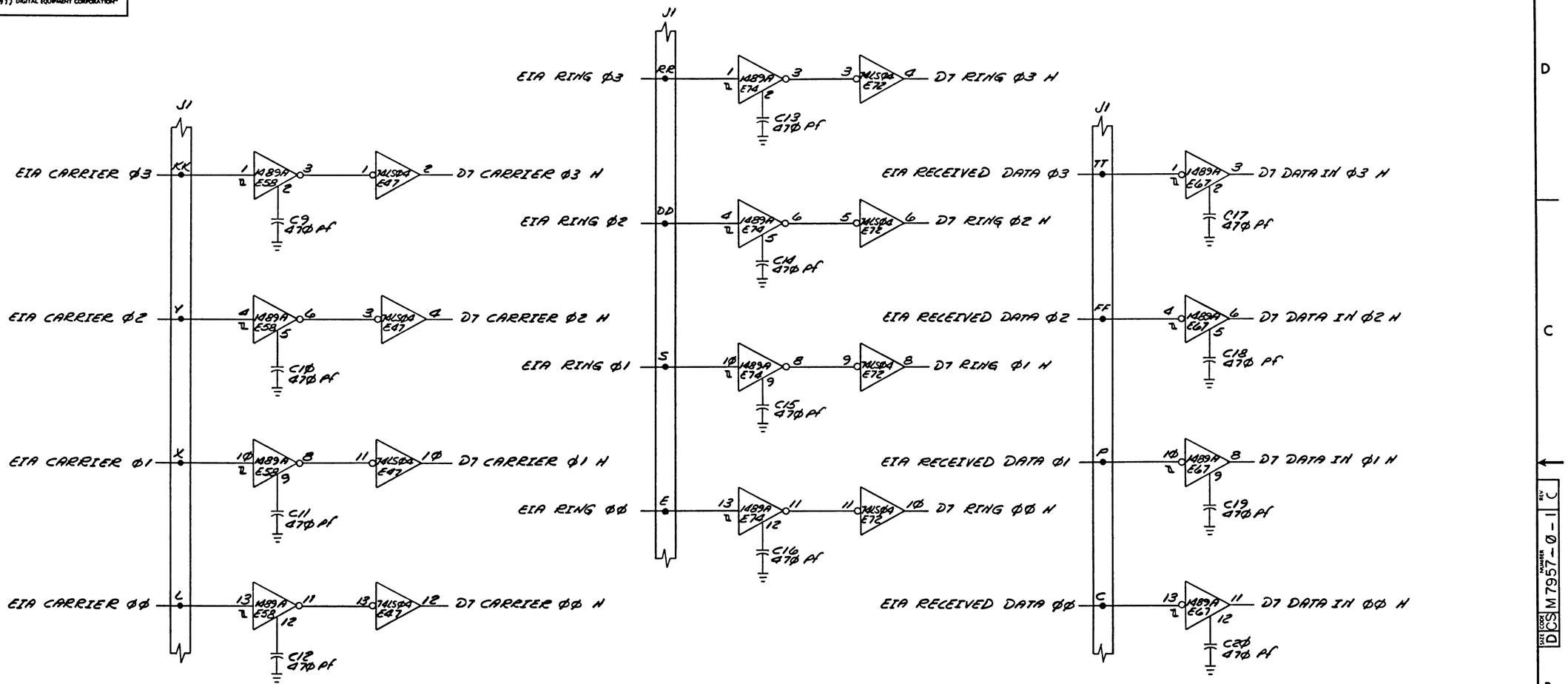


(EIA DRIVER & RECEIVERS)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D6)	D	CS	M7957-0-1	C
SCALE —	SHEET 6 OF 14	DIST.		

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(EIA RECEIVERS)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	ASYN MUX (D7)	SIZE	CODE	NUMBER	REV.
SCALE	SHEET 7 OF 14	D	CS	M7957 - Ø - 1	C
		DIST			

DEC FORM NO. DRD 128

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NOTE:
1. REMOVE JUMPERS FOR AUTOMATED MODULE TEST.

74LS98 E66
SET9
R3(1)
R2(1)
R1(1)
R0(1)
CLK
CLK/8
CLK/16
D8 MASTER SCAN CLOCK
D5 MASTER SCAN ENBL L
+3V
+5V
E78 50/16 MHZ
W9 (SEE NOTE 1)
74LS37 E63
+12V +5V BD2
EXT2 EXT1
D1 C1 B1 A1 D0 C0 B0 A0
F1 F0
50/16 E31
W13 (SEE NOTE 1)
W14 (SEE NOTE 1)
CLK1 CLK2
D8 TX CLOCK Ø0 H
D8 RCV CLOCK Ø0 H
D8 TX CLOCK Ø1 H
D8 RCV CLOCK Ø1 H
74LS259 E34
D2 DEVICE DATA BUS Ø0
D2 DEVICE DATA BUS Ø1
D2 DEVICE DATA BUS Ø2
D2 DEVICE DATA BUS 12
A B C DATA
F0 F1 F2 F3 F4 F5 F6 F7
C̄ Ē
74LS259 - E34

C̄	Ē	F
L	H	CLEAR
H	H	MEMORY
H	L	LATCH

(BD2)
D5 INITIALIZE L
D4 LD LPR REGISTER L
W16 (SEE NOTE 1)
W15 (SEE NOTE 1)
D8 TX CLOCK Ø2 N
D8 RCV CLOCK Ø2 H
D8 TX CLOCK Ø3 N
D8 RCV CLOCK Ø3 N
74LS04 E22d
74LS04 E22c
74LS04 E22b
74LS04 E22a
D2 DEVICE DATA BUS 11
D2 DEVICE DATA BUS 10
D2 DEVICE DATA BUS Ø9
D2 DEVICE DATA BUS Ø8
74LS259 E33
D2 DEVICE DATA BUS Ø0
D2 DEVICE DATA BUS Ø1
D2 DEVICE DATA BUS Ø2
+3V
D8 CONTROL STROBE Ø0 N
D8 CONTROL STROBE Ø1 N
D8 CONTROL STROBE Ø2 N
D8 CONTROL STROBE Ø3 N
D4 LD LPR REGISTER L
74LS259 - E33

C̄	Ē	F
L	H	CLEAR
L	L	DEMUX

(CLOCKS & PARAMETER STROBE)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
ASYN MUX (D8)	D	CS	M7957-0-1	C
SCALE —	SHEET 8 OF 14	DIST		

DEC FORM NO. DRD 138

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NOTE:
1. REMOVE JUMPER FOR AUTOMATED MODULE TEST.

D13 TBMT Ø0
D13 TBMT Ø1
D14 TBMT Ø2
D14 TBMT Ø3

D2 DEVICE DATA BUS Ø0
D2 DEVICE DATA BUS Ø1
D2 DEVICE DATA BUS Ø2
D2 DEVICE DATA BUS Ø3

D5 INITIALIZE L
D4 LD TCR LOW BYTE H

D9 TRANSMITTER LINE B
D9 TRANSMITTER LINE A
D9 TRANSMITTER READY H

D5 MASTER SCAN ENBL H
D5 MASTER SCAN ENBL L

D9 TCR LINE Ø0 H
D9 TCR LINE Ø1 H
D9 TCR LINE Ø2 H
D9 TCR LINE Ø3 H

D4 LOAD IN PROGRESS L
D4 LD TDR REGISTER H

D9 TNRL Ø3 L
D9 TNRL Ø2 L
D9 TNRL Ø1 L
D9 TNRL Ø0 L

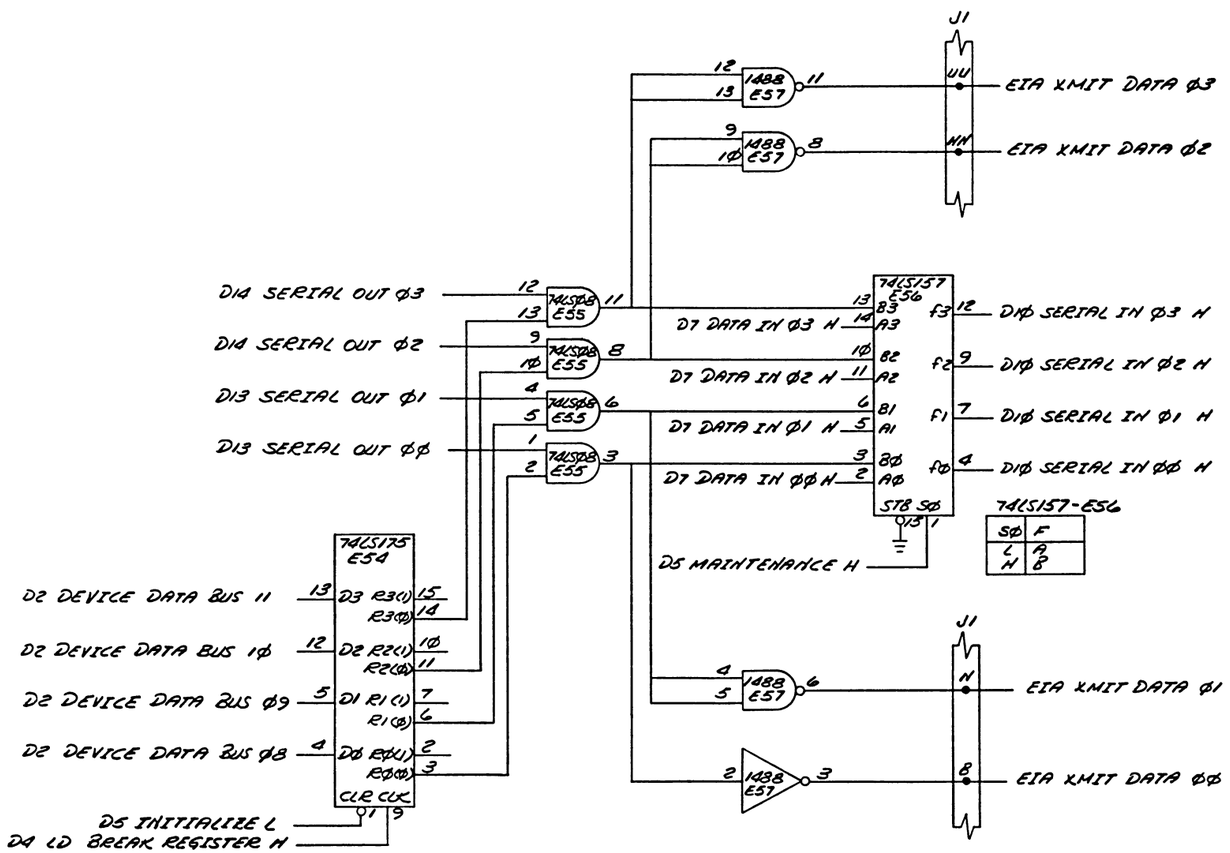
W12 (SEE NOTE 1)

(TRANSMITTER CONTROL)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D9)	D	CS	M7957-0-1	C
SCALE —	SHEET 9 OF 14	DIST.		

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(BREAK, TRANSMIT DATA, MAINTENANCE)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (DIØ)	D	CS	M7957-Ø-1	C
SCALE	SHEET 10 OF 14	DIST.		

DEC FORM NO. DRD 138

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D11 PHASE TWO N
D11 PHASE ONE N
(PHASE THREE)
74LS175 E65
D5 MASTER SCAN ENBL N
D8 MASTER SCAN CLOCK N
74LS193 E36
+3V
D11 RCV SCAN LEAD B
D11 RCV SCAN LEAD A
74LS155 E76
D11 RCV DATA ENABLE Ø3
D11 RCV DATA ENABLE Ø2
D11 RCV DATA ENABLE Ø1
D11 RCV DATA ENABLE ØØ
D11 RESET DA Ø3 L
D11 RESET DA Ø2 L
D11 RESET DA Ø1 L
D11 RESET DA ØØ L
D11 SILO ALARM H
74LS74 E62
74LS193 E68
D12 SILO LOAD REQUEST H
D11 LOAD SILO N
74LS08 E71
D4 READ RCV BUFFER H
D5 SILO ALARM ENABLE L
74LS32 E59
74LS04 E49
(RECEIVER CONTROL)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (DII)	D	CS	M7957-Ø-1	C
SCALE	SHEET 11 OF 14	DIST.		

DEC FORM NO. DRD 130

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DCSM7959-0-1 REV C

DI3 FE Ø0
DI3 FE Ø1
DI4 FE Ø2
DI4 FE Ø3
DI3 OR Ø0
DI3 OR Ø1
DI4 OR Ø2
DI4 OR Ø3
74LS153 E9
DI1 RCV SCAN LEAD B
DI1 RCV SCAN LEAD A

DI3 DA Ø0
DI3 DA Ø1
DI4 DA Ø2
DI4 DA Ø3
DI3 PE Ø0
DI3 PE Ø1
DI4 PE Ø2
DI4 PE Ø3
74LS153 E10

74LS21 E28
74LS11 E64
DI2 SILO LOAD REQUEST H

3341 E18
DI2 PARITY ERROR
DI2 FRAMING ERROR
DI2 OVERRUN ERROR

3341 E27
DI2 RECEIVE LINE A
DI2 RECEIVE LINE B

3341 E17
DI3 RD5
DI3 RD6
DI3 RD7
DI4 RD8
DI2 RCV DATA Ø4
DI2 RCV DATA Ø5
DI2 RCV DATA Ø6
DI2 RCV DATA Ø7

3341 E35
DI3 RD1
DI3 RD2
DI3 RD3
DI3 RD4
DI2 RCV DATA Ø0
DI2 RCV DATA Ø1
DI2 RCV DATA Ø2
DI2 RCV DATA Ø3

D5 MASTER SCAN ENBL H
D2 -12VA
D2 -12VB
DI1 LOAD SILO H

DI4 READ RCV BUFFER H

74LS21 E28
DI2 RECEIVER DONE H
DI2 VALID DATA H
74LS74 E70
D5 INITIALIZE L

+5V
R216 5.6K
C2 50pF
+3V
74LS20 E41
DI2 UNLOAD SILO H

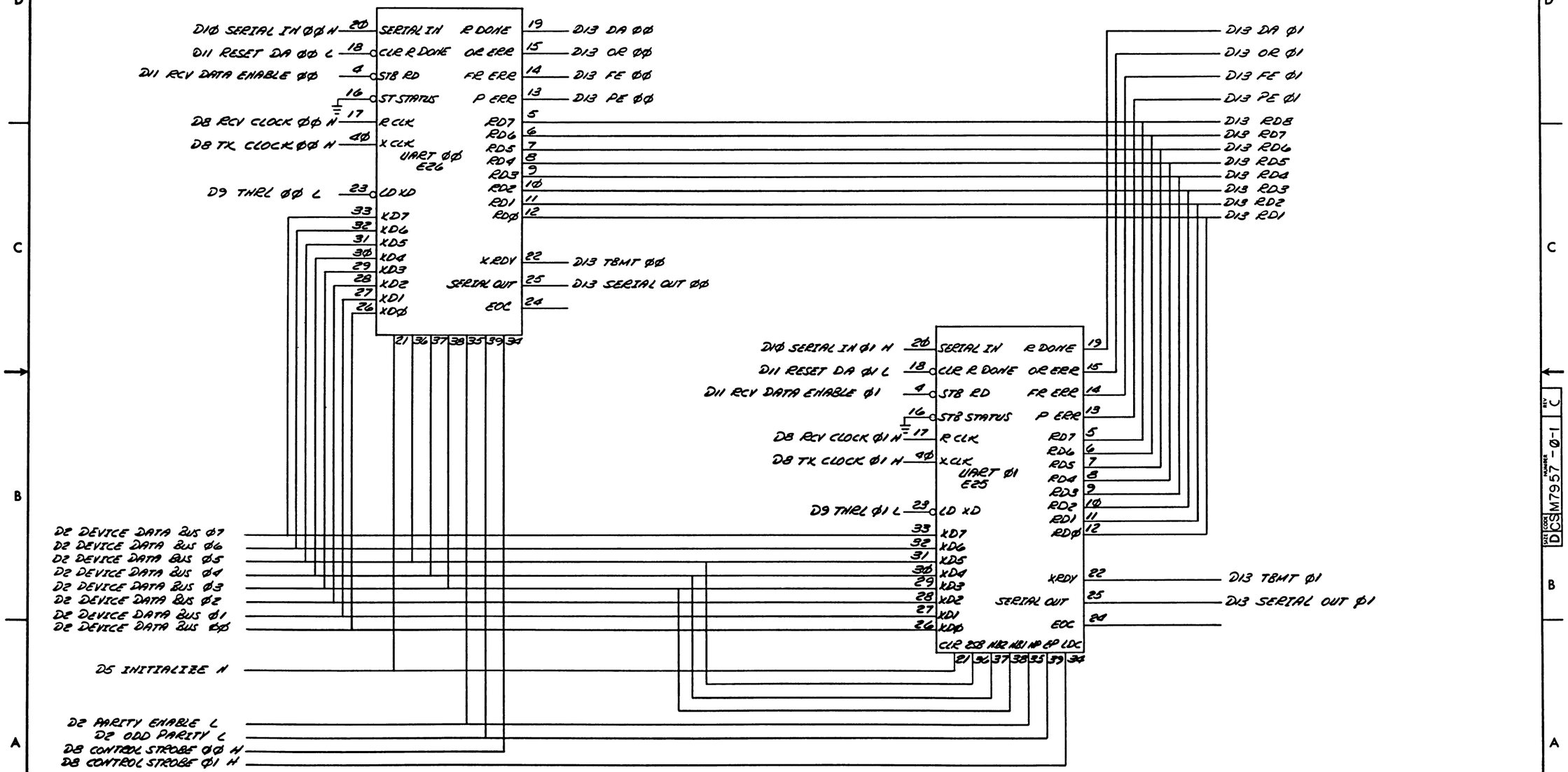
(SILO BUFFERS AND UNLOAD CONTROL)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	ASYN MUX (DI2)	SIZE	CODE	NUMBER / REV.
		D	CS	M7957-0-1 C
SCALE	—	SHEET 12 OF 18	DIST.	

DEC FORM NO. BRD 130

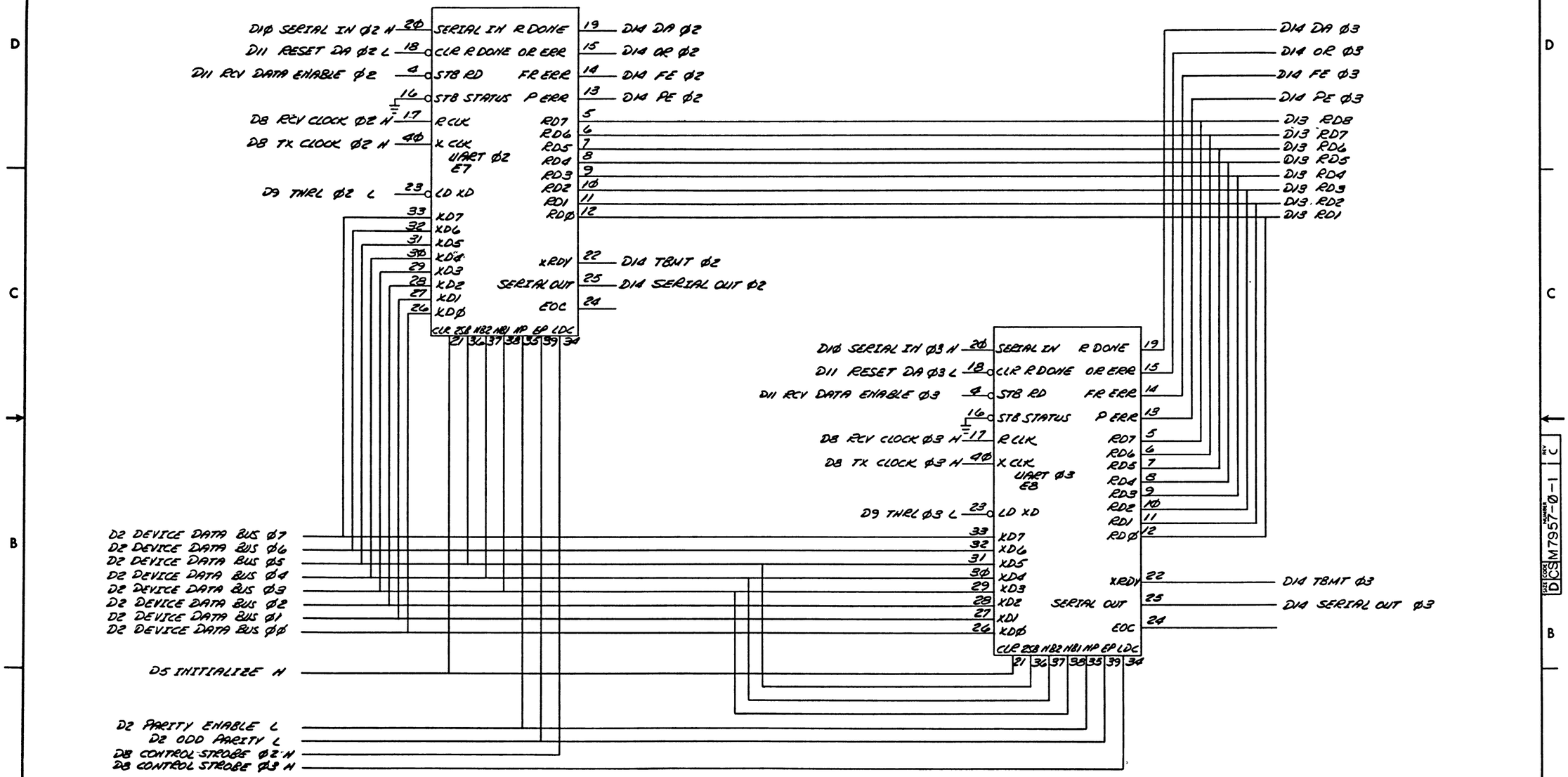
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	ASYN MUX (D13)	SIZE	CODE	NUMBER	REV.
SCALE —/—	SHEET 13 OF 14	D	CS	M7957-0-1	C
		DIST.			

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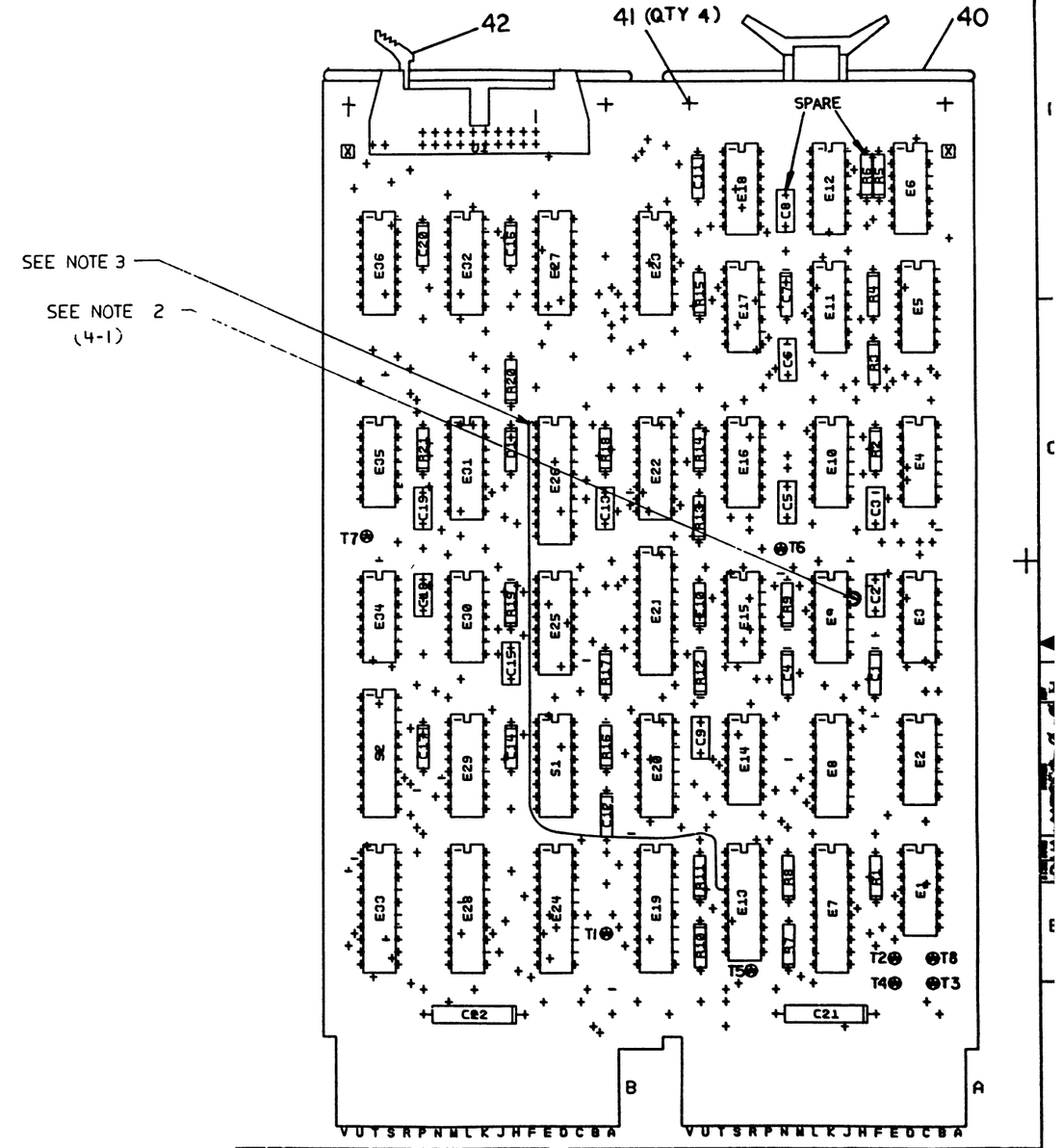


(UARTS Ø2 & Ø3)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	ASYN MUX (D14)	SIZE	CODE	NUMBER	REV.
		D	CS	M7957-0-1	C
SCALE	SHEET 14 OF 14	DIST.			

DEC FORM NO. BRD 135



NOTES: 1: REMOVE THE FOLLOWING UNUSED FINGERS FROM ARTWORK: ABJ, ACJ, ADJ, AEJ, AFJ, AHJ, AKJ, ALJ, ANJ, APJ, ABJ, ASJ, AUJ, BCJ, BDJ, BEJ, BFJ, BHJ, BKJ, BLJ, BNJ, BPJ, BRJ, BSJ, BUJ.
2. (4-1): WIRE ADDED (SIDE 1) E9 PIN 9 TO E9 PIN 10.
NOTE 3: (5-1) WIRE ADDED SIDE ONE FROM E13-4 TO E26-1. WIRE PATH NOT CRITICAL.

CH	CHA.	GE	ECO	REV
	M7954-2			D
		C. LAU		
	M7954-ABOSA			E
	M7954-ABOSA			F
	M7954-ABOOF			H
		J.M. CURTIS		

ETCH REV. D
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE
DRN.	4/6/72
CHK'D	5/11/72
ENG.	11/21/72
PROJ. ENG.	5/11/72
PROD.	5/11/72

SCALE 2/1
SHT. 1 OF 1
NEXT HIGHER ASSY. 8-DD-M7954-0

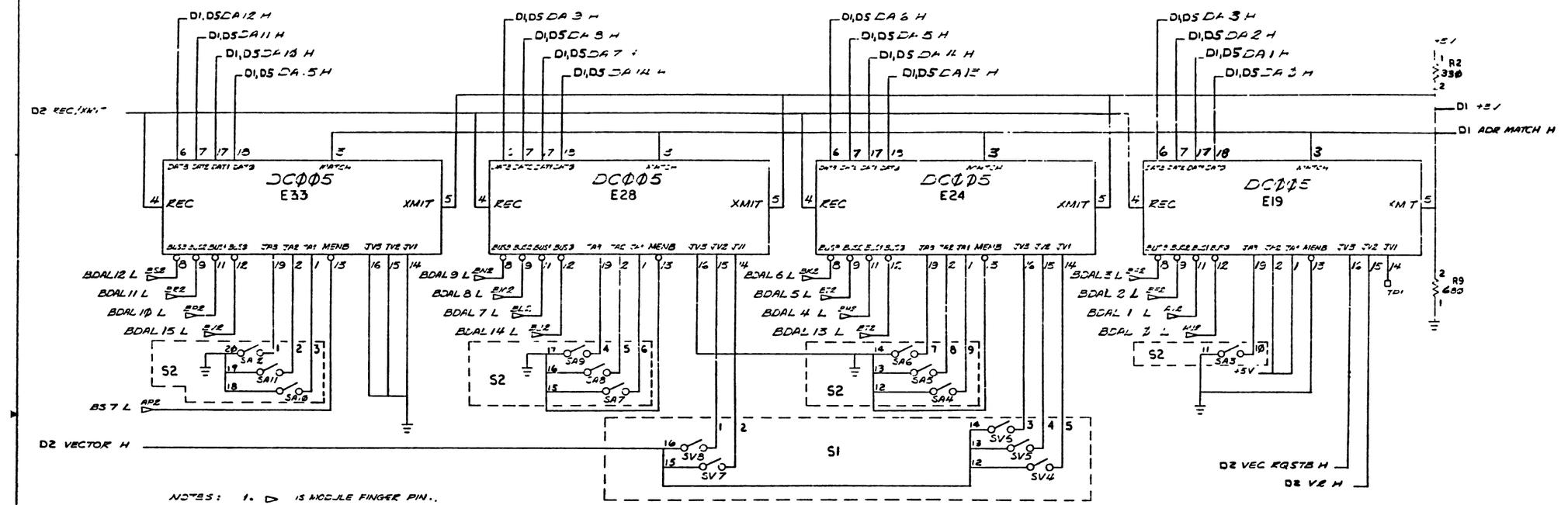
digital

TITLE
LSI INTERFACE

SIZE D | CODE UA | NUMBER M7954-0 | REV H

MS#

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NOTES:

1. ▷ IS MODULE FINGER PIN.
2. ON THIS AND THE FOLLOWING PAGES, ALL RESISTORS ARE 1/4 W, 5% UNLESS INDICATED OTHERWISE.
3. SELECTABLE REGISTER ADDRESS RANGE: 160300 - 177776. SET AT 160150 FOR PRODUCTION TESTING AND SHIPPING.
4. SELECTABLE VECTOR ADDRESS RANGE: 000 — 760
5. SV SWITCHES
 SVi DRIVES BDALi. BDALi IS LOW WHEN SVi IS CLOSED
 i=4,5,...,8
6. SA SWITCHES. i=3,4,...,11,12
 a) SAi IS COMPARED WITH BDALi. CLOSING SWITCH IS EQUAL TO "LOW" ON THE BUS.
 b) ADR MATCH IS HIGH WHEN ALL SAi'S ARE EQUAL TO ALL BDALi'S.
7. DATA MODES:

REC	XMIT	MODES
L	L	DISABLE: BUS, DAT ARE OPEN.
L	H	DAT→BUS
H	L	BUS→DAT
H	H	BUS→DAT. VECTOR ADDRESS TRANSMITTED WHEN REQUIRED.

AA2, BA2 +5V — C21 — C22 — AJ1, AM1, AT1, BJ1, BM1, BT1, AC2, BC2

ADDRESS SWITCH (S2) SETTING FOR TESTING : 160150

	1	2	3	4	5	6	7	8	9	10
S2							ON	ON		ON
	OFF	OFF	OFF	OFF	OFF	OFF			OFF	
	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3

VECTOR SWITCH (S1) SETTING FOR TESTING : 42 X

	1	2	3	4	5	6	7	8*
S1	ON				ON			
		OFF	OFF	OFF		OFF	OFF	OFF
	SV8	SV7	SV6	SV5	SV4			

* ERI INH SWITCH ON SHEET 3.

LSI/1 BUS INTERFACE

NOTES:

CHK	CHANGE NO	REV
GP	M7954-00001	C
	D. Lau Mar 77	
	C. LAU	
GP	CHANGE NO M7954-2	D
QD	M7954-3	
	C. LAU	
	C. Lau 29 Aug 77	E
RR	M7954-4	
	J. CURTIS	
	M7954-4 BOOK	F
	R SALETT	
RR	M7954-5 BOOT	H
	J.M.CURTIS	
RR	M7954-6 BOOT	J

SIGNATURES	DATE
DRN. M Cyrulnik	29 Sept 76
CHK'D R Salett	2/14/77
ENG.	2/11/77
PROJ. ENG.	2/11/77
PROD.	2/14/77
SCALE —	
SHT. 1 OF 7	
ETCH REV	FIRST USED ON IBVII-A

digital

TITLE LSII/IB INTERFACE D1

SIZE	CODE	NUMBER	REV
D	CS	M7954-0-1	H

1 MS#

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BDMGI L — AR2 — 452 — BDMGO L

-5V — R1 1K

BSYNC L — AJ2 — BRPLY L

D1, D5 DA0 H
D1, D5 DA1 H
D1, D5 DA2 H
D1 ADR MATCH H
BWTBT L — AK2
BCOUT L — AE2

DC004 E7 (RXCX): BCAO, BCA1, BCA2, ENB, BWTBT, BDOUT, BDIN, VECTOR; SEL0, SEL2, SEL4, SEL6, OUTHB, OUTLB, INWD; TP2, TP3, TP4

7437 E2

LS02 E1 ×3

D2 DA→IBS LB H
D2 DA→IBD LB H
D2 SEL 2 L
D2 READ H
D2 REC/XMIT

BCIN L — AH2 — 8837 E8 ×2

D1, D5 DA6 H

R10 680 — R11 330 — +5V

BIAKI L — AM2
BINIT L — AT2

DC003 E13: RQSTA, ENA DATA, ENA CLK, BIAKI, BINIT, BDIN, RQSTB, ENB DATA, ENB CLK; ENA ST A, BIRQ, BIAKO, INITO, VECTOR, VEC RQSTB, ENB ST B; TP5

R7 680 — R8 330 — +5V

BIRQ L — AL2
BIAKO L — AN2
D2 IE H
D2 INIT L
D2 VECTOR H
D2 VEC RQSTB H

D4 CMD H
D4 TKR H
D4 LNR H

LS27 E9 — 8837 E8

R4 20K — R3 22K — +5V
C2 100 pf
R5 22K — +5V

D4 ER2 H
D3 ER1 H

LS27 E9 — LS00 E18 — LS00 E12 — LS04 E16

LS00 E14 — LS08 E12 — LS00 E14

D2 V2 H

D6 REC SRQ H — LS00 E18 — LS04 E16

INTERRUPT PRIORITY	VECTOR ADDRESS	VEC RQSTB JV3	V2 JV2
ERR	XXX*	L	L
SRQ	XXX+4	L	H
CMD, TKR	XXX+10	H	L
LNR	XXX+14	H	H

* 000 ≤ XXX ≤ 760

REC SRQ H
ER2 H
E12 - 9
E13 - 17 — ~ 500 ns

REG SEL AND INTR

D2

REVISIONS

CHK	CHANGE NO.	REV

TITLE: LSI11/IB INTERFACE
SIZE D | CODE CS | NUMBER M7954-0-1 | REV. B
SCALE — | SHEET 2 OF 7 | DIST.

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D1,D5 DA15 H
D1,D5 DA7 H
D1,D5 DA5 H
D1,D5 DA4 H
D1,D5 DA2 H
D1,D5 DA1 H
D1,D5 DA3 H
D2 DA-IES LB H
D2 INIT L
D1,D5 DA0 H
D6 REC DAV H
D6 REC ATN H
D6 REC IFC H
D6 REC REN H

LS273 E21: CLR, 6D, SRQ,6Q, 1D, ACC,1Q, 2D, TCN,2Q, 3D, LON,3Q, 4D, REM,4Q, 5D, EOP,5Q, 7D, IBC,7Q, CK

D3 ERI INH L
LS00 E14
LS02 E4
D3 ASRT SRQ H
D3 ACC H
D3 TCN H
D3 LON H
D3 REM H
D3 EOP H

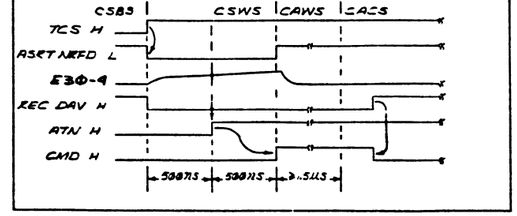
C13 .01 uf
R18 1.39K
+5V
D1 1N664
R12 6.8K
LS123 E31 TBC 74S123 CLR
7417 E30 OC
C9 1200 PF
8837 E8
7437 E2
D3 IBC H
D3 TCS H

LS74 E11
LS02 E4
LS02 E5
D1 +3V
LS74 E11 ATN
D3 ATN H
D3 ASRT NRFD L
LS04 E16
LS132 E10
LS02 E5
LS00 E18
LS10 E12
7417 E30 OC
R19 3.3K
+5V
~500 NS
R20 1K
+5V
8242 E17 OC
7417 E30 OC
R14 3.3K
+5V
~500 NS
LS132 E10
C5 470 PF
C18 470 PF
LS02 E35
D3 ERI H
D3 ERI INH L
R16 3.3K
+5V
R15 3.9K
+5V
8242 E17 OC
C6 470 Pf
S1
ERI INH SW (SEE NOTE)
LS132 E10
~500 NS

NOTE:

SWITCH	ERI DETECTION
CLOSE	INHIBITS
OPEN	ENABLES

TAKE CONTROL SYCHRONOUSLY TIMING DIAGRAM



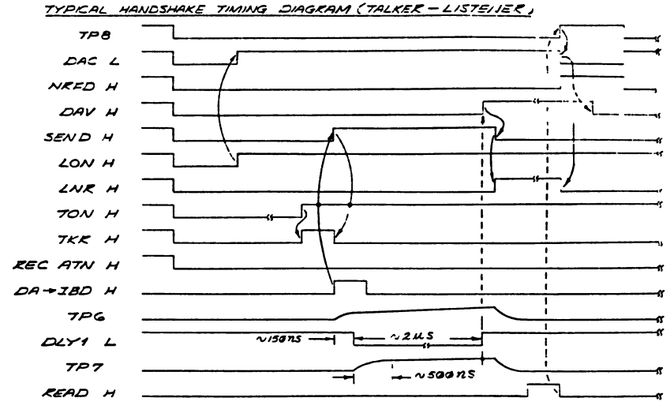
CONTROL AND STATUS
D3

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: LSI11/IB INTERFACE
SIZE D | CODE CS | NUMBER M7954-0-1 | REV. H
SCALE | SHEET 3 OF 7 | DIST.

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TYPICAL HANDSHAKE TIMING DIAGRAM (TALKER – LISTENER)



REVISIONS		
CHK	CHANGE NO.	REV.

CONTROL AND HANDSHAKE D4

TITLE	SIZE	CODE	NUMBER	REV.
LSI11/IB INTERFACE	D	CS	M7954-Ø-1	H
SCALE —	SHEET 4 OF 7		DIST.	

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D2 INIT L

D1,D5 DA Ø H

D1,D5 DA 1 H

D1,D5 DA 2 H

D1,D5 DA E H

D1,D5 DA 4 H

D1,D5 DA 5 H

D1,D5 DA 6 H

D1,D5 DA 7 H

D4 BUF CLK H

LS273 E26

D5 DIO 1 H

D5 DIO 2 H

D5 DIO 3 H

D5 DIO 4 H

D5 DIO 5 H

D5 DIO 6 H

D5 DIO 7 H

D5 DIO 8 H

D4 REC DAC H

D6 REC DAV H

D4 REC RFD H

D6 REC SRQ H

D6 REC REN H

D6 REC IFC H

D6 REC ATN H

D6 REC EOI H

D2 REC/XMIT

D2 SEL2 L

D6 REC DIO1 H

D3 TCS H

D6 REC DIO2 H

D3 EOP H

D6 REC DIO3 H

D3 REM H

D6 REC DIO4 H

D3 IBC H

74LS257 E22

D1,D5 DA Ø H

D1,D5 DA 1 H

D1,D5 DA 2 H

D1,D5 DA 3 H

D6 REC DIO5 H

D3 LON H

D6 REC DIO6 H

D3 TON H

D6 REC DIO7 H

D2 IE H

D6 REC DIO8 H

D3 ACC H

74LS257 E25

D1,D5 DA 4 H

D1,D5 DA 5 H

D1,D5 DA 6 H

D1,D5 DA 7 H

D4 LNR H

D4 TKR H

D4 CMD H

74LS257 E20

D1,D5 DA 8 H

D1,D5 DA 9 H

D1,D5 DA 10 H

D1,D5 DA 11 H

D3 ER1 H

D4 ER2 H

74LS257 E29

D1,D5 DA 12 H

D1,D5 DA 13 H

D1,D5 DA 14 H

D1,D5 DA 15 H

74LS257 TRUTH TABLE

SE, S	A, B	Y	
H	X	X	HIGH IMP
L	L	L	DATA
L	H	H	DATA
↓	L	L	START
↓	H	H	START

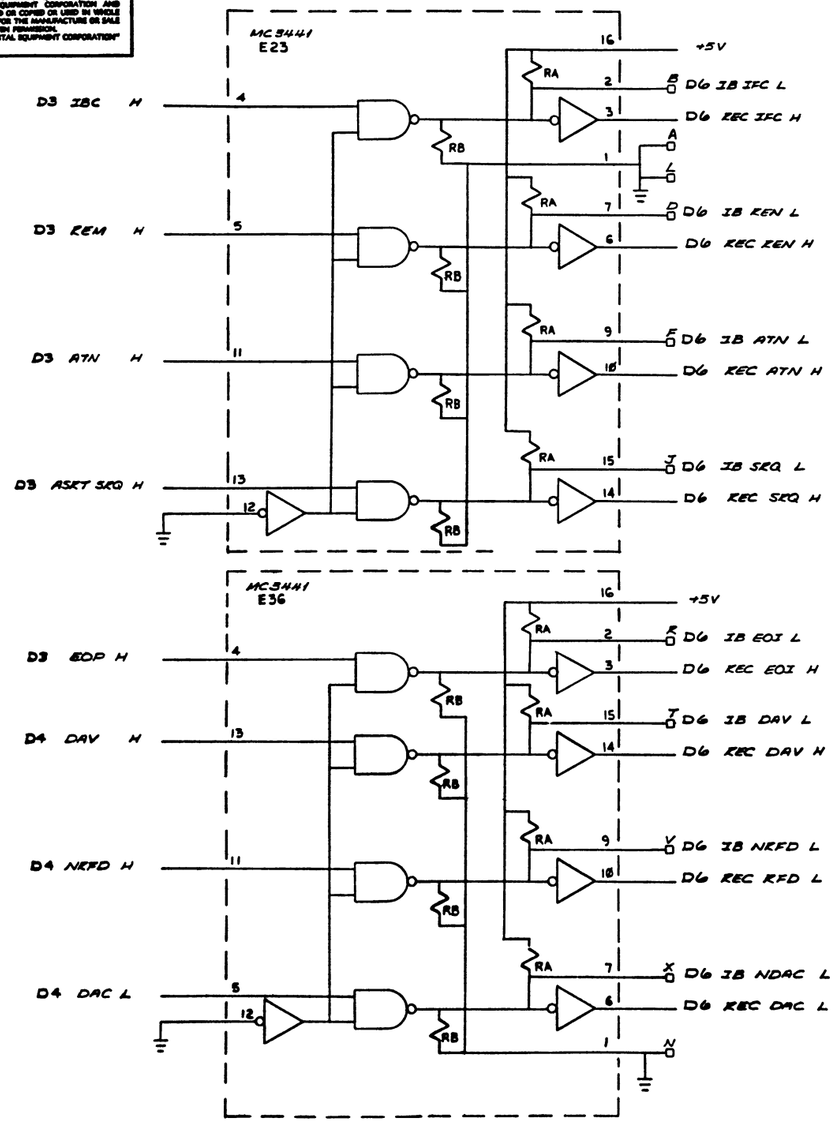
REVISIONS		
CHK	CHANGE NO.	REV.

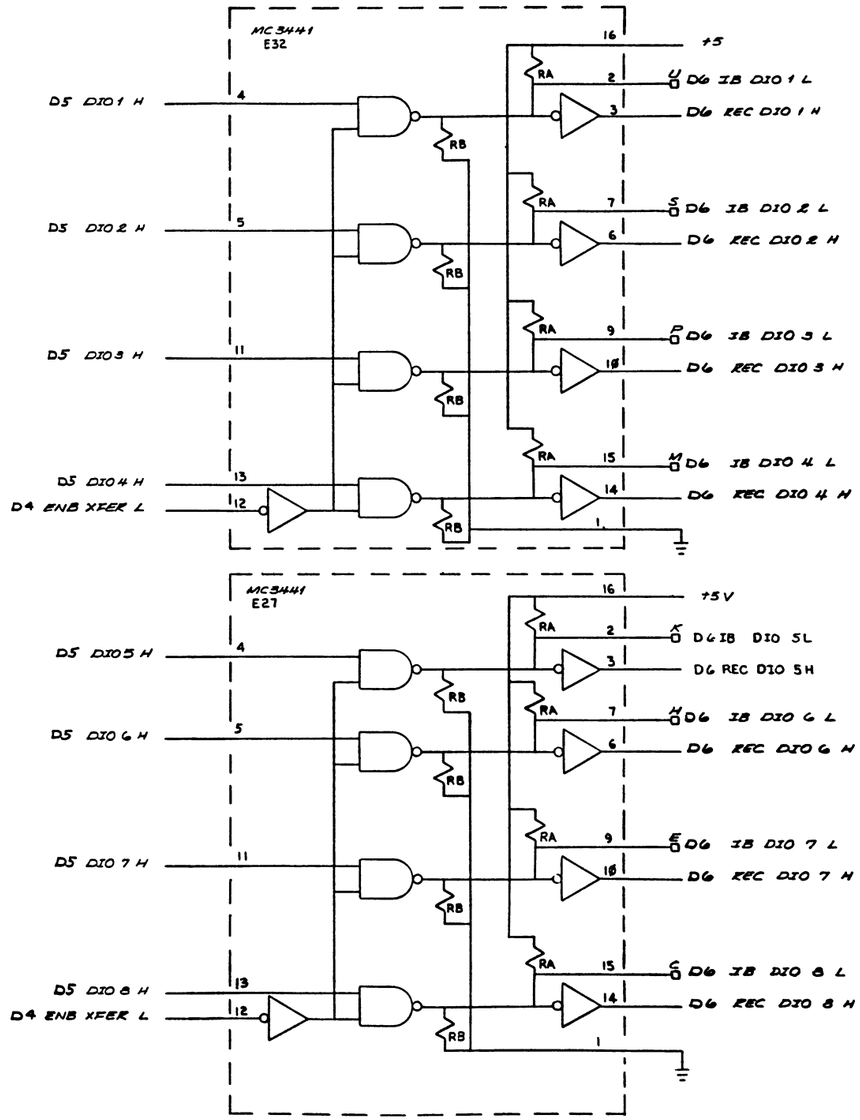
DATA/STAT MUX D5

TITLE LSI11/IB INTERFACE | SIZE D | CODE CS | NUMBER M7954-Ø-1 | REV. B

SCALE — | SHEET 5 OF 7 | DIST.

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NOTES: 1. RA = 8.0 KΩ, INTERNAL RESISTOR.
2. RB = 6.2 KΩ, INTERNAL RESISTOR.
3. —O IS A BERG CONNECTOR PIN.

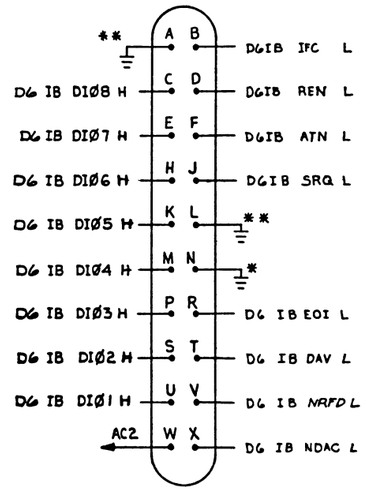
REVISIONS		
CHR	CHANGE NO.	REV.

INSTRUMENT BUS INTERFACE D6

TITLE	SIZE	CODE	NUMBER	REV.
LSI11/IB INTERFACE	D	CS	M7954-0-1	H
SCALE —	SHEET 6 OF 7		DIST.	

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NOTES:
1. (*) TERMINATION GROUND (PIN 1) OF DRIVER FOR EOI, DAV, NRFD & NDAC SIGNALS.
2. (**) TERMINATION GROUND (PIN 1) OF DRIVER FOR IFC, REN, ATN & SRQ SIGNALS.



CABLE CONNECTOR PIN ASSIGNMENT

D7

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 / IB INTERFACE	D	CS	M7954-Ø-1	
SCALE	SHEET 7 OF 7	DIST.		

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NOTES:

NOTES:

1. ~~ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57 PIN 6 IS 2.5 MHZ MIN TO 2.63 MHZ MAX. THE MODULE MAY BE OPERATED AT OTHER FREQUENCIES FOR TEST PURPOSE ONLY. SEE SHEET (K-9) MANUFACTURING ADJUSTS TO 2.59 MIN TO 2.63 MAX.~~
2. ADJUST R15 SO THAT THE REFRESH FREQUENCY MEASURED AT E78 PIN 8 IS 625 HZ ± 20 HZ. SEE SHEET (K-9).
3. TIME DELAY FROM FALLING EDGE ON E51 PIN 9 TO FALLING EDGE ON E76 PIN 4 SHOULD BE 110 TO 140 NS. R7 MAY BE REMOVED TO INCREASE THE DELAY SLIGHTLY IF LESS THAN 110 NS IS MEASURED SEE SHEET (K 9).
4. JUMPER FUNCTIONS AND CONFIGURATION ARE AS FOLLOWS

JUMPER SELECT FEATURES				
JUMPER	SELECTION WHEN INSTALLED	OPTION	SHIPPING STATUS M7264(REV E)	-YA
W1	RESIDENT MEMORY BANK 1	C.O.	R	R
W2	RESIDENT MEMORY BANK 0	C O	I	R
W3	DISABLE EVENT LINE	C.O.	R	R
W4	DISABLE MEMORY REFRESH	C O	R	I
W5	POWER UP MODE SELECT	C.O.	R	R
W6	POWER UP MODE SELECT	C O.	R	R
W7	BIASING VOLTAGE VDATA = VROM	F O.	I	I
W8	BIASING VOLTAGE VCTL = VROM	F O.	I	I
W9	DISABLE REPLY FROM RESIDENT MEMORY	F.O.	R	I
W10	DISABLE REPLY DURING REFRESH *	C O.	R	R
W11	ENABLE ON BOARD MEMORY SELECT	C.O.	I	R

* INSTALLED IF RESIDENT RAM IS NOT THE SLOWEST REPLY IN THE SYSTEM.

POWER-UP MODES			
MODE	JUMPERS W6	JUMPERS W5	MODE SELECT
0	R	R	PC AT 24 AND PS AT 26, OR HALT MODE
1	R	I	ODT MICROCODE
2	I	R	PC AT 173000 FOR USER BOOT STRAP
3	I	I	MICRO ADDRESS 3000 2

I; INSTALLED R; REMOVED C.O; CUSTOMER OPTION F.O; FACTORY OPTION

4K RAM	16	9	8
DEC MH8026	3		
DEC 75322	7	14	
DEC 7497	8	16	
DEC 8641	8	16	
DEC 74S257	8	16	
DEC 74S174	8	16	
DEC 74S140	7	14	
DEC 74S139	8	16	
DEC 7475	12	5	
DEC 74S74	7	14	
DEC 7474	7	14	
DEC 7442	8	16	
DEC 74S11	7	14	
DEC 74S10	7	14	
DEC 8837	8	16	
DEC 74S05	7	14	
DEC 74S04	7	14	
DEC 74S00	7	14	
DEC 7400	7	14	
IC TYPE	GND	+5V	+12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

5. COMPONENTS ARE NOT INSTALLED (RESERVED OPTION) UNLESS SPECIFICALLY INSTRUCTED
6. DELETED FOR M7264 YA VERSION

M7264	~~+5 V FOR 1ST CHIP SET, +5 V FOR MOSTEK WE RAM~~
M7264-YA	~~+5 V FOR 1ST CHIP SET, NO ON BOARD RAM~~
M7264-BB	~~+5 V FOR 1ST CHIP SET, +5 V FOR INTEL WE RAM~~
M7264-JB	~~SAME AS M7264 EXCEPT E50, 64 & 70~~
M7264-YB	~~SAME AS M7264-YA EXCEPT E50, 64 & 70~~

8 SIGNAL DESIGNATION: XX YYY Z — XX: SIGNAL ORIGIN (PAGE) IDENTIFIER; YYY: SIGNAL NAME; Z: H (HIGH), L (LOW) WHEN ASSERTED

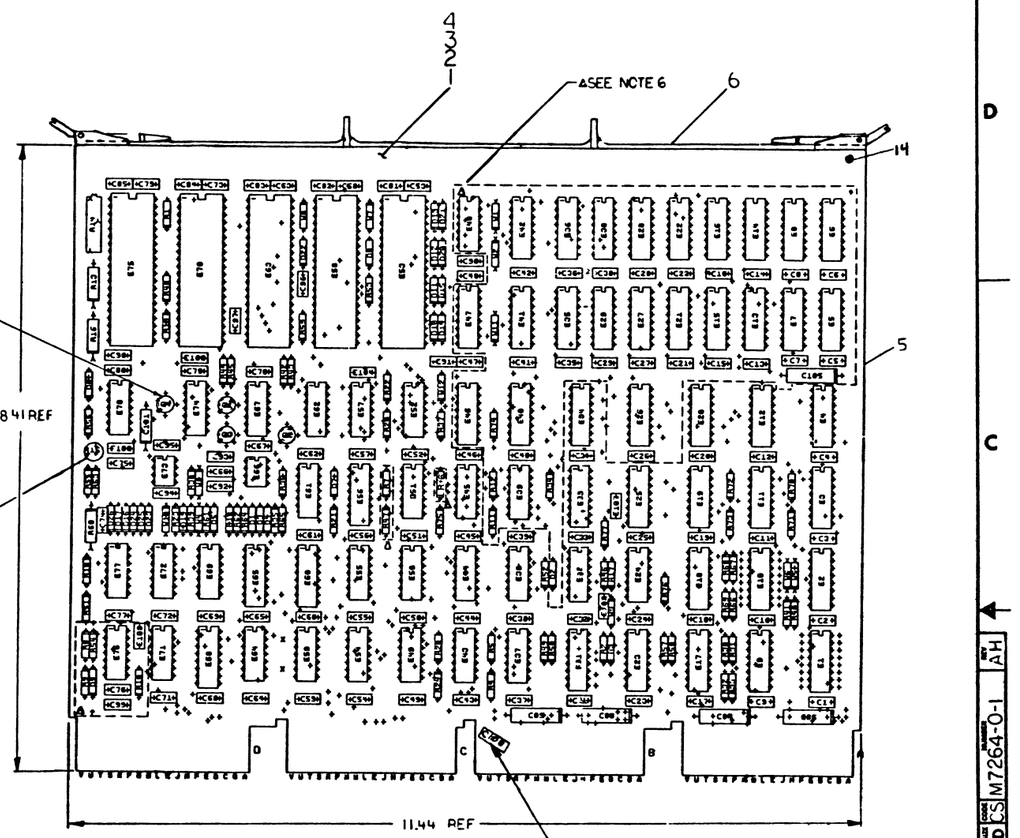
9.

ALTERNATE PARTS CHART		
ITEM*	PREFERRED PART	ALTERNATE PART
6	1213113-01	7413826-00 AND -01
21, 22	1001610-00	1001510-01
9, 10	9009149-01	9009149

10 THE 23Ø2B6 IS AN ALLOWABLE SUBSTITUTION FOR THE 23Ø3B6 ON THE M7264 BB AND M7264-YB. THE 23Ø3B6 IS PREFERRED.

VARIATION CHART	
VARIATION	DESCRIPTION
M7264-AA	M7264 OR M7264-AB,CB,DB,EB,FB,HB,JB
M7264	PROCESSOR W MOSTEK 4096
M7264-AB	PROCESSOR W INTEL 2104
M7264-BB	PROCESSOR W MOSTEK 4097 AND HYBRID MICROM
M7264-CB	PROCESSOR W FUJITSU 8224
M7264-DB	PROCESSOR W INTEL 2104A
M7264-EB	PROCESSOR W MOSTEK 4027
M7264-FB	PROCESSOR W DEC 4027
M7264-HB	PROCESSOR W MOTOROLA 4027
M7264-JB	PROCESSOR W FUJITSU 8227
M7264-YA	PROCESSOR W NO MOS RAM CS REV W OR LOWER
M7264-YB	PROCESSOR W NO MOS RAM AND HYBRID MICROM
M7264-YC	PROCESSOR W NO MOS RAM CS REV AA OR HIGHER

11. FOR VARIATIONS - BB AND YB ONLY, ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57, PIN 6 IS 2.450 MHZ MIN. TO 2.490 MHZ MAX. FOR ALL OTHER VARIATIONS ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57, PIN 6 IS 2.591 MHZ MIN. TO 2.631 MHZ MAX. SEE SHEET K-9. THE MODULE MAY BE OPERATED AT OTHER FREQUENCIES FOR TEST PURPOSES ONLY.
12. ADD A 01 pfd CAPACITOR BETWEEN FINGER BR1 AND THE FEED THRU HOLE CONNECTED TO FINGER BT1
13. ADD TRANSIPAD, DEC P/N 9007201-00, TO EACH TRANSISTOR, REF DESIGNATORS Q1-Q4



4. PLACE TRANSISTOR IN ACCORDANCE TO VEDOR PART USED.

A5T4260 B-C-E A8T4260 B-C-E

NOTE: FOR PARTS LIST, SEE K-PL-M7264-Ø-DBP

PARTS LIST				
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
		M7264-ML024		AE
		M7264-ML025		AF
		M7264-ML026		AH

FIRST USED ON OPTION MODEL: KDII-F

ETCH BOARD REV: H

SEMICONDUCTOR CONVERSION CHART			
DEC NO.	EIA NO.	J/C NO.	EIA NO.

REVISED	CHANGE NO.	REVISIONS
M7264-00005	V	
M7264-00006	W	
M7264-00007	Y	
M7264-00008	J	
M7264-00009	N	
M7264-00010	P	
M7264-00011	R	
M7264-00012	S	
M7264-00013	T	
M7264-00014	U	
M7264-00015	V	
M7264-00016	W	
M7264-00017	Y	
M7264-00019	Z	
M7264-00020	AA	
M7264-00021	AB	
M7264-ML022	AC	
M7264-ML023	AD	

ORN	Linda Peterson	DATE 19 Nov 76
CHKD	D Maloney	DATE 19 Nov 76
ENG	Chuck S. Chi	DATE 11-22-76
PROJ ENG	Ed Pierson	DATE 11-30-76
PROD	Chuck S. Chi	DATE 11-24-76

NEXT HIGHER ASSY: B-DD-M7264-0

SCALE: —

SHEET 1 OF 9

digital

TITLE: LSI-11 CPU MODULE

SIZE D | CODE CS | NUMBER M7264-0-1 | REV AH

DIST.

M7264-0-1 AH

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PREFIX "K2" APPLIES TO ALL WDAL, WMIB } SIGNALS

K9 -VDATA (SEE NOTE 4) W7 K9 -VROM

C81 .47µf C84 .47

K9 RPH 3H
K7 RPH 1 H
K9 +12 VA

CPU621B E58 DATA CHIP

WDAL 00 H 3 … WDAL 15 H 18
WMIB 00 L 38 … WMIB 15 L 23

CPU621B E58 CONTROL CHIP

K8 IOIRQ (I) H 3 (I3)
K8 EVIRQ (I) H 4 (I2)
K8 IPIRQ (I) H 5 (I1)
K8 RPIRQ (I) H 6 (I0)
K8 BUSY H 8
K2 MCOMP H 9
K8 RESET (I) L 10
K7 REPLY H 12
K2 WDOUT H 13
K2 WWB H 14
K2 WIAK H 15
K2 WSYNC H 16
K2 WDIN H 17

+5V
R1 2K R22 2K
K2 MSTB L 3
K2 MCCMB H 4
WMIB 15 L 7 … WMIB 21 L 18
R19 2K R18 2K
K2 MCKD L
K2 MCK L

ETS J1

WMIB 00 L 38 … WMIB 15 L 23
K9 PH2 H 24
K9 PH4 H 25
R48 2K +5V
K2 WROM DISABLE L

+5V
K9 RPH 2 H
K9 RPH 4 H

WAIT H
K9 -VCTL (SEE NOTE 4) W8 K9 -VROM
C82 .47µf
C83 .47µf
C85 .47µf K9 -VROM

CPU621B E58 CONTROL CHIP

WMIB 00 L 38 … WMIB 15 L 23

CPU621B E63 ROM CHIP 1

WMIB 13 L 7 … WMIB 21 L 18
WMIB 00 L 38 … WMIB 15 L 23
K2 MROM DISABLE L

CPU621B E70 ROM CHIP 2

WMIB 13 L 7 … WMIB 21 L 18
WMIB 00 L 38 … WMIB 15 L 23
K2 MROM DISABLE L

K9 RPH3 H
K9 RPH1 H
K9 +12VA
+5V
K9 RPH 2 H
K9 RPH 4 H

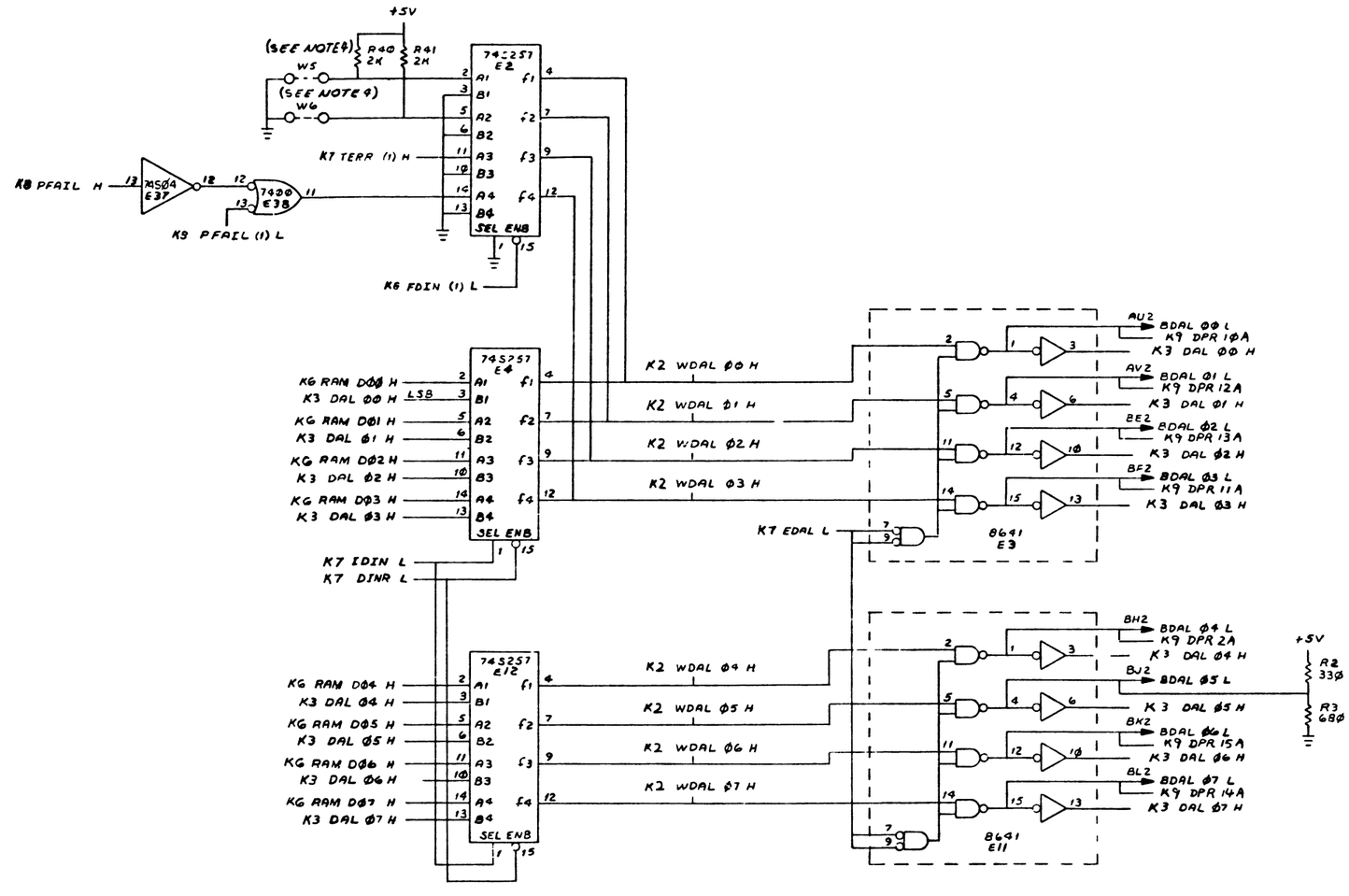
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
LSI-11 CPU MODULE (K2)	D	CS	M7264-0-1	AH
SCALE — SHEET 2 OF 9	DIST			

DEC FORM NO. 5RD 3.20

CHK FOR DCS M7264-0-1 REV A

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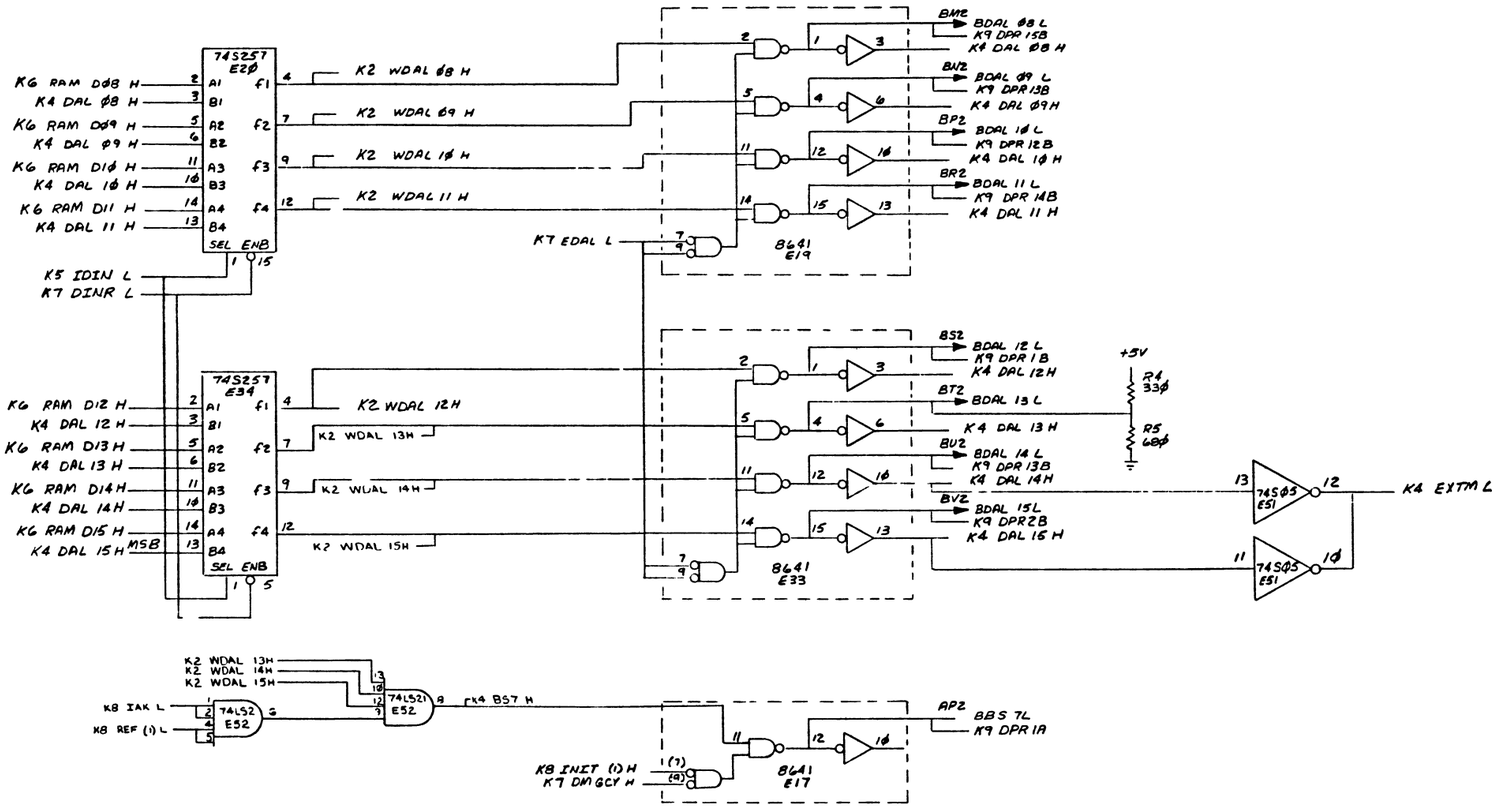


REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 CPU MODULE (K3)	D	CS	M7264-Ø-1	AH
SCALE —/— SHEET 3 OF 9 DIST				

DEC FORM NO. SMD 1.1Ø

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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 CPU MODULE (K4)	D	CS	M7264-Ø-1	AH
SCALE - SHEET 4 OF 9	DIST			

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K5 A Ø(1) L
K7 WTBTR H
K5 A Ø(Ø) L
K7 DOUTR H
K5 BYTE 1 WT L
K5 BYTE Ø WT L
K3 DAL ØØ H
K4 EXTM L
K4 DAL 13 H
K8 REFR H
K7 SYNCR L
K5 REFR (Ø) H
(SEE NOTE 4)
W1 BNK 1
W2 BNK Ø
W11 (SEE NOTE 4)
CF1
K5 SMENB L
K5 BNK OR REF H
R11 1Ø (22)
K5 RRAS L
(SEE NOTE 3)
R7 6.8K (DEL)
R47 3ØØ (243) 1%
R8 133 1%
K5 AMX H
K5 -5V
R9 38.3 1%
R1Ø 133 1%
LPSI
LPSO
CL1
CK1
C71 Ø1Uf
C1Ø3 22ØpF 1%
K5 E CAS H
K7 SYNCR H
R12 1Ø (22)
K5 RCAS L
K5 CAS L
C1Ø2 68ØPF (22ØPF) 1%
R46 5.11K (1.5K) 1%
R17 12K (DELETED)
K9 VNEG
R54 27Ø
K5 -5V
D9 1N751A 5.1V
C64 .Ø1
C99 .Ø1
K4 DAL 12 H
K3 DAL Ø6 H
K4 DAL 11 H
K3 DAL Ø5 H
K5 RAM A5 H
K5 RAM A4 H
K4 DAL 1Ø H
K3 DAL Ø4 H
K4 DAL Ø9 H
K3 DAL Ø3 H
K5 RAM A3 H
K5 RAM A2 H
K5 RAM A1 H
K5 RAM AØ H
K4 DAL Ø8 H
K3 DAL Ø2 H
K3 DAL Ø7 H
K3 DAL Ø1 H

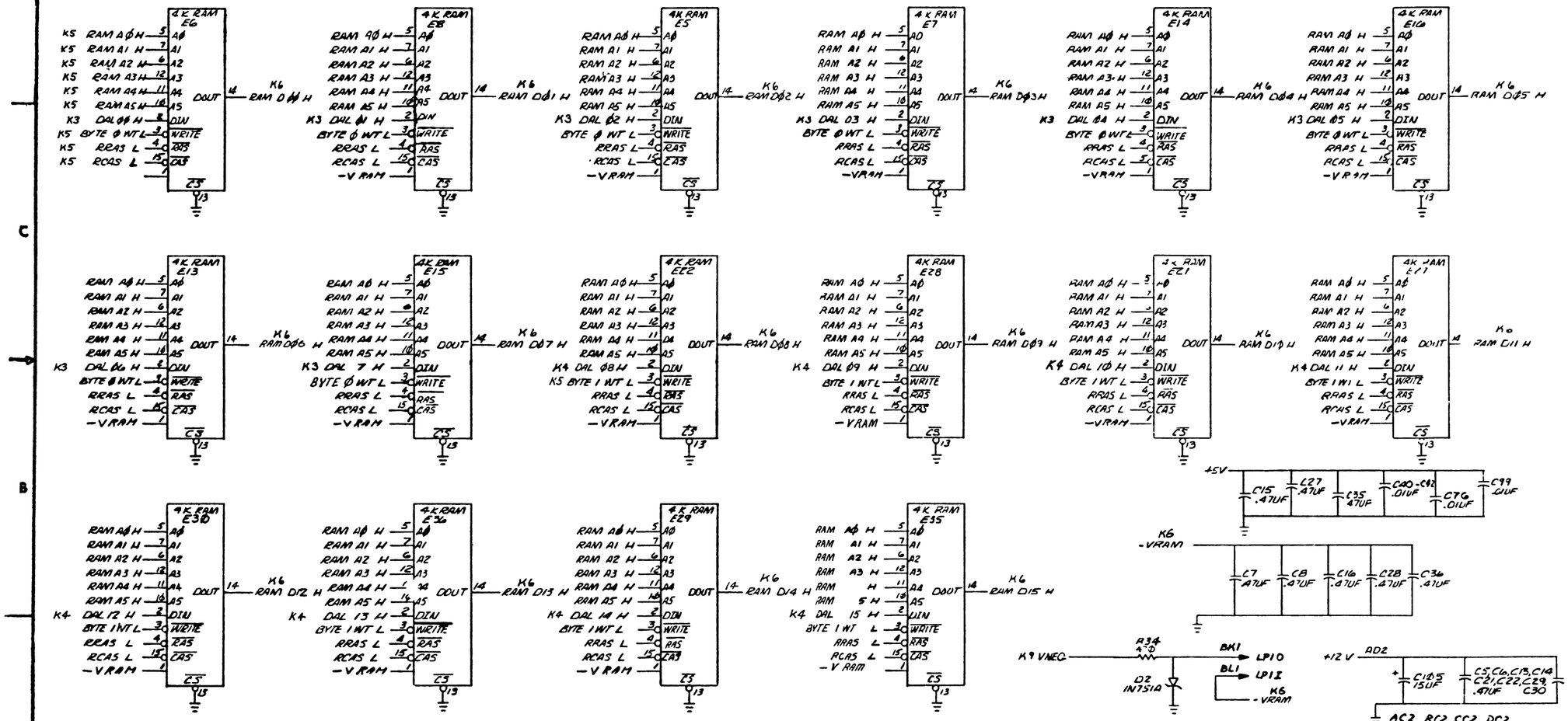
NOTE:
1 COMPONENTS ON THIS SHEET ARE DELETED FOR THE YA VAR. WITH THE EXCEPTIONS OF E45, R74 AND R75
2. NUMBERS IN BRACKETS DENOTE COMPONENT VALUES FOR M7264-EB, FB, HB AND JB VARIATIONS ; 7 PLACES. ALSO DENOTE FOR M7264-BB VARIATION AT CS OF REVISION 'AH' OR LATER

CIRCUIT SCHEMATIC ON THIS SHEET IS DELETED FOR "YA" VERSION

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	LSI-11 CPU MODULE (K5)			
SIZE	CODE	NUMBER	REV.	
D	CS	M7264-Ø-1	AH	
SCALE		SHEET 5 OF 9	DIST	

M7264-Ø-1 AH DCS



CIRCUIT SCHEMATIC ON THIS SHEET IS DELETED FOR "YB" VERSION

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 CPU MODULE (K6)	D	DCS	M7264 Ø-1	A4
SCALE	SHEET 6 OF 9	DIST		

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T497T F69
+3V
E1 E2 E4 E8 E16 E32
U/C Z Y EN/OUT
K7 TERR L
K7 TERR (I) H
K8 INIT (I) L
K7 TF CLR L
C4 STB CLR EN
K9 PH 3 H
K7 REPLY (I) H
74S10 E55

K7 DIN L
K8 DOUT D (I) L
74S00 E24
7404 E69
+5V
R52 680
74S11 E32
K7 REPLY H

K7 RPLYR H
74S74 E50
K7 REPLY (I) H
K7 REPLY (I) L
K9 PH 1 H
K8 INIT (I) L
K2 WDOUT H
K9 PH 3 H
K7 SYNC H
K7 DOUT (I) H
K7 DOUT (I) L
AE2
8DOUT L
K9 DPR 7B
K7 DOUTR H
8641 E18

AK2
BWTBT L
K9 DPR 10B
K2 WWB H
K8 INIT(I) H
K7 WTBTR H

R57 R58 R67 R66 R69 R68 RT1 RT0 RT3 RT2
680 330
BPI AC1 ADI AA1 ABI
BAD IG L
BAD IT L
+5V

+5V
R49 330
R50 680
B9ACK L
BN1
8837 E31
74S04 E37
K7 SACK R L

K7 DMGCY H
K8 DMG (I) L
74S00 E38
K7 DINR H
K5 BNK CR REF H
74S10 E55
74S11 E32
K7 EDAL L
K7 DIN L
K2 WDIN H
K7 DIN H

AH2
8DIN L
K9 DPR 4B
K8 INIT (I) H
8641 E18
K7 DINR H
FDIN (I) L
74S20 E24
K7 DINR L

K7 REPLY(I)H
74S00 E72
TP1
K7 SYNC H
K2 WSYNC H
74S04 E59
K7 SYNC L
74S74 E54
K9 PH 3 L
K8 IAK L
K7 TSYNC H
K8 INIT (I)H
8641 E18
A-2
BSYNC L
K9 DPR 6A
K7 SYNC R H
74S190 E77
K7 SYNC R L

(SEE NOTE 4)
R23 680
K5 REFR (Ø) H
W10
K7 DINR H
K5 GCAS H
74S10 E62
K7 IDIN L
74S00 E24
K7 TRPLY H
W9
K7 DOUTR H
AF2
8RPLY L
K9 DPR 11B
8641 E23
K7 RPLYR H

REVISIONS
CHK | CHANGE NO. | REV

TITLE LSI-11 CPU MODULE (K7)
SIZE D | CODE DCS | NUMBER M7264-Ø-1 | REV AH
SCALE — | SHEET 7 OF 9 | DIST

M7264-Ø-1 AH DCS

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+5V (SEE NOTE 4) R39 2K W4
+3V
7474 E71
K8 RF REQ (1) L
K9 RF OSC H
K8 RF SET L
K7 DOUT (1) L
74S174 E60
D5 R5(1) K8 DOUT D (1) L
D4 R4(1) K8 RFIRQ (1) H
D3 R3(1) K8 IDIRQ (1) H
D2 R2(1) K8 EVIRQ (1) H
D1 R1(1) K8 IPIRQ (1) H
K7 TERR L
D0 R0(1) K8 RESET (1) L
CLR CLK
K9 PH 2H

AL2 BIRQ L K9 DPR 5A
8837 E31

+5V (SEE NOTE 4) R38 2K W3
+3V
7474 E71
K8 EF CLR L

* C108 .01μF
BR1 BEVNT L K9 DPR 6B
8837 E31

R32 330Ø +5V
R33 680Ø
API B HALT L

+5V P20Ø 680Ø
K8 INIT (1) H
K7 DMG CY H
8641 E17
K8 PFAIL H
74S05 E51
7400 E72
K8 PFAIL (1) L

BA1 BDC OK H K9 DPR 9A
8837 E31
74S04 E59
K8 DC LO L

BB1 BPWR OK H K9 DPR 7A
8837 E31
74S11 E32
R77 330Ø
C107 1200pF

+3V
7474 E43

R30 330Ø +5V
931 680Ø
ANI BDMRL
8837 E31

K8 DCLD L
K8 PFCLR
7400 E38
74S04 E37

K7 SACKR L
74S74 E54
K9 PH 1 H
K8 INIT (1) L
K9 PH 4 H
7474 E49
7400 E72
K8 BUSY H
951 680Ø +5V

+3V
K8 DMG (1) H
7474 E49
K9 PH 4 H
K7 SYNC L
K8 DMG (1) L
AS2 B DMGO L K9 DPR 9B
8641 E23

K9 PH 3 L
7404 E69
DC1 K8 SPH 3 H

K2 WMIB 21 L
7404 E69
DH1 K8 SROM 3H
K9 PH 3 H
7400 E45

K2 WMIB 20 L
7404 E69
DF1 K8 SROM 2H

K2 WMIB 19 L
7404 E69
DE1 K8 SROM 1H

K2 WMIB 18 L
7404 E69
DD1 K8 SROM ØH

7442 E68
K8 EF CLRL
K8 PF CLRL
K8 TF CLRL

K8 DC LO L
7474 E64
K8 INIT (1) H
K8 INIT (1) L
AT2 BINIT L K9 DPR 3B
8641 E23

CR2 LP2O
CS2 LP2I
CM2 LP3O
CN2 LP3I

+5V R76 680Ø
K8 IF CLR L
RF SET L
7474 E64
K8 REF (1) L
TP2 K8 T REF (1) H
K8 INIT (1) H
K7 DMG CY H
8641 E17
AR1 B REF L K9 DPR 4A
K8 REF R H
8641 E23
AF1 K8 SRUN L
CH1 K8 SRUN L

K8 IAK L
K2 WIAK H
74S04 E59
+3V
74S04 E53
K8 TIAK (1) H
K8 IAK (1) L
K9PH 1 L
7474 E43
K7 DIN H
K8 INIT (1) H
K7 DMG CY H
8641 E17
AN2 BIAKO L K9DPR 3A

K8 FDIN (1) H
K8 FDIN (1) H
7474 E44
K7 SYNC H

* C108 IS AN OPTIONAL CAP. AND IS NOT INSTALLED BY MODULE BUILD AREAS. THE CAP MAYBE INSTALLED IN M7264'S USED IN LARGE SYSTEMS AT FIELD SERVICE'S DISCRETION REFER TO ECO* M7264-ML022.

REVISIONS		
CHK	CHANGE NO	REV

TITL.	SIZE	CODE	NUMBER	REV.
LSI-11 CPU MODULE (K8)	D	CS	M7264-Ø-1	A H
SCALE — SHEET 8 OF 9	DIST.			

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CLK. GEN

REF GEN

K9 +12VA
R1G 5G 1/2W
R13 5G 1/2 W
C9Ø .47UF
DG IN751A 5.1V
CØØ .01UF
C1ØØ 12PF
MC 4024 E7B
(SEE NOTE 1)
R14 5K
C1Ø1 .33UF
MC 4024A E7B
K9 RF OSC H
RG3
R15 2K (SEE NOTE 2)
R55
K2 MCKD L
T4ØØ E7Z
74S14Ø E77
K2 MCK L

T74S139 E5G
K9 DIVA(Ø) H
K9 DIVB(Ø) H
K2 MSTB L
C1Ø4 68 PF
R21 150
D7 DGG4
K9 PH 1 L
K9 PH 3 L
74SØ4 EG1
K9 PH 1 H
K9 PH 2 H
K9 PH 3 H
K9 PH 4 H

K9 +12VA
RG5 33
R35 33
CG7 .47
K9 DIVB (Ø) H
R36 120
MHØØ2G EG6
C93 .47UF
D4 DGG4
D3 DGG4
C92 .47UF
D1 DGG4
K9 VNEG
R37 330
R59 *
R53 *
K9 -VROM
K9 -VCT L
K9 -VDATA
D5 IN748A 3.9V
D22 *
D8 *
CG8 .47UF
C9G .Ø1UF
C97 .Ø1 UF
D2G DGG4
DK1 LP4I
DL1 LP4O

K9 +12VA
RG4 33
RG2 33
CT5 .47
K9 DIVA (Ø) H
RG1 100Ω
MHØØ2G ET3
C95 .47
D1 DG.4
K9 VDVR
D16 D23 DGG4 D25 DGG4 D24 DGG4
+12 VA
D18 DGG4 D19 DGG4
C94 .47 UF
74S04 EG1
MHØØ2G ET3
RGØ 5G 1/2W
CT4 .47 UF

K9 +12VA BD2
CG9 15UF
C8Ø .47UF
C53 .47UF
C58 .47UF
CG3 .47UF
CT3 .47UF
C79 .47UF
AC2,BC2,CC2,DC2
AT1,BT1,CT1,DT1

+12V AD2
CG7 15UF

+5V
R28 330
R29 680

+5V AA2,BA2
CBG 15UF
CB8 15UF
C1-C4 .Ø1
C9-C12 .Ø1
C17-C2Ø .Ø1
C23-C26 .Ø1
C31-C34 .Ø1
C37-C52 .Ø1
C54-C57 .Ø1
C59-CGE .Ø1
AC2,BC2,CC2,DC2
AT1,BT1,CT1,BT1

C7Ø .47UF
+5V
R5G 2K
K9 VDVR
R42 22Ω
R43 22Ω
R45* 22Ω
R44 27Ω
K9 +12VA
K9 RPH 1 H
K9 RPH 2 H
K9 RPH 4 H
K9 RPH 3 H
Q1
Q2
Q3
Q4
75322 EG7
T5322 E74
K9 PH 1 H
K9 PH 2 H
K9 PH 4 H
K9 PH 3 H
C78 .47UF
D2Ø DGG4
D21 DGG4
DKØ DGG4
D11 DGG4
D14 DGG4
D15 DGG4
D12 DGG4
D13 DGG4

+5V AA2,BA2
C1ØG .Ø1
C7F .Ø1
C7G .Ø1
C72 .Ø1
C71 .Ø1
C69 .Ø1
CG8 .Ø1
CG5 .Ø1

* FOR VARIATIONS -YB AND -3B ONLY, R45 IS 15Ω.

E9

K9 DPR 15A	15	330 680
K9 DPR 14A	14	330 680
K9 DPR 13A	13	330 680
K9 DPR 12A	12	330 680
K9 DPR 11A	11	330 680
K9 DPR ØA	10	330 680
K9 DPR 9A	9	330 680
K9 DPR 8A	7	330 680
K9 DPR 7A	6	330 680
K9 DPR 6A	5	330 680
K9 DPR 5A	4	330 680
K9 DPR 4A	3	330 680
K9 DPR 3A	2	330 680
K9 DPR 2A	1	330 680
K9 DPR 1A	+5V 16	330 680

E25

K9 DPR 15B	15	330 680
K9 DPR 14B	14	330 680
K9 DPR 13B	13	330 680
K9 DPR 12B	12	330 680
K9 DPR 11B	11	330 680
K9 DPR 1ØB	10	330 680
K9 DPR 9B	9	330 680
K9 DPR 7B	7	330 680
K9 DPR 6B	6	330 680
K9 DPR 5B	5	330 680
K9 DPR 4B	4	330 680
K9 DPR 3B	3	330 680
K9 DPR 2B	2	330 680
K9 DPR 1B	1	330 680
+5V	16	330 680

* SEE NOTE *5 ON SHEET 1

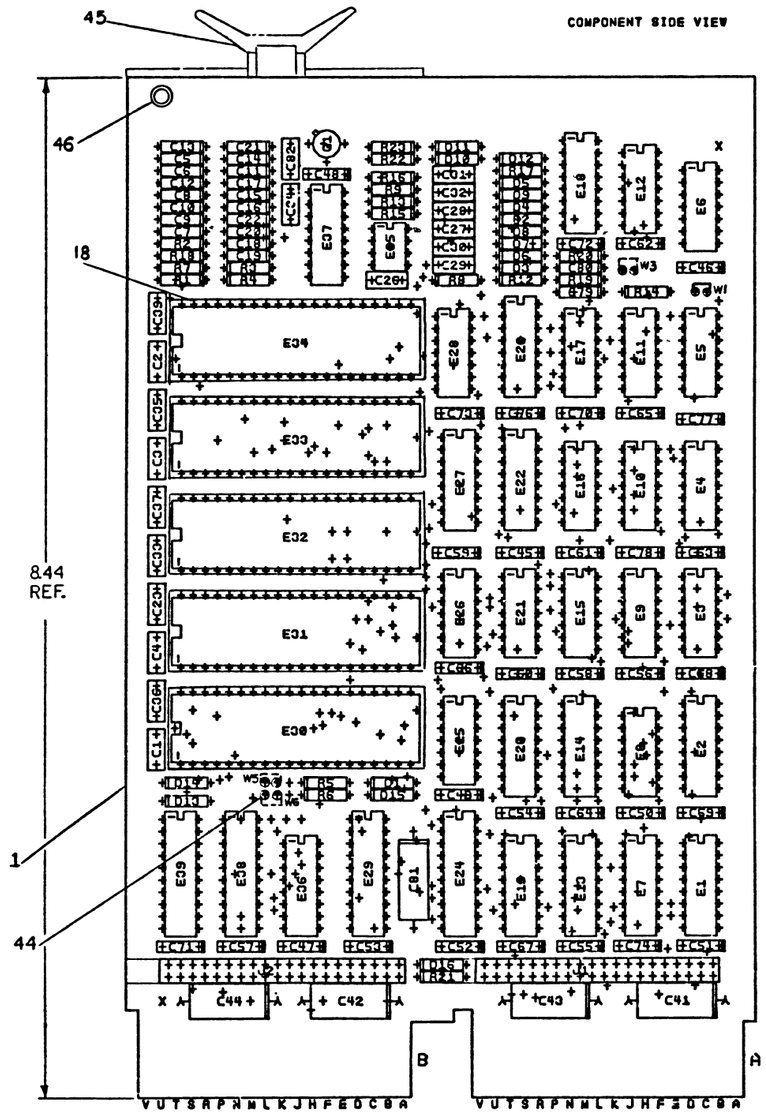
REVISIONS

CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 CPU MODULE (K9)	D	CS	M7264-Ø-1	AH
SCALE —	SHEET 9 OF 9	DIST		1

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COMPONENT SIDE VIEW



NOTES:
1. W1 INSTALLED. W3, W5, AND W6, NOT INSTALLED.
2. C81 MAY BE REMOVED AS A CUSTOMER OPTION.

CH	CHANGE NO	REV
5411	M7270-H0008	F
	M7270-H0009	G
	M7270-H0010	H
	M7270-H0008	J
	M7270-H0009	K
	M7270-H0008	L

ETCH REV. F-P1
P.C. DESIGN DATA BASE REV. F

SIGNATURES	DATE
DRN: J. Vasquez	10 NOV 87
CHK'D. M. Tarsala	11 NOV 87
ENG. M. Tarsala	23 NOV 87
PROJ. ENG. M. Tarsala	23 NOV 87
PROD. K. MERCADO	24 NOV 87

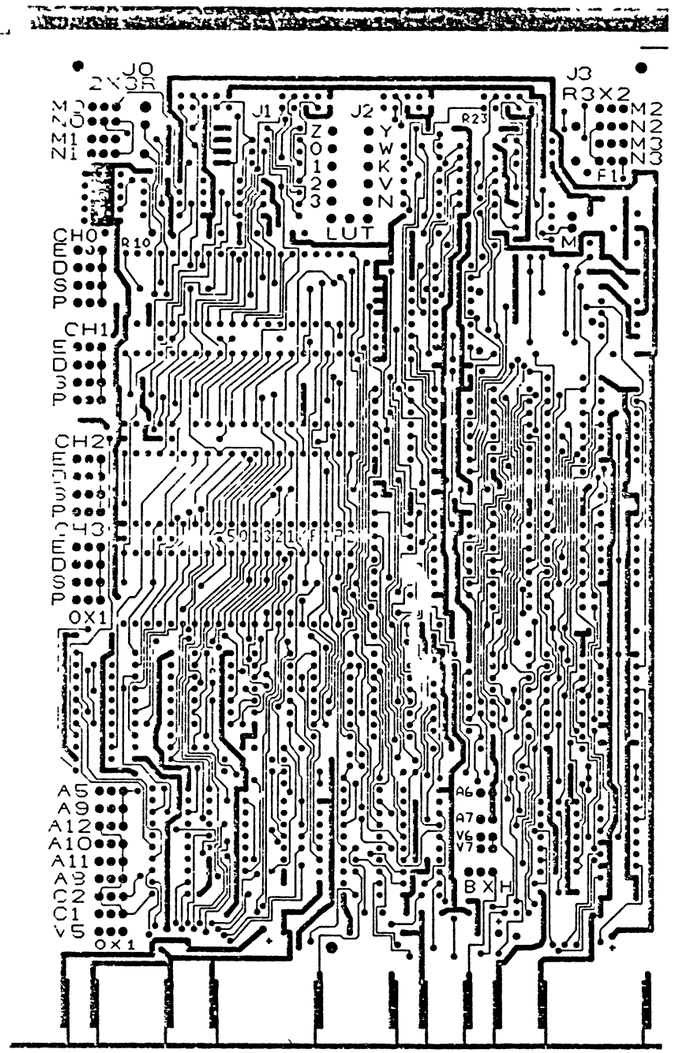
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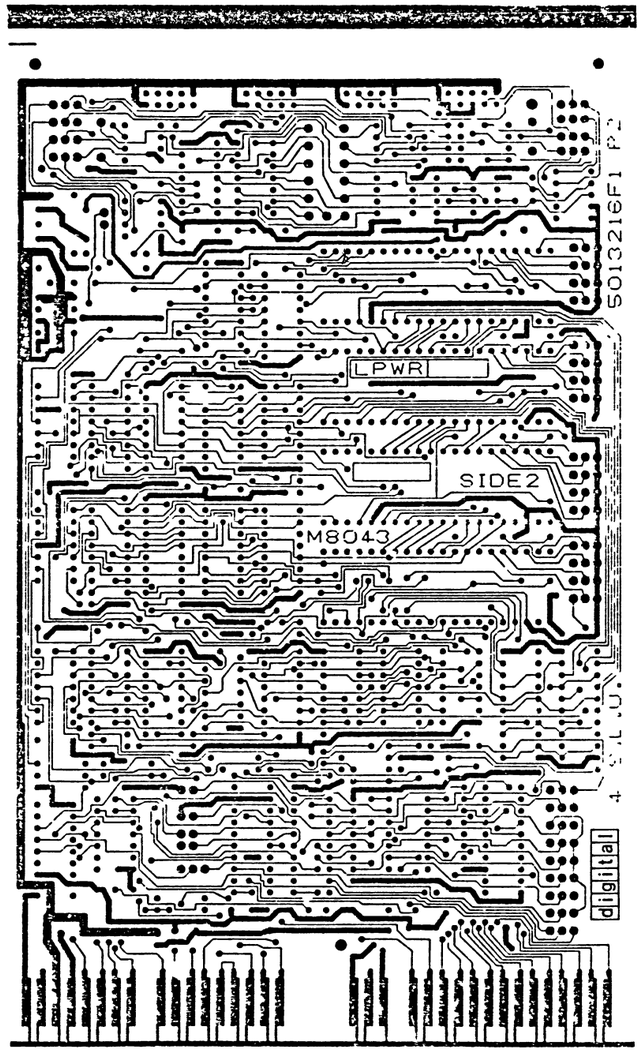
digital

TITLE LSI-11 CPU

SIZE	CODE	NUMBER	REV
D	UA	M7270-00	L

D UA M7270-00 L





ETCH ART DRAWING

D-UA-M8043-0-0

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+12V

D13 DG64 D14 DG64

C23 .47μF C39 .47μF

K5 -VBB
K5 RPH 3 H
K5 RPH 1 H
+12 V

C1 .47 μF

+5V

C2 .47 μF

R1 2K

K1 MSTB L
K1 MCOMP H

1611 DATA CHIP 2111549-01 OR 2115579-00 E38

1631-15 (3015) E18/F18 E34 2300385 OPTIONAL

K1 WDAL 00 H
K1 WDAL 01 H
K1 WDAL 02 H
K1 WDAL 03 H
K1 WDAL 04 H
K1 WDAL 05 H
K1 WDAL 06 H
K1 WDAL 07 H
K1 WDAL 08 H
K1 WDAL 09 H
K1 WDAL 10 H
K1 WDAL 11 H
K1 WDAL 12 H
K1 WDAL 13 H
K1 WDAL 14 H
K1 WDAL 15 H

K1 WMIB 00 L
K1 WMIB 01 L
K1 WMIB 02 L
K1 WMIB 03 L
K1 WMIB 04 L
K1 WMIB 05 L
K1 WMIB 06 L
K1 WMIB 07 L
K1 WMIB 08 L
K1 WMIB 09 L
K1 WMIB 10 L
K1 WMIB 11 L
K1 WMIB 12 L
K1 WMIB 13 L
K1 WMIB 14 L
K1 WMIB 15 L

K1 WMIB 15 L
K1 WMIB 14 L
K1 WMIB 13 L
K1 WMIB 12 L
K1 WMIB 16 L
K1 WMIB 17 L
K1 WMIB 18 L
K1 WMIB 19 L
K1 WMIB 20 L
K1 WMIB 21 L

K1 WMIB 00 L
K1 WMIB 01 L
K1 WMIB 02 L
K1 WMIB 03 L
K1 WMIB 04 L
K1 WMIB 05 L
K1 WMIB 06 L
K1 WMIB 07 L
K1 WMIB 08 L
K1 WMIB 09 L
K1 WMIB 10 L
K1 WMIB 11 L
K5 PH 2 H
K5 PH 4 H
+5V
RB 2K
K1 MROM DISABLE L

+5V
K5 RPH 2 H
K5 RPH 4 H

C5 33 PF K1 WMIB 00 L
C6 33 PF K1 WMIB 01 L
C9 33 PF K1 WMIB 02 L
C7 33 PF K1 WMIB 03 L
C8 33 PF K1 WMIB 04 L
C12 33 PF K1 WMIB 05 L
C21 33 PF K1 WMIB 06 L
C14 33 PF K1 WMIB 07 L
C16 33 PF K1 WMIB 08 L

C18 33 PF K1 WMIB 09 L
C20 33 PF K1 WMIB 10 L
C22 33 PF K1 WMIB 11 L
C17 33 PF K1 WMIB 12 L
C11 33 PF K1 WMIB 13 L
C13 33 PF K1 WMIB 14 L
C10 33 PF K1 WMIB 15 L
C15 33 PF K1 WMIB 16 L
C19 33 PF K1 WMIB 17 L

K1 WAIT H

+12V

D1 DG64 D15 DG64

C35 .47μF C36 .47μF C37 .47μF

K5 -VBB
K5 RPH 3 H
K5 RPH 1 H
+12V

C3 .47μF

1621-7 (2007) CONTROL CHIP 23-00204 E33

K3 WIOI RQ (1) H
K3 WEVI RQ (1) H
K3 WIPI RQ (1) H
K1 WMIB 17 L
K2 WBUSY H
K1 MCOMP H
K3 WRESET (1) L
K1 WMIB 16 L
K2 WREPLY H
K1 WDOUT H
K1 WWB H
K1 WIAK H
K1 WSYNC H
K1 WDIN H

I3
I2
I1
I0

K1 WMIB 00 L
K1 WMIB 01 L
K1 WMIB 02 L
K1 WMIB 03 L
K1 WMIB 04 L
K1 WMIB 05 L
K1 WMIB 06 L
K1 WMIB 07 L
K1 WMIB 08 L
K1 WMIB 09 L
K1 WMIB 10 L
K1 WMIB 11 L
K1 WMIB 12 L
K1 WMIB 13 L
K1 WMIB 14 L
K1 WMIB 15 L

C4 .47 μF

1631-7 (3007) MICROM 0 E31 2300285

K1 WMIB 15 L
K1 WMIB 14 L
K1 WMIB 13 L
K1 WMIB 12 L
K1 WMIB 16 L
K1 WMIB 17 L
K1 WMIB 18 L
K1 WMIB 19 L
K1 WMIB 20 L
K1 WMIB 21 L

K1 WMIB 00 L
K1 WMIB 01 L
K1 WMIB 02 L
K1 WMIB 03 L
K1 WMIB 04 L
K1 WMIB 05 L
K1 WMIB 06 L
K1 WMIB 07 L
K1 WMIB 08 L
K1 WMIB 09 L
K1 WMIB 10 L
K1 WMIB 11 L
K1 MROM DISABLE L

C33 .47 μF

1631-10 (3010) MICROM 1 E32 2300185

K1 WMIB 15 L
K1 WMIB 14 L
K1 WMIB 13 L
K1 WMIB 12 L
K1 WMIB 16 L
K1 WMIB 17 L
K1 WMIB 18 L
K1 WMIB 19 L
K1 WMIB 20 L
K1 WMIB 21 L

K1 WMIB 00 L
K1 WMIB 01 L
K1 WMIB 02 L
K1 WMIB 03 L
K1 WMIB 04 L
K1 WMIB 05 L
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K1 WMIB 11 L
K1 MROM DISABLE L

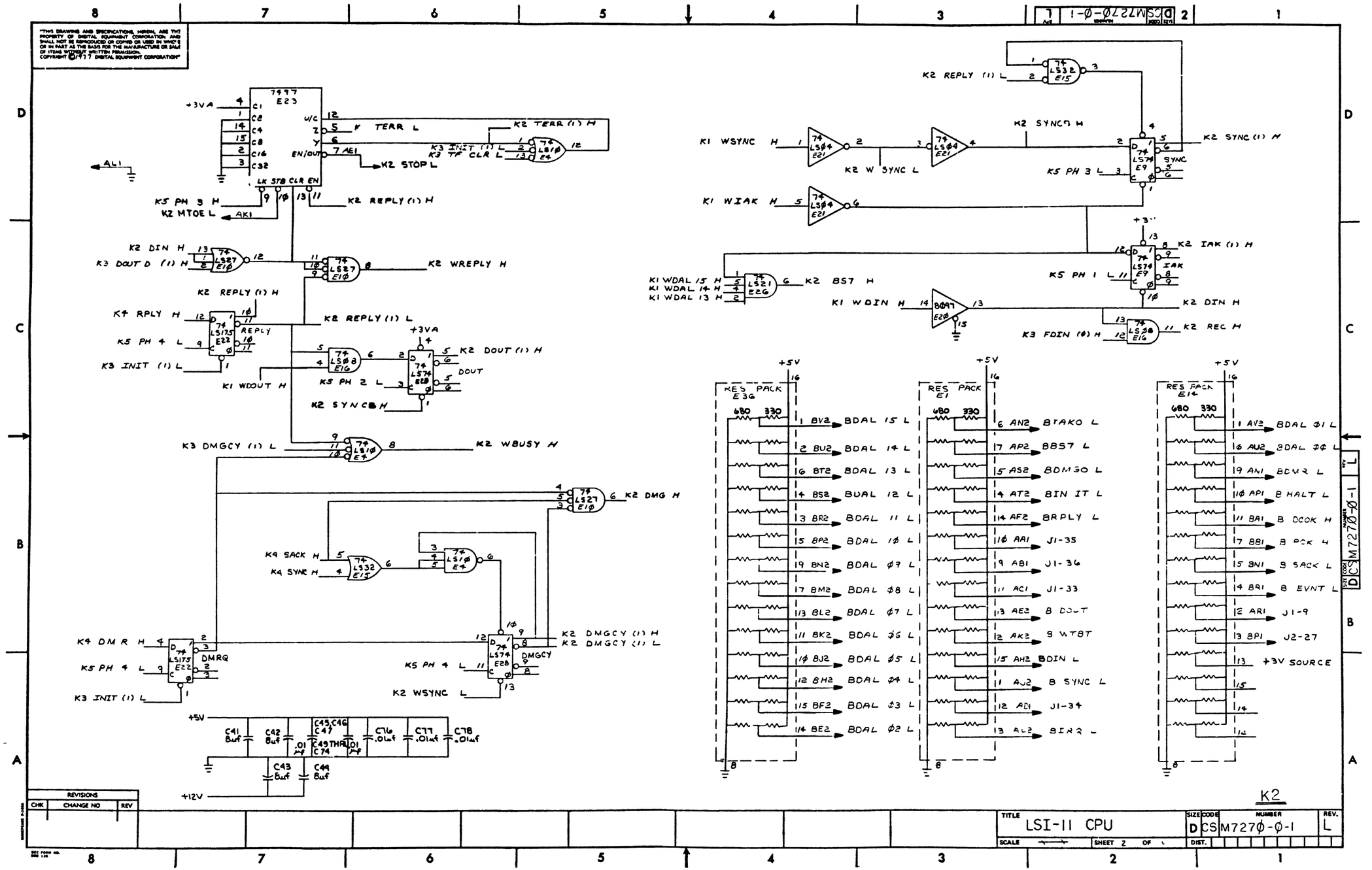
+5V
K5 RPH 2 H
K5 RPH 4 H

REVISIONS			
CHK	CHANGE NO.	REV.	
[illegible]	M7270-00001	D	
H. Bonanno 11/30/77			
R. FITCH	M7270-MR002	E	
Robert Fitch 1 Dec 77			
R. FITCH	M7270-MR003	F	
Robert Fitch 21 MAR 78			
R. FITCH	M7270-MR004	H	
Robert M. Fitch 15 MAY 78			
R. FITCH	M7270-MR005	J	
Robert Fitch 27 Sept 78			
R. SALETT	M7270-MR006	J	
Gerald M. Salett 11/6/79			
R. SALETT	M7270-MR007	L	
Gerald M. Salett 11/9/79			
G. KUSHNER			

DRN. E. Wilson	4/14/77	FIRST USED ON: LSI-11
CHK'D R.J. Conti	19 Sept 77	digital
ENG. Robert Fitch	20 SEP 77	TITLE: LSI-11 CPU
PROJ. ENG. Robert Fitch	20 SEP 77	
PROD. [illegible]	20 SEP 77	
NEXT HIGHER ASSY. B-DD-M7270-0		SIZE D CODE CS NUMBER M7270-0-1 REV. L
SCALE NONE		
SHEET 1 OF 0		DIST

K1

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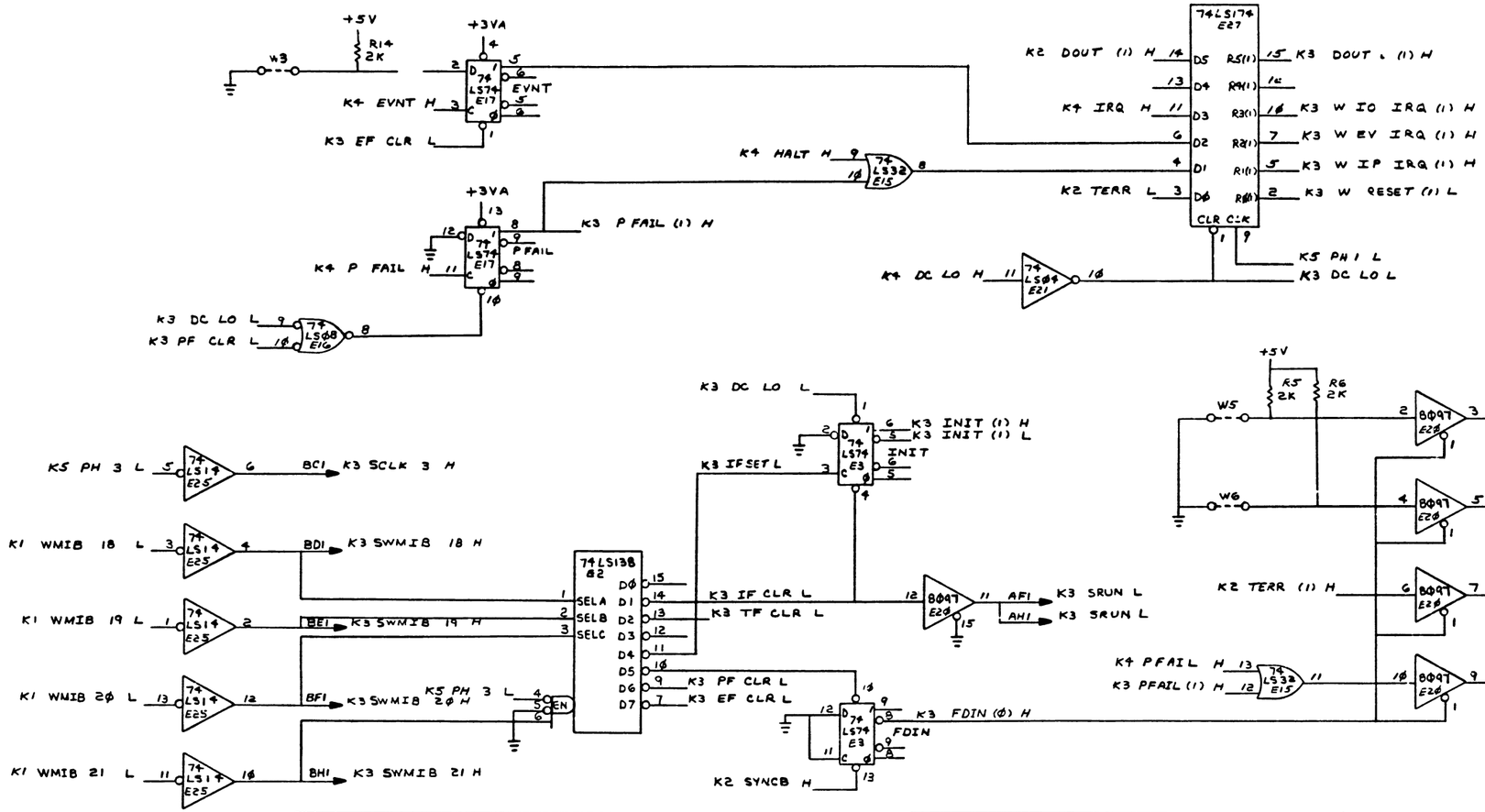


REVISIONS		
CHK	CHANGE NO	REV

K2

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LSI-11 CPU	D	CS	M7270-0-1	L
SCALE	SHEET 2 OF 4	DIST.		

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JUMPER TABLE

JUMPER	FUNCTION WHEN INSTALLED	FACTORY CONFIGURATION
W1	CRYSTAL CLOCK	I
W3	DISABLE EVENT LINE INTERRUPT	R
W5	POWER UP SELECT	P
W6	POWER UP SELECT	R

POWER-UP MODES

MODE	JUMPERS W6	JUMPERS W5	MODE SELECT
0	R	R	PC AT 24 AND PS AT 26, OR HALT MODE
1	R	I	ODT MICROCODE
2	I	R	PC AT 173000 FOR USER BOOTSTRAP
3	I	I	SPECIAL PROCESSOR MICROCODE (NOT IMPLEMENTED)

NOTE: R = JUMPER REMOVED, I = JUMPER INSTALLED

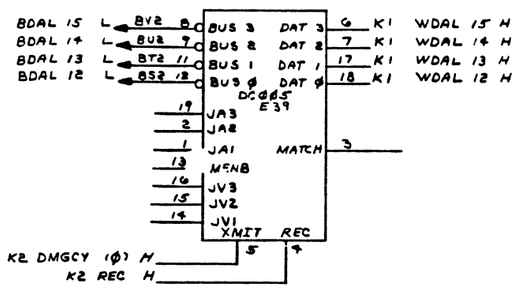
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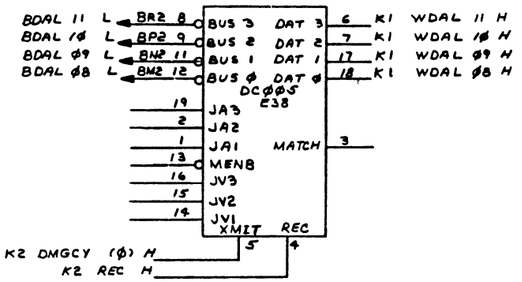
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CHK	CHANGE NO	REV

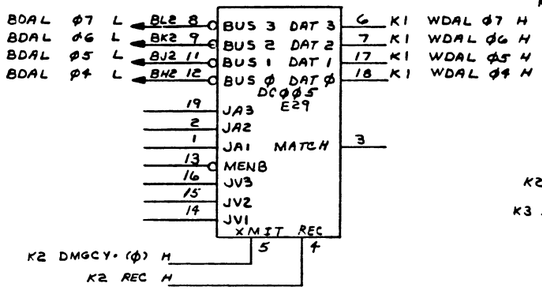
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SIZE D CODE CS NUMBER M7270-0-1 REV L
SCALE — SHEET 3 OF 3 DIST.

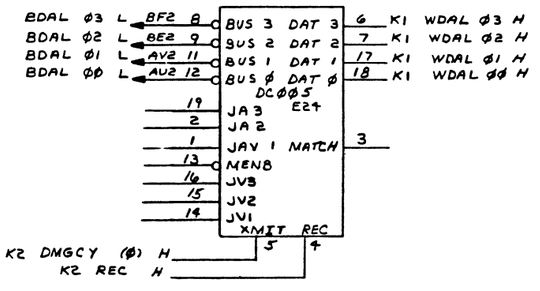
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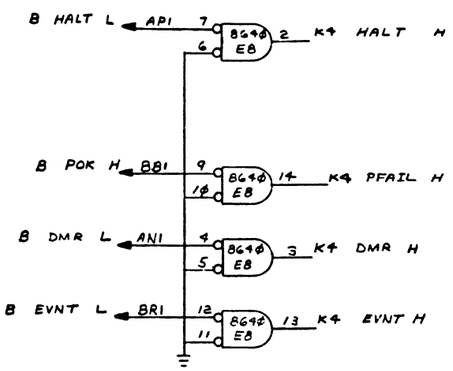
NOTES:
1. THE WAKE UP CIRCUIT MAY BE DISABLED BY REMOVING C81

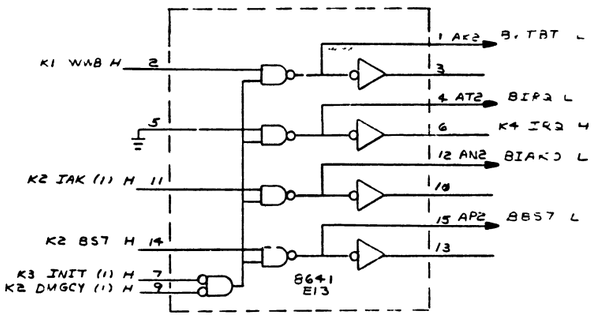


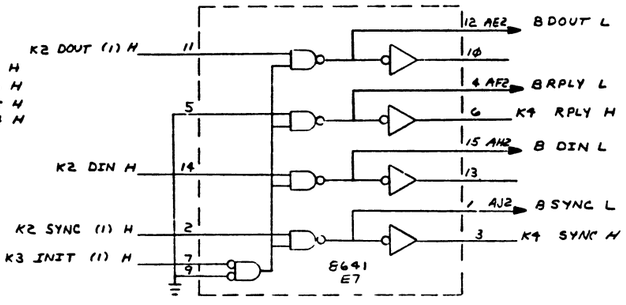


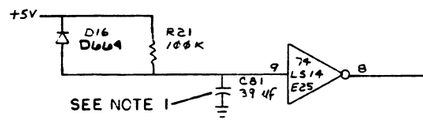


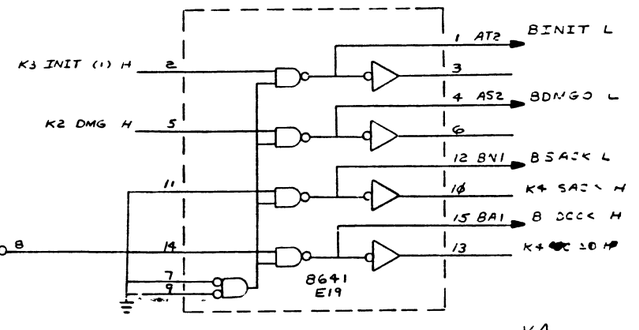










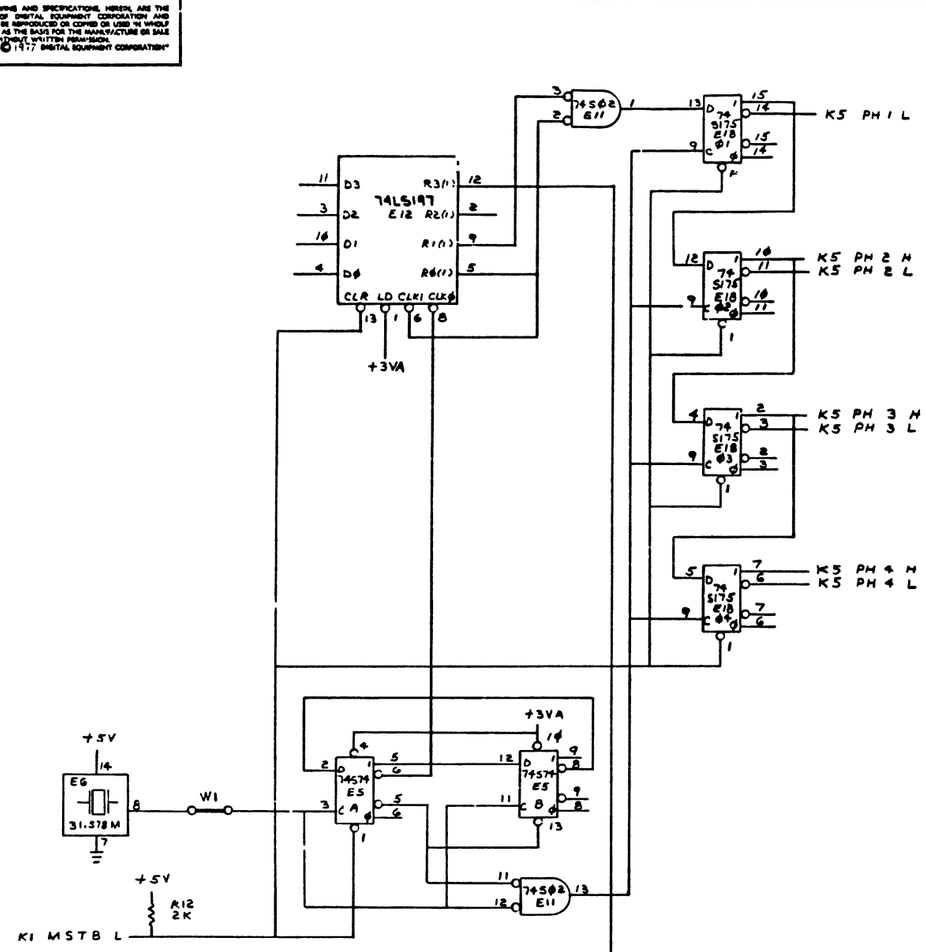


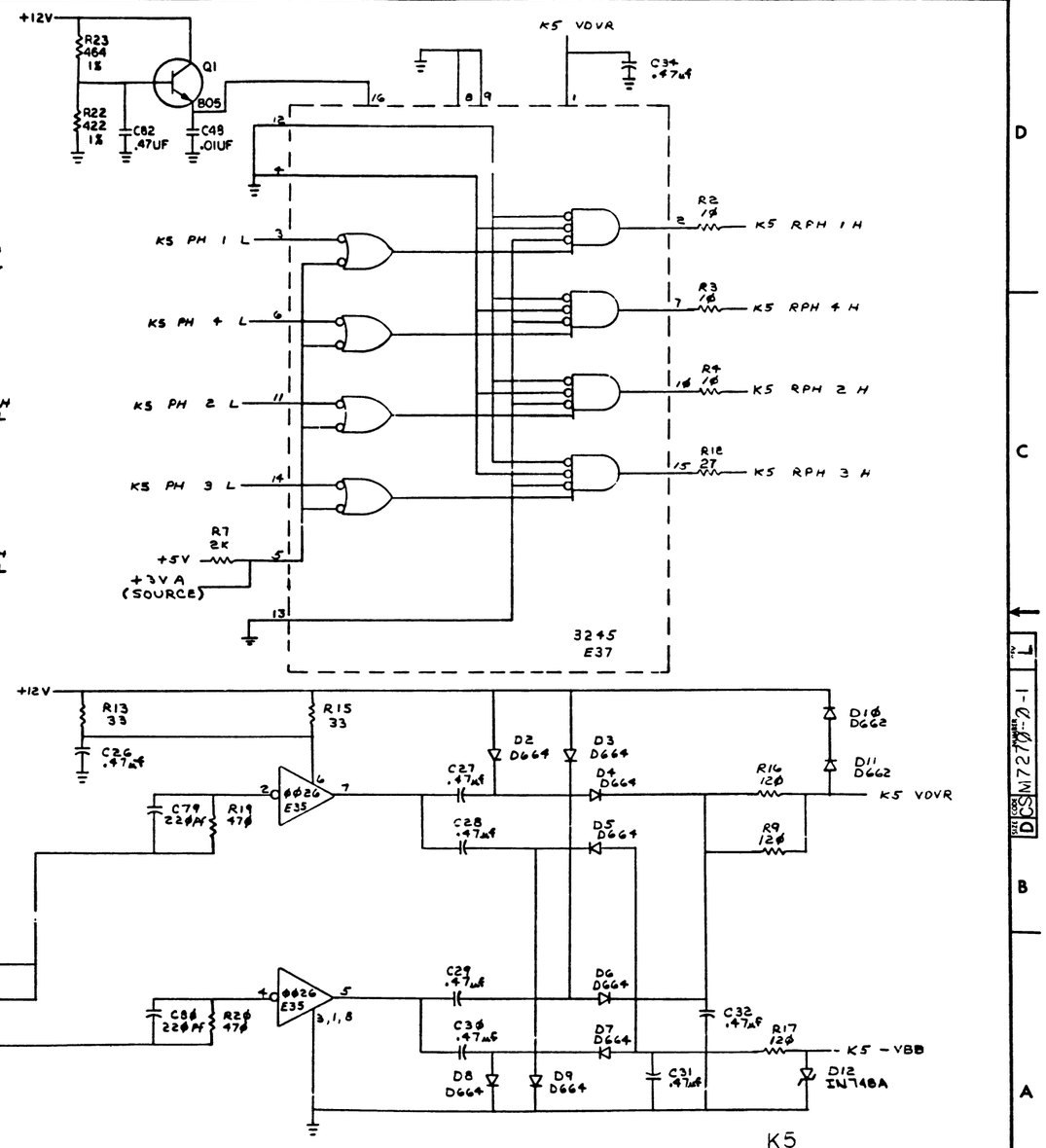
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CHK	CHANGE NO.	REV

K4

TITLE	SIZE	CODE	NUMBER	REV.
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SCALE — SHEET 4 OF 6	DIST.			

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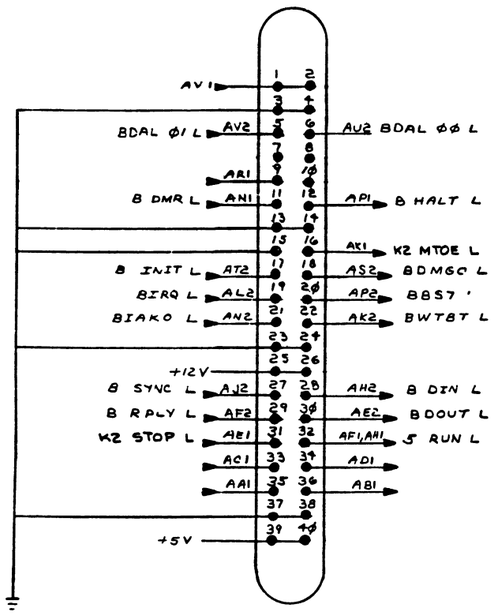
K5

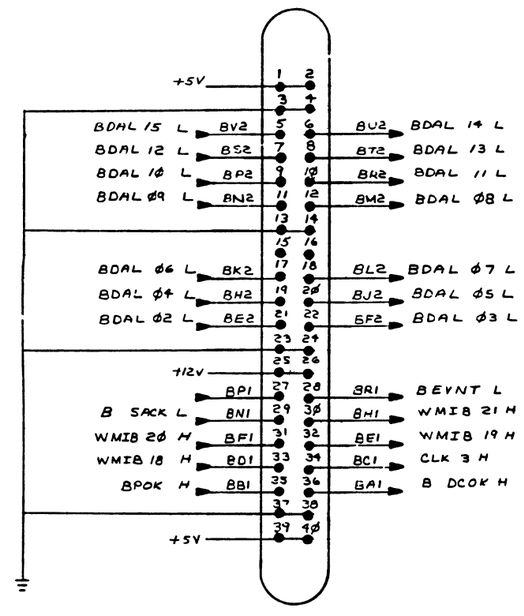
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LSI-11 CPU	D	CS	M727Ø-Ø-1	L
SCALE —	SHEET 5 OF 6	DIST.		

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J2





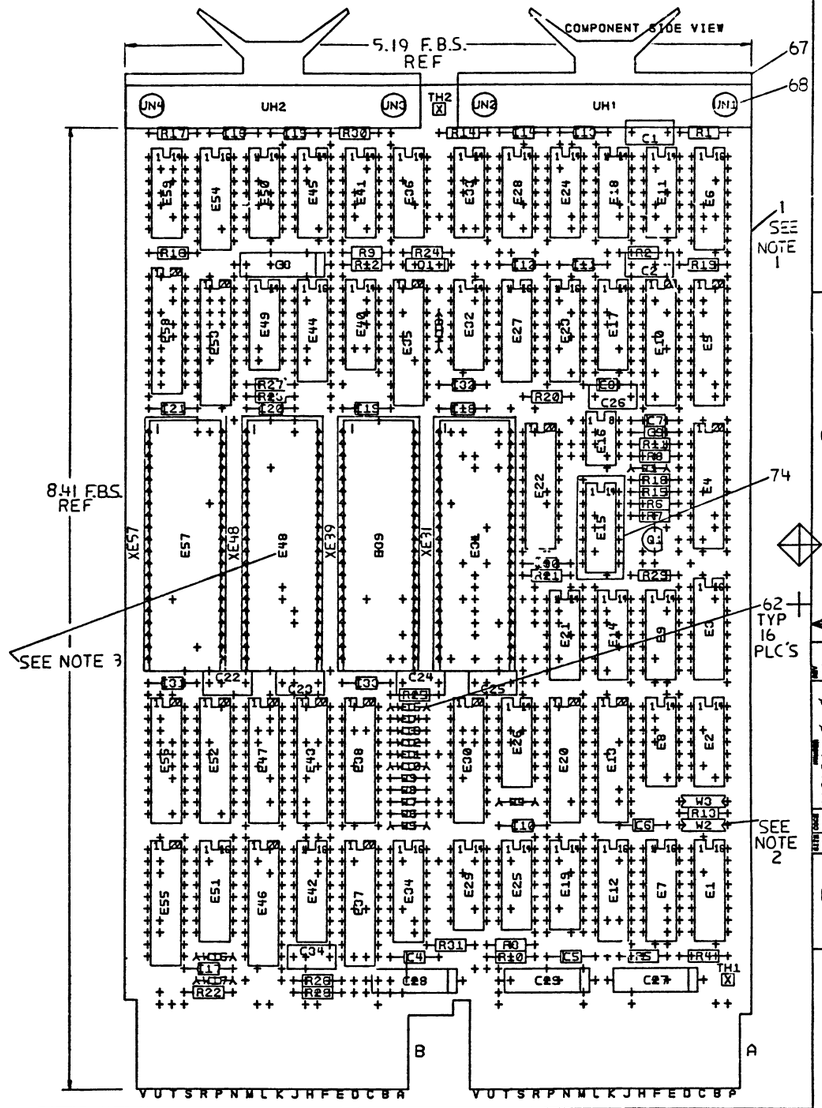
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI-11 CPU	D	CS	M7270-0-1	L
SCALE 2/1 SHEET 6 OF 6	DIST.			

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JUMPER CONFIGURATIONS

JUMPER	NAME	FUNCTIONALITY	SHIPPING STATUS
W1	MASTER CLOCK	IN=ENABLED	IN
W2	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE	OUT
W3	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE	IN
W4	EVENT LINE ENABLE	OUT=ENABLED	IN
W5,W6	POWER UP MODE	MODE 0: NAME PC@24, PS@26; W5 OUT; W6 OUT MODE 1: NAME CONSOLE ODT; W5 IN; W6 OUT MODE 2: NAME BOOTSTRAP; W5 OUT; W6 IN MODE 3: NAME EXTENDED MICROCODE; W5 IN; W6 IN	W5-IN W6-OUT
W7	HALT/TRAP OPTION	IN=TRAP TO 10_8 ON HALT OUT=ENTER CONSOLE ODT ON HALT	OUT
W8	BOOTSTRAP ADDRESS	IN=POWER UP TO 173000_8 OUT=POWER UP TO ADDRESS SPECIFIED BY W9-W15	IN
W9-W15	USER SELECTABLE BOOTSTRAP ADDRESS	W9-W15 CORRESPOND TO ADDRESS BITS 9 THRU 15 RESPECTIVELY IN=LOGIC 1, OUT=LOGIC 0	IN
W16,W17	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE	IN
W18	WAKE-UP CIRCUIT	OUT=ENABLED	IN



NOTES: 1. REFER TO PARTS LIST FOR ALL NUMBERED ITEMS.
2. W2 IS A SPARE JUMPER.
3. E29, E48 & E57 ARE SPARE IC'S.

STEP ↕	↑ Y AXIS ___ STEP ___ TIMES
REPEAT	→ X AXIS ___ STEP ___ TIMES

CHK	CHANGE NO	REV
	REDRAWN M8186-ML01Ø	H

ETCH REV. D-P4

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH. ENG.	
PROJ. ENG.	
PROD.	
SCALE 2:1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M8186-Ø	

digital

TITLE: KDF11-A CPU

SIZE D | CODE UA | NUMBER M8186-Ø-Ø | REV H

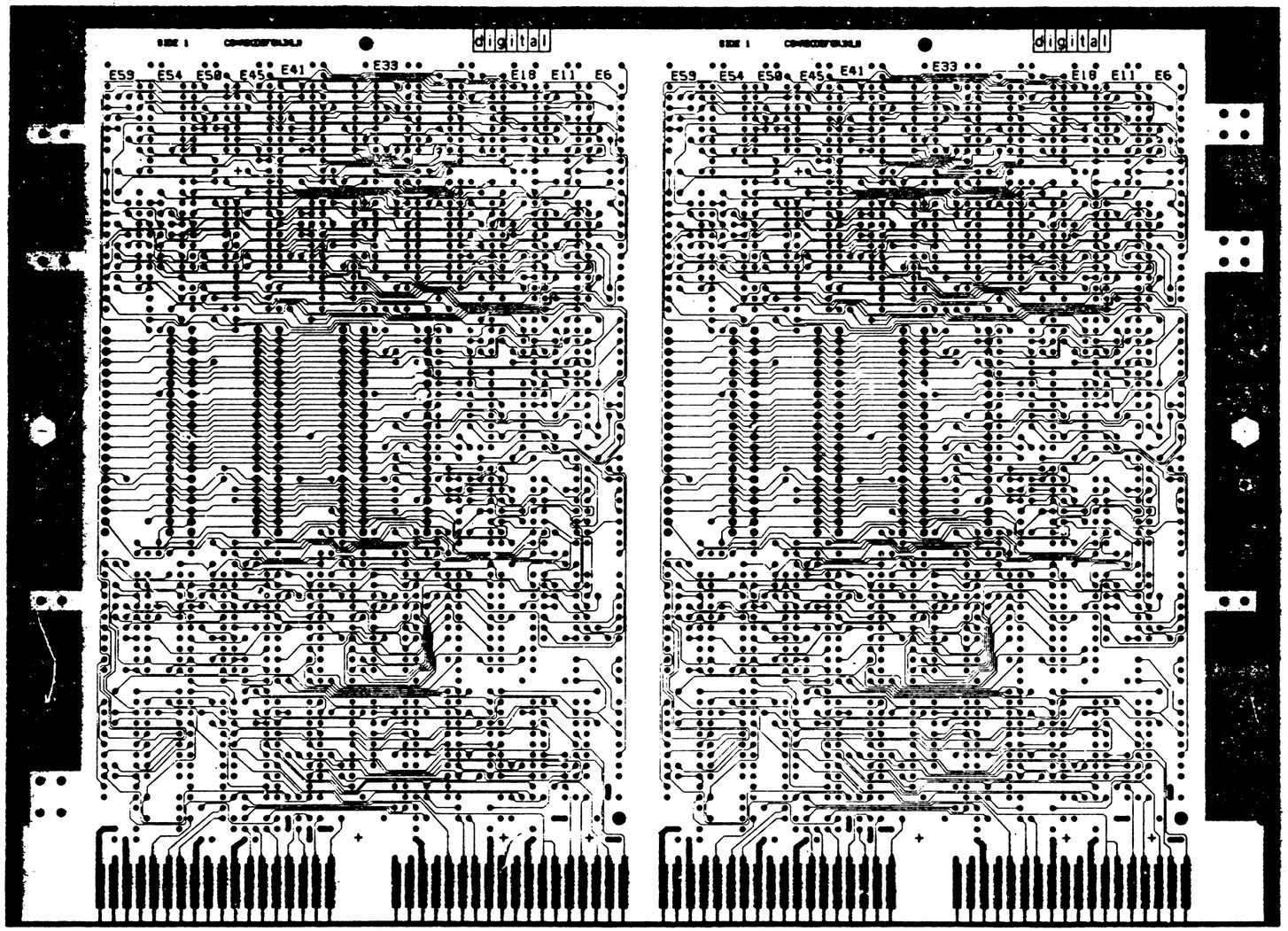
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LAYER 1

8/8 5013326 D-P4 M8186

8/8 5013326 D-P4 M8186



NOTES:

REV	CHANGE NO	CHK
H	MAGFLØW ORIGINATED	

SIGNATURES	DATE
DRN. L. Delaware	1/23/81
CHK'D. D. Bowman	14 MAY 81
ENG. Tony Ng	21 MAY 81
PROJ. ENG. Tony Ng	21 MAY 81
PROD. Tony Ng	21 MAY 81
SCALE 2:1	
SHT. 1 OF 2	
ETCH REV D-P4	FIRST USED ON: M8186

digital

TITLE: ETCH CUT DRAWING

SIZE	CODE	NUMBER	REV
D	EC	5013326-0-0	H

D EC 5013326-0-0 H

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L4

LAYER H

L4

KDF11 CPU SIDE2

5013326 D-P4

MB186

KDF11 CPU SIDE2

5013326 D-P4

MB186

REVISIONS			
CHK	CHANGE NO		

TITLE: ETCH CUT DRAWING							SIZE: D	CODE: DEC	NUMBER: 5013326-0-0	REV: H
SCALE: 2:1	SHEET 2 OF 2						DIST			

DEC 5013326-0-0 H

DEC 5013326-0-0 H

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REVISIONS	
REV.	CHANGE NO.
D	REVISED & REDRAWN M8186-ML0049
E	M8186-ML0046
F	M8186-ML0093
H	M8186-ML0101
CHK	
DRAWN	R. BADEAU, M. TEHRANIAN, GREG OPP 20 MAY 81

DRAWN		FIRST USED ON: KDFII-A
CHK'D		TITLE: KDFII-A CPU (K1)
ENG.		
PROJ.		
PROD.		
NEXT HIGHER ASSY.		
B-DD-M8186-0		SIZE D, CODE CS, NUMBER M8186-0-1, REV. H
SCALE		
SHEET 1 OF 4		DIST

digital

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+5V
R11 5.1K
AE1
SINGLE STEP
K2 65 CLK H
(TP2)
BHI
CLK DIS L
K2 CLK RESTART L
K1 INIT L
K2 START A H
K1 CLK HOLD H
K2 CLK STOP (1) L
K2 E130 H
K2 MME HOLD H
K2 RESET H
K1 CLK STUT H
K2 PRECSEL H
K2 MCLK H
K2 TTL CLK L
R20 10
K2 CHIP CLK H
K2 MCLK L
BIRQ4 L
BIRQ5 L
BIRQ6 L
BIRQ7 L
K2 EVENT H
K4 DAL 12
K4 DAL 11
K4 DAL 10
K4 DAL 09
K4 DAL 08
K4 DAL 05
K4 DAL 07
K4 DAL 01
K1 TIMEOUT H
BHALT L
BPOK H
K2 POK L
K4 DGPO6 L
K1 INIT L
K4 ABORT L
K2 SYMME (0) H
K2 SVC ENA (1) H
K2 SVC ENA (1) L
K2 E65 L
K2 E33 H
K2 PDCLO H
K2 E65 H
K2 E130 H
K2 E195 H
K2 MCLK H
E15 13.824 MH
W1
TP4
R18 180
TP2
R15 180
K2 E130 L
BRI
BEVNT L
E26
W4
K4 DGPO5 L
K1 BUS INIT L
K2 EVENT H
K2 65 CLK H
K2 E33 L
K2 E98 H
K2 E33 H
K2 65 CLK L
(TP1)
(TP4)
R8 22K
R6 620
K4 CSEL L
Q1 3009
R7 2.2K
K1 DINIT L
K2 E65 H
K2 E130 L
K2 PRECSEL H
K2 CTL ERR H
K2 MCLK L
K2 SVC ENA (1) L
R9 15K
K4 ABORT L
K1 BUS ERR H
R17 270
K4 DAL 04
K4 DAL 03
K4 DAL 02
K4 DAL 00
K4 DAL 06
K2 AIO2 ENA H
K2 E163 H
K2 E228 H
K2 E293 H
K2 E358 H
K2 E423 H
K2 E65 H
K2 65 CLK L
K1 DIN H
K3 REC DAL 17
K3 REC DAL 16
R30 1K
R31 1K
K2 PAR ERR H
K2 MCLK CLR L
K2 MCLK H
K1 INIT L
K1 DOUT HOLD L
K2 RESTART END H
K1 BUS CYC L
K1 DMA ENA (0) H
K1 INIT H
K1 REARB B H
K2 65 CLK H
K2 CLK RESTART L
K1 RPLY RESTART L
(TP2)
K1 DINIT L
K2 E65 L
K1 INIT L
K2 PDCLO H
K2 DCLO H
AM2
K2 MMUSTR H
W2
W3
K4 MIB 15
K2 MCLK L
K2 SYMME (1) H
K2 SYMME (0) H
K2 MME HOLD H
K2 65 CLK H
(TP2)
K2 RESET H
K2 E65 H
K2 PAR ERR H
R13 2K
K2 SYNC RESET L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
KDF11-A CPU (K2)	D	CS	M8186-0-1	H
SCALE —	SHEET 2 OF 4	DIST.		

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330/680 TERM E51
BDAL 15 L (BV2) 15
BDAL 14 L (BU2) 14
BDAL 13 L (BT2) 7
BDAL 12 L (BS2) 6
BDAL 11 L (BR2) 13
BDAL 10 L (BP2) 12
BDAL 09 L (BN2) 5
BDAL 08 L (BM2) 4
BDAL 07 L (BL2) 11
BDAL 06 L (BK2) 10
BDAL 05 L (BJ2) 3
BDAL 04 L (BH2) 2
BDAL 03 L (BF2) 9
BDAL 02 L (BE2) 1

330/680 TERM E7
BIRQ 5 L (AA1) 13
BIRQ 6 L (A81) 11
BIRQ 4 L (AL2) 10
BWTBT L (AK2) 9
BDIN L (AH2) 7
BDOUT L (AE2) 6
BIAK L (AN2) 15
BSYNC L (AJ2) 1
BRPLY L (AF2) 4
BDMR L 12
BBS7 L (AP2) 14
BDAL 17 L (ADI) 5
BDAL 16 L (ACI) 2
BHALT L (API) 3

330/680 TERM E42
BDMGO L (AS2) 12
BPOK H (BBI) 11
BDCOK H (BAI) 15
BINIT L (AT2) 14
BDAL 01 L (AV2) 1
BDAL 00 L (AU2) 2
BSACK L (BNI) 3
BEVENT L (BRI) 4
BIRQ 7 L (BPI) 5
BDAL 21 L (BFI) 13
BREF L (ARI) 6
BDAL 20 L (BEI) 10
BDAL 19 L (BDI) 9
BDAL 18 L (BCI) 7

K1 WTBT H
K2 PRECSEL H
74LS75 E27
2908 E37 ODD
AK2 BWTBT L
AP2 BBS7 L
ADI BDAL 17 L
ACI BDAL 16 L
K3 REC DAL 17
K3 REC DAL 16
K3 DAL FF CLK
K3 BDAL ENA L
DRCP BE RLE OE
K1 2908 OE L
K4 DAL 01
K2 MCLK L
K4 DGP07 L
74S02 E33
74LS10 E36
74LS240 E20
K4 BSIO
K4 DAL 17
R5 680
K4 DAL 00
K2 MME HOLD H
K4 DAL 16
R4 680
K4 MIB 06
K1 MIB 07B L
74LS00 E45
K3 ENA BSIO L
+3V
74 J 276 E35 K
K1 INIT L
74LS244 E53
K4 MIB 15
R29 150
K3 DMMUS L
K4 MIB 12
74S240 E4
(TP4)
74S20 E18
K2 E98 H
K2 E33 H
74S241 E13
K2 E130 H
K4 MIB 03
K3 FDIN ENA L
K2 PRECSEL H

+5V
E26
W15
W14
W13
W12
W11
W10
W9
W8
W7
W6
W5
74LS240 E30
K4 DAL 15
K4 DAL 14
K4 DAL 13
K4 DAL 12
K4 DAL 11
K4 DAL 10
K4 DAL 09
K4 DAL 08
74LS240 E20
K2 POK L
K4 DAL 07
K4 DAL 02
K4 DAL 01
K4 DAL 00
K3 FDIN ENA L

2908 E47
K4 DAL 03
K4 DAL 02
K4 DAL 01
K4 DAL 00
BF2 BDAL 03 L
BE2 BDAL 02 L
AV2 BDAL 01 L
AU2 BDAL 00 L

2908 E52
K4 DAL 07
K4 DAL 06
K4 DAL 05
K4 DAL 04
BL2 BDAL 07 L
BK2 BDAL 06 L
BJ2 BDAL 05 L
BH2 BDAL 04 L

2908 E55
K4 DAL 11
K4 DAL 10
K4 DAL 09
K4 DAL 08
BR2 BDAL 11 L
BP2 BDAL 10 L
BN2 BDAL 09 L
BM2 BDAL 08 L

2908 E56
K4 DAL 15
K4 DAL 14
K4 DAL 13
K4 DAL 12
BV2 BDAL 15 L
BU2 BDAL 14 L
BT2 BDAL 13 L
BS2 BDAL 12 L

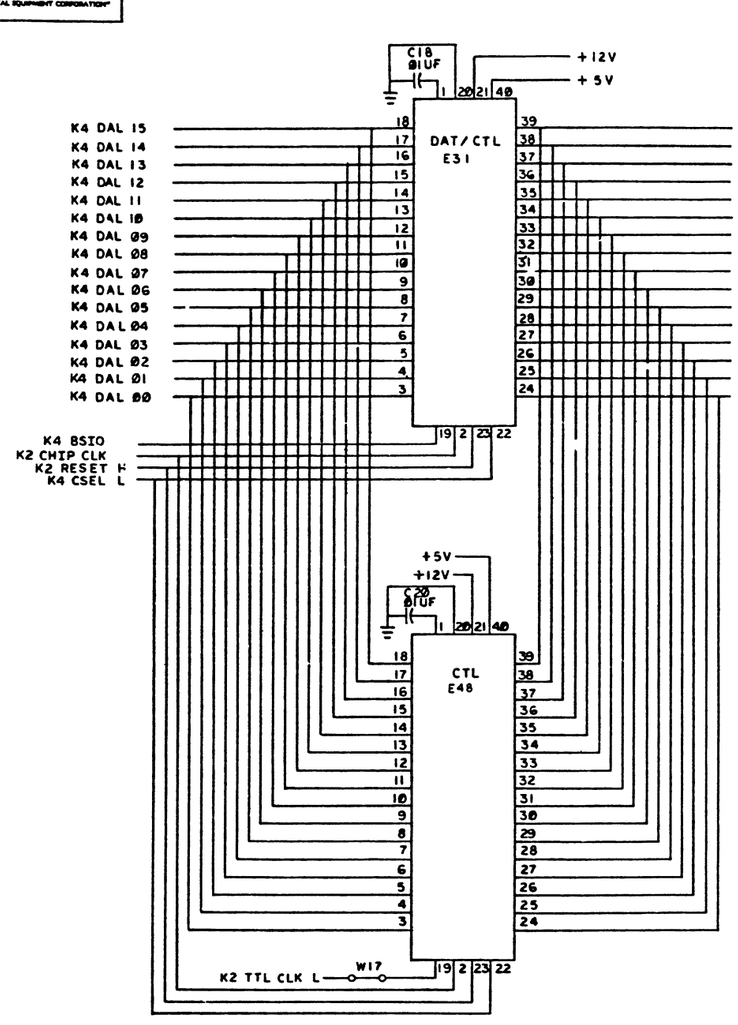
K2 MMUSTR H (AM2)
K2 E163 H
74S32 E32
K3 DAL FF CLK H
K1 2908 OE L
K1 BUS ENA H
K2 E130 L
74 276 E35
K1 BUS DISABLE (1) L
74LS00 E45
K3 BDAL ENA L
K1 INIT L

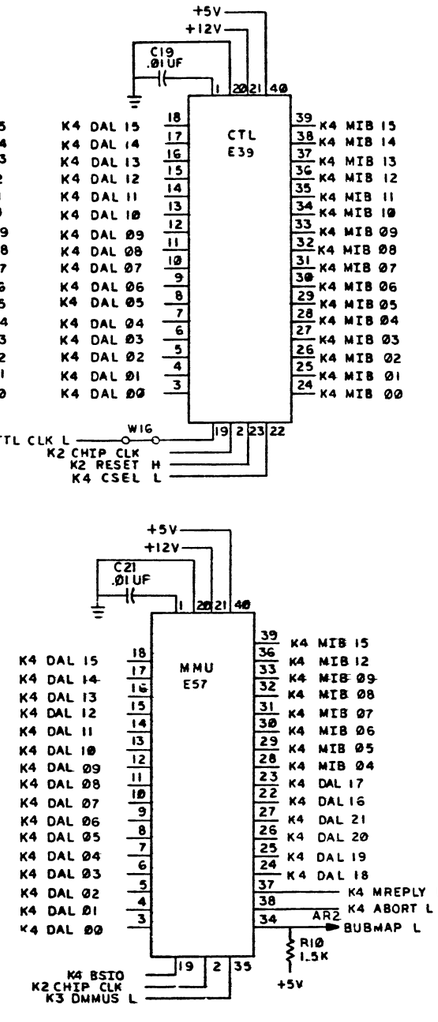
REVISIONS		
CHK	CHANGE NO.	REV

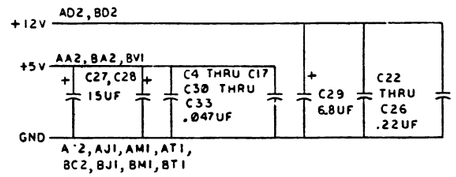
TITLE	KDF11-A CPU (K3)	SIZE	CODE	NUMBER	REV.
		D	CS	M8186-0-1	H
SCALE	SHEET 3 OF 4	DIST.			

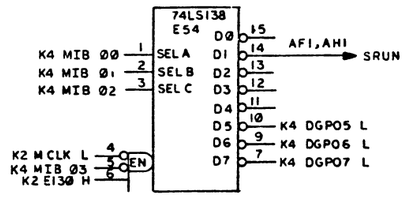
M8186-0-1 H
SIZE D CODE CS NUMBER M8186-0-1 REV H

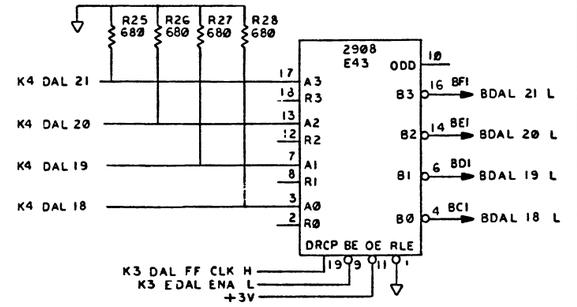
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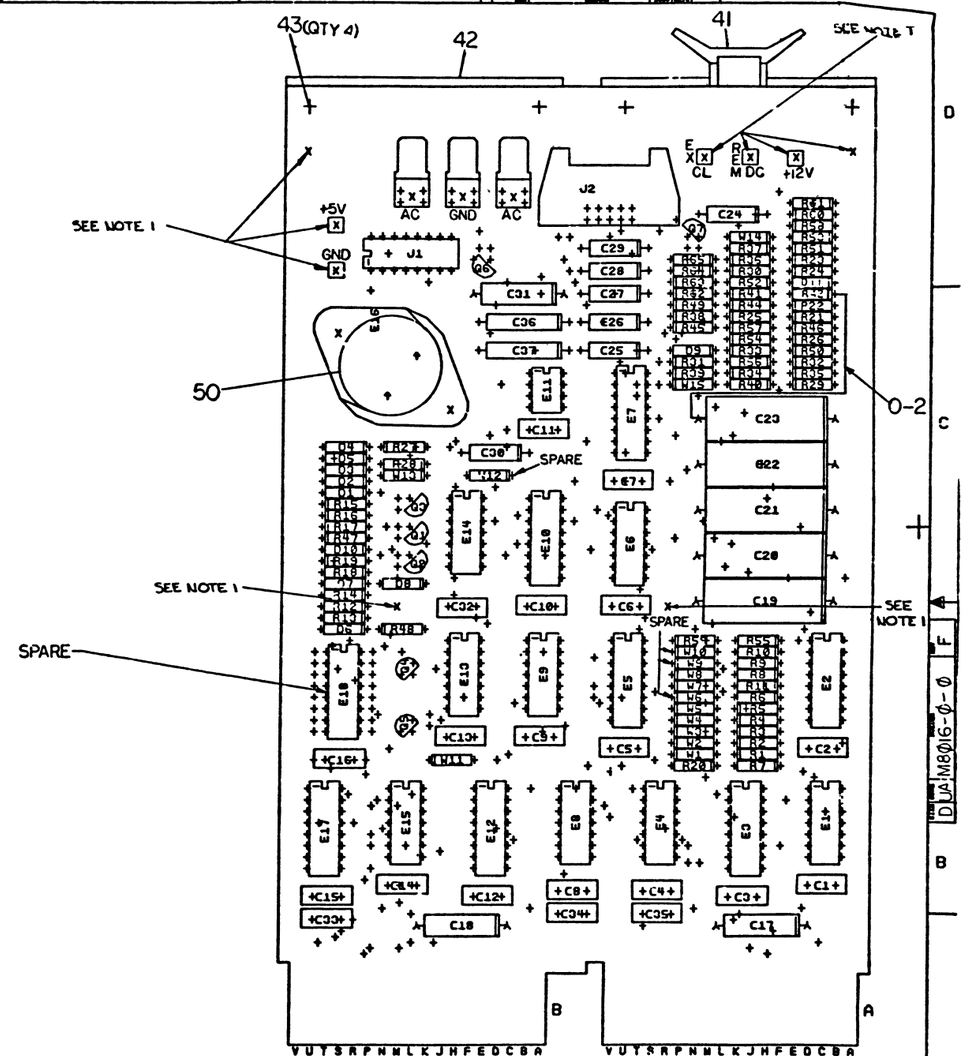
REVISIONS		
CHK	CHANGE NO	REV

TITLE	KDF11 A CPU (K4)	SIZE	CODE	NUMBER	REV.
SCALE	SHEET 4 OF 4	D	CS	M8186-0-1	H
		DIST.			

M8186-0-1 H
D CS

REWORK INSTRUCTION
ETCH CUT SIDE 1
0-1 TO RIGHT SIDE OF R42

WIRE ADD SIDE 1 AS SHOWN
0-2 FROM R42 TO C23



NOTES: 1. FILL "X" HOLES DESIGNATED ON DRAWING WITH SOLDER MASKING COMPOUND BEFORE WAVE SOLDER.
2. E3, E12, E17 ARE OPTIONAL.

CH	CHANGE NO	REV
4	1758	D
5	-	-
6	1810	E
7	1810	F

J. MARTINEZ
MAR 03
R. SALETT

ETCH REV. E
P.C. DESIGN DATA BASE REV. E

SIGNATURES	DATE
DRN.	
CHK'D	
ENG.	
PROJ. ENG.	
PROD.	
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DU-M8016-0	

digital

TITLE POWER FAIL TIME CLOCK GEN

SIZE D | CODE | NUMBER UA M8016-0-0 | REV F

DU-M8016-0-0

MS#104253

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NOTE:
1. UNLESS NOTED OTHERWISE, ALL +5V SOURCES ORIGINATE FROM THE LM309K +5 VOLT REGULATOR (VCC), AND IS REFERENCED TO EARTH (VIRTUAL) GROUND.

HLT L
S SPARE 3
AH1
B HALT L
API
SYS +5V (AA2,BA2)
SEE NOTE #1
T1 AC
T2 GND
T3 AC
01 IN4004
D2 IN4004
D3 IN4004
D4 IN4004
D5 IN4004
D6 IN4004
C22 100uF
C19 100uF
C20 100uF
C21 100uF
C23 100uF
C32 .22uF
C31 8uF
LM309K E18
Q1 MXA05
Q2 MXA05
Q3 MXA05
D7 DG64
-17 V
+5 VCC
DC POWER ON H
LTC ON H
D2 LTC ENB(1) L
D1 LTC OUT H
EX. CL
BR1
BEVNT L
T4 +5V
+5V SYS (AA2)
T6 GND
T5 +12V
+12V SYS AD2
D9 D664
D10 D664
D11 IN748A
R42 10K
Q4 2N5433
Q5 2N5433
Q6 MXA05
Q7 MXA05
DC ON H
BA1 SDCOK H
BB1 BPOK H
REM DC ON L
2-6 MS (PWR ON.) DLY 1
17 MS MIN. (PWR UP) DLY 2
70MS MIN (PWR UP) DLY 3
C29 1.9uF
C24 33uF
C36 39uF
C37 39uF

IAC
AM2 | AN2
DMG
AR2 | AS2
(AC2 ; AJ1 ; AM1 ; AT1)
(BC2 ; BJ1 ; BM1 ; BT1)

NOTE:
UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
IC DEC 75451	8	4
IC DEC 8Ø4Ø	8	1
IC DEC LM339	3	12

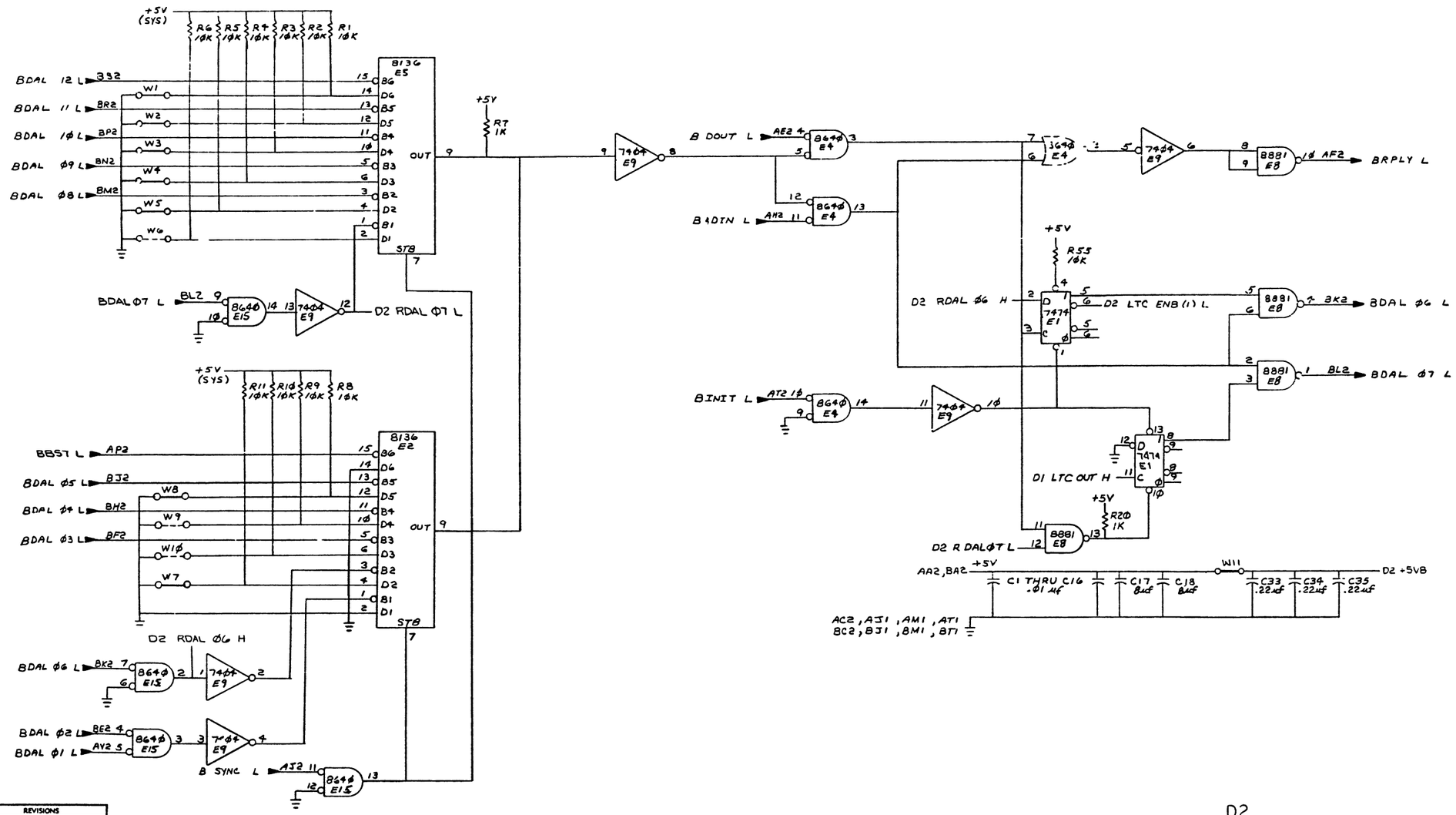
REVISIONS			
CHK	CHANGE NO.		REV.
GH	M8Ø11 (ØØØ1		D
	M8106-HK002		E
	M8Ø16-AB004		F

DRN.	J. HART
CHK'D	
ENG.	J. CURTIS
PROJ. ENG.	
PROD.	
NEXT HIGHER ASSY.	B-DD-M8Ø16-Ø
SCALE	NONE
SHEET	1 OF 3

FIRST USED ON
digital
TITLE PWR FAIL/LINE TIME CLK GENERATOR
SIZE D | CODE CS | NUMBER M8Ø16-Ø-1 | REV. F
DIST.

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NOTE
1 +5V SOURCE FOR LOGIC ON THIS PAGE IS FROM SYSTEM POWER SUPPLY. (AA2, BA2)

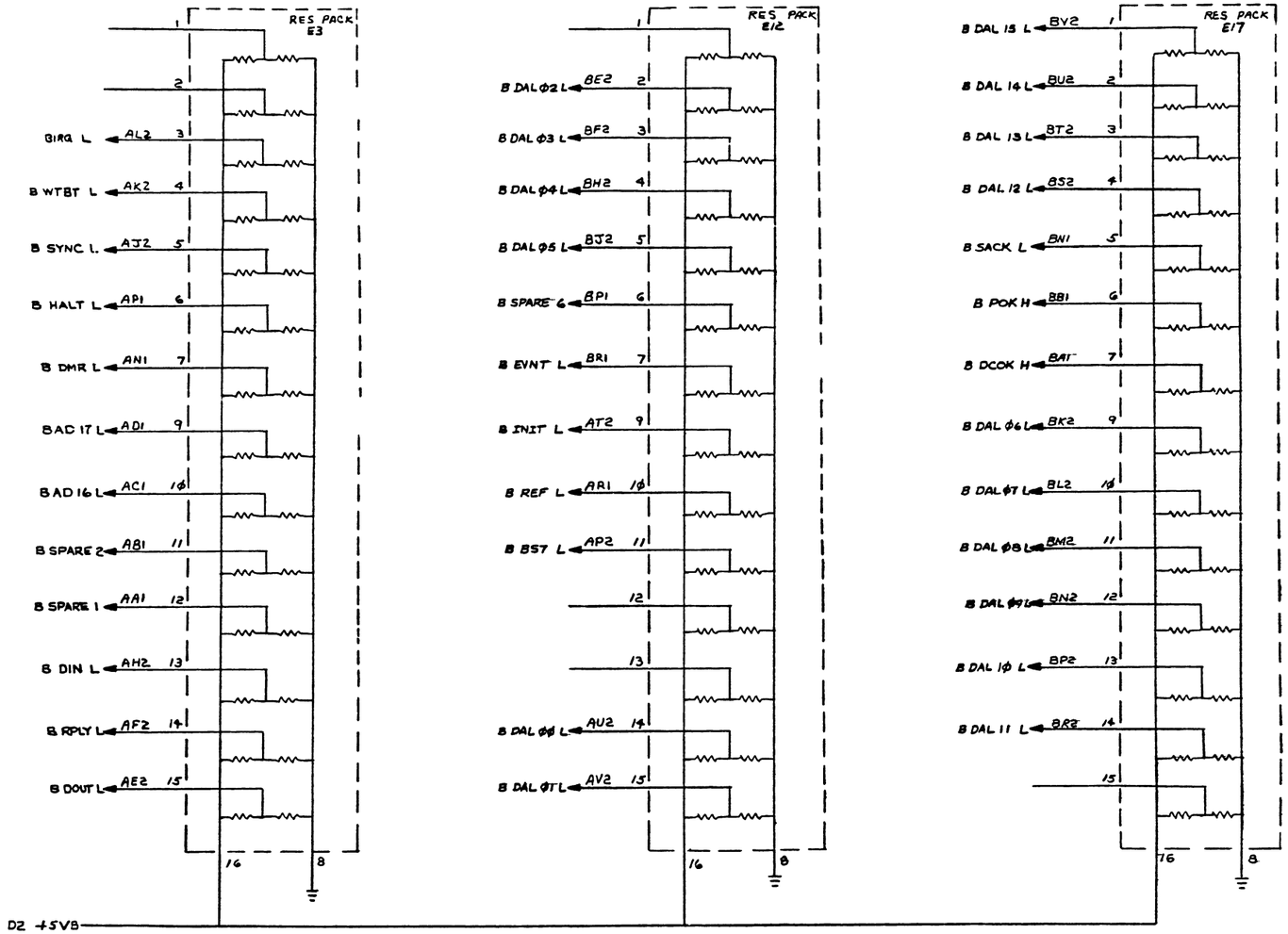


D2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
PWR FAIL/LINE TIME CLK GENERATOR	D	CS	M8Ø16-Ø-1	F
SCALE	SHEET 2 OF 3	DIST.		

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NOTE:
1. CIRCUIT SHOWN WITH OPTIONAL TERMINATION RESISTOR PACKS USED ON M8016-YB (120 NOM) AND M8Ø5-YC (220 NOM).

2. W11 IS FOR VOLTAGE MARGINING
3. +5V SOURCE ON THIS PAGE IS SYSTEM POWER (AA2, BA2).

JUMPER USAGE CHART

JUMPER	INSTALLED	REMOVED
W1	* YES	NO
W2	* YES	NO
W3	* YES	NO
W4	* YES	NO
W5	* YES	NO
W6	NO	* YES
W7	* YES	NO
W8	* YES	NO
W9	NO	* YES
W10	NO	* YES
W11	*VOLTAGE MARGINING	EXTERNAL 5V SOURCE MAY BE USED
W12	ENABLE MANUAL CONTROL OR CONTINUOUS LTC INTERRUPT REQUEST OPERATION. DO NOT INSTALL WHEN W13 IS INSTALLED.	*DISABLE CONTINUOUS OR MANUAL OPERATION
W13	*LTC INTERRUPT REQUESTS CAN BE ENABLED AND DISABLED BY PROGRAM. DO NOT INSTALL WHEN W12 IS INSTALLED.	LTC INTERRUPT REQUESTS CANNOT BE PROGRAM CONTROLLED.
W14	*CONSOLE (OPTIONAL) LTC ON/OFF SWITCH ENABLED.	CONSOLE LTC ON/OFF SWITCH DISABLED.
W15	*LTC SIGNAL OCCURS AT THE POWER LINE FREQUENCY.	LTC FREQUENCY IS DETERMINED BY AN EXTERNAL SOURCE VIA EXT TIME REF ETCHED PAD ON MODULE.

*FACTORY-JUMPERED CONFIGURATION

REVISIONS

CHK	CHANGE NO	REV

D3

TITLE PWR FAIL/LINE TIME CLK GENERATOR
SIZE D CODE CS NUMBER M8Ø16-Ø-1 REV. F
SCALE
SHEET 3 OF 3
DIST.

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MODE	SW1 S1	S2	S3	S4	S5	S6	S7	S8	MICRO ADDRESS RESPONSE
I	ON	OFF	OFF	ON	OFF	ON	OFF	-	MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777
II	OFF	ON	OFF	ON	OFF	OFF	ON	-	INITIAL MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 0-777. TOGGLED MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 1000-1777
III	OFF	OFF	ON	ON	OFF	ON	OFF	-	MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777. THIS IS IDENTICAL TO MODE I, EXCEPT THE TWO 512 WORD BLOCKS OF RAM ARE SWAPPED.
IV	ON	OFF	OFF	OFF	ON	ON	OFF	-	MICRO ADDRESSES 0-1777 CORRESPOND TO WCS RAM ADDRESSES 0-1777

WCS COMMAND/STATUS REGISTER (177540)

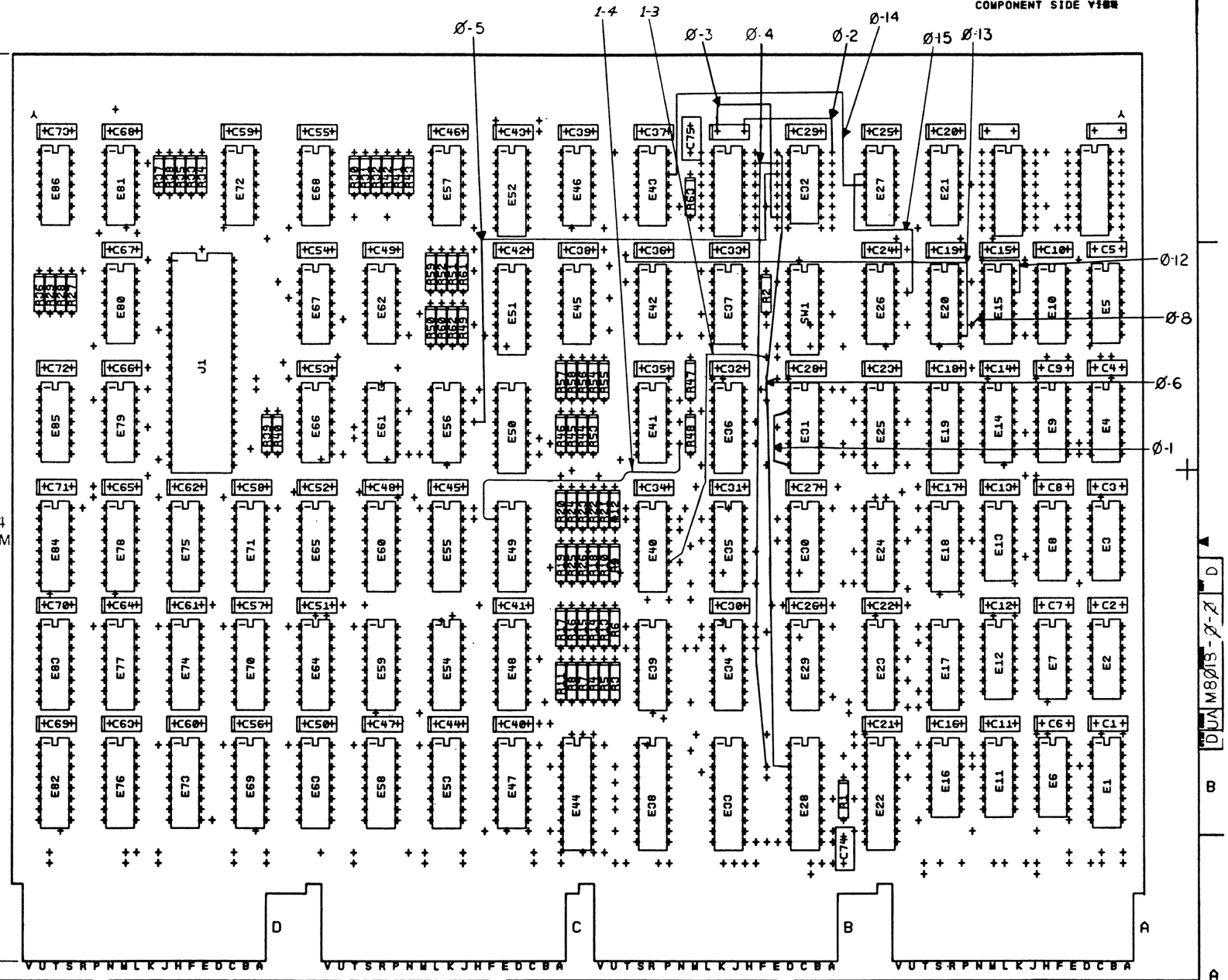
BIT	FUNCTION
15	WHEN SET TO A 1 THE TRACE RAM ADDRESS IS INITIALIZED TO Ø AND THE PAGING LOGIC IS INITIALIZED TO THE LOWER 512 WORDS OF RAM, SUBSEQUENTLY CLEARING THIS BIT TO A Ø ENABLES THE TRACE RAM AND PAGING LOGIC.
14	WHEN SET TO A 1, THE DATA AT THE CURRENT TRACE RAM LOCATION CAN BE READ (ONLY) AT ADDRESS 177542.
13	WHEN SET TO A 1 AND THEN CLEARED TO A Ø, THE NEXT TRACE RAM LOCATION IS ADDRESSED TO BE ACCESSED USING CSR BIT (14).
12	WHEN SET TO A 1, THE WCS IS ENABLED TO RESPOND TO THE LSI-11 MID. WHEN CLEARED TO A Ø, THE WCS WILL NOT RESPOND TO THE LSI-11 MIB AND THE RAM LOCATION POINTED TO BY CSR BITS 9:Ø CAN BE READ OR WRITTEN (RAM BITS <23:16> AT 177544 AND RAM BITS <15:Ø> AT 177542).
11-1Ø	UNUSED, WILL ALWAYS BE READ AS CLEARED TO Ø.
9-Ø	THE WCS RAM ADDRESS THAT CAN BE ACCESSED WHEN BITS <14,12> ARE CLEARED TO A Ø.

2115-02	8	16
74298	8	16
74174	8	16
74LS253	8	16
74193	8	16
7483	8	16
8640	1	8
74148	8	16
SD5101	4	11
DC005	10	20
DC004	10	20
ICTYPE	GND	+5V

GND AND +5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

8.44
214.37MM
P.B.S.



NOTES:
Ø-1: ADD WIRE FROM E31-3 TO E31-8.
Ø-2: ADD WIRE FROM E32-14 TO NEAR CAPACITOR PAD OVER SPARE IC LEFT OF E32.
Ø-3: ADD WIRE FROM E32-7 TO FAR CAPACIATOR PAD OVER SPARE IC LEFT OF E32.
Ø-4: ADD WIRE FROM E32-2 TO PTH RIGHT OF E33-18
Ø-5: ADD WIRE FROM E32-3 TO PTH LEFT OF E50-4
Ø-6: ADD WIRE FROM E32-1 TO E28-3.
1-3: FROM E40-11 TO PTH TO THE RIGHT OF C32.

CHK	CHANGE NO	REV
PC M8018-0000	11	C

J. Clarke
A. DRINKARD
J. Munk 7-JUN-78
COMPOSITE L004 D
Ø-8: ADD WIRE FROM E15-5 TO PTH LEFT OF E15-6.
~~Ø-9: SIDE 2 ETCH CUT FROM E15-4 AND PTH ABOVE E15-4.~~
~~Ø-10: SIDE 1 ETCH AFTER PTH ABOVE LEFT OF E42-1.~~
~~Ø-11: SIDE 1 ETCH CUT AFTER E43-12.~~
Ø-12: ADD WIRE FROM E15-12 TO PTH ABOVE E15-1.
Ø-13: ADD WIRE FROM E20-8 TO PTH ABOVE LEFT OF E42-1.
Ø-14: ADD WIRE FROM E27-4 TO E43-12.
Ø-15: ADD WIRE FROM E27-3 TO PTH RIGHT OF E26-12.
1-4: FROM E49-2 TO PTH TO THE RIGHT OF E49.

BOARD FABRICATION INFORMATION
PANEL SIZE
PANEL DATA DWG.#
PANEL MAT'L
QTY. OF LAYERS
COPPER THICKNESS
PTH. X PRINT AND ETCH
MODULE INSERTED 100 TIMES OR MORE?

SIGNATURES	DATE
DRN. [illegible]	12-22-76
CHK'D. [illegible]	1-6-77
ENG. A. Drinkard	8-22-77
PROJ.ENG. A. Drinkard	8-22-77
PROD. [illegible]	12-1-77
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M8018-Ø	

digital

TITLE WRITEABLE CONTROL STORE

SIZE	CODE	NUMBER	REV
D	UA	M8018-Ø-Ø	D

ETCH REV. C-P1

MS#

DUA M8018-Ø-Ø D

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MIB INTERFACE TRANSCIEVERS

K-1 OUT ØØ H → R62 47Ω → +5V → K-1 REC ØØ H
K-1 MIB ØØ L → K-1 MIB ØØ L
K-1 OUT Ø1 H → R61 47Ω → +5V → K-1 REC Ø1 H
K-1 MIB Ø1 L → K-1 MIB Ø1 L
SD5101 E67

K-1 OUT Ø2 H → R60 47Ω → +5V → K-1 REC Ø2 H
K-1 MIB Ø2 L → K-1 MIB Ø2 L
K-1 OUT Ø3 H → R59 47Ω → +5V → K-1 REC Ø3 H
K-1 MIB Ø3 L → K-1 MIB Ø3 L
SD5101 E62

K-1 OUT Ø4 H → R52 47Ω → +5V → K-1 REC Ø4 H
K-1 MIB Ø4 L → K-1 MIB Ø4 L
K-1 OUT Ø5 H → R51 47Ω → +5V → K-1 REC Ø5 H
K-1 MIB Ø5 L → K-1 MIB Ø5 L
SD5101 E37

K-1 OUT Ø6 H → R50 47Ω → +5V → K-1 REC Ø6 H
K-1 MIB Ø6 L → K-1 MIB Ø6 L
K-1 OUT Ø7 H → R49 47Ω → +5V → K-1 REC Ø7 H
K-1 MIB Ø7 L → K-1 MIB Ø7 L
SD5101 E56

K-1 OUT Ø8 H → R48 47Ω → +5V → K-1 REC Ø8 H
K-1 MIB Ø8 L → K-1 MIB Ø8 L
K-1 OUT Ø9 H → R47 47Ω → +5V → K-1 REC Ø9 H
K-1 MIB Ø9 L → K-1 MIB Ø9 L
SD5101 E61

K-1 OUT 1Ø H → R46 47Ω → +5V → K-1 REC 1Ø H
K-1 MIB 1Ø L → K-1 MIB 1Ø L
K-1 OUT 11 H → K-1 MIB 11 L
K-1 OUT 12 H → K-1 MIB 12 L
SD5101 E66

K-1 OUT 13 H → K-1 MIB 13 L
K-1 OUT 14 H → K-1 MIB 14 L
K-1 OUT 15 H → K-1 MIB 15 L
K-1 OUT 16 H → K-1 MIB 16 L
SD5101 E80

K-1 OUT 17 H → R39 47Ω → +5V → K-1 REC 16 H
K-1 MIB 16 L → K-1 MIB 17 L
K-1 OUT 18 H → K-1 MIB 18 L
K-1 OUT 19 H → K-1 MIB 19 L
SD5101 E79

K-1 OUT 2Ø H → K-1 MIB 2Ø L
K-1 OUT 21 H → K-1 MIB 21 L
SD5101 E85

MIB DATA OUT SELECTION

+5V
R58 27Ω R57 27Ω R56 27Ω
K-4 DOUT ØØ H
K-6 PØ1 H
K-6 DABL L
74S15 E45
K-1 OUT ØØ H
K-4 DOUT Ø1 H
K-1 OUT Ø1 H
K-4 DOUT Ø2 H
K-1 OUT Ø2 H

+5V
R55 27Ω R54 27Ω R53 27Ω
K-4 DOUT Ø3 H
74S15 E42
K-1 OUT Ø3 H
K-4 DOUT Ø4 H
K-1 OUT Ø4 H
K-4 DOUT Ø5 H
K-1 OUT Ø5 H

+5V
R46 27Ω R45 27Ω R44 27Ω
K-4 DOUT Ø6 H
74S15 E41
K-1 OUT Ø6 H
K-4 DOUT Ø7 H
K-1 OUT Ø7 H
K-4 DOUT Ø8 H
K-1 OUT Ø8 H

+5V
R43 27Ω R42 27Ω R41 27Ω
K-4 DOUT Ø9 H
K-6 PØ1 H
K-6 DABB L
74S15 E57
K-1 OUT Ø9 H
K-4 DOUT 1Ø H
74 E5.
K-1 OUT 1Ø H
K-4 DOUT 11 H
74S15 E57
K-1 OUT 11 H

+5V
R32 27Ω R31 27Ω R3Ø 27Ω
K-4 DOUT 12 H
K-6 PØ1 H
K-6 DABB L
74S15 E68
K-1 OUT 12 H
K-4 DOUT 13 H
K-1 OUT 13 H
K-4 DOUT 14 H
74S15 E68
K-1 OUT 14 H

+5V
R35 27Ω R34 27Ω R33 27Ω
K-4 DOUT 15 H
74S15 E72
K-1 OUT 15 H
K-3 DOUT 16 H
K-1 OUT 16 H
K-3 DOUT 17 H
74S15 E72
K-1 OUT 17 H

+5V
R38 27Ω R37 27Ω R36 27Ω
K-1 LOUT 18 H
K-6 DABC L
K-6 P23 H
74S15 E81
K-1 OUT 18 H
K-1 LOUT 19 H
K-1 OUT 19 H
K-1 LOUT 2Ø H
74S15 E81
K-1 OUT 2Ø H

+5V
R29 27Ω
K-1 LOUT 21 H
74S15 E86
K-1 OUT 21 H

74174 E52
K-3 DOUT 18 H → D0 R0(1)
K-3 DOUT 19 H → D1 R1(1)
K-3 DOUT 2Ø H → D2 R2(1)
K-3 DOUT 21 H → D3 R3(1)
K-3 DOUT 22 H → D4 R4(1)
K-3 DOUT 23 H → D5 R5(1)
CLR CLK
K-6 DABL L
K-6 PØ1 H

K-1 LOUT 18 H
K-1 LOUT 19 H
K-1 LOUT 2Ø H
K-1 LOUT 21 H
74S11 E46
K-6 PØ2 H
74Ø7 E14
12 AE1 → K-1 SROM 4 H
15 AF1 → K-1 SROM 5 H

+5PP
74S74 E93
K-1 PAGE H
74S11 E96
K-6 CSR 15 L

PAGING LOGIC AND USER BITS

J1
K-1 MIB ØØ L
K-1 MIB Ø1 L
K-1 MIB Ø2 L
K-1 MIB Ø3 L
K-1 MIB Ø4 L
K-1 MIB Ø5 L
K-1 MIB Ø6 L
K-1 MIB Ø7 L
K-1 MIB Ø8 L
K-1 MIB Ø9 L
K-1 MIB 1ØL
K-1 MIB 11L
K-1 Ø2 H
K-1 Ø4 H
K-1 MIB 15L
K-1 MIB 14L
K-1 MIB 13L
K-1 MIB 12L
K-1 MIB 16L
K-1 MIB 17L
K-1 MIB 18L
K-1 MIB 19L
K-1 MIB 2ØL
K-1 MIB 21L

(K-1)

REVISIONS			
SYM	CHANGE NO.	REV.	
PC	M8018-00001	C	J. Clark 15 MAR 76
PC	M8018-ML002	D	A. DRINKARD 2-NOV-76
			J. W. CURTIS 2 Sept 77
PC	M8018 ML004	E	K. Cain 26 Sept 77
			K. Bassett 28 NOV 77
			JOHN CURTIS

DRN. D. Vincent	8-3-76	FIRST USED ON
CHK'D		
ENG. A. D. Vincent	8-22-77	
PROJ. ENG. A. D. Vincent	8-22-77	
PROD.	12-1-77	
NEXT HIGHER ASSY.		
SCALE		
SHEET 1 OF 6		

TITLE: WRITEABLE CONTROL STORE (WCS-LSI-11)

SIZE	CODE	NUMBER	REV.
D	CS	M8Ø18-Ø-1	E
DIST.			

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DAL BUS TIMING AND SELECTION

K-2 B DAL Φ0 L
K-2 B DAL Φ4 L
K-2 B DAL Φ5 L
K-2 B DAL Φ6 L
AV2 BH2 EJ2 BK2
DCΦΦ5 E44
BUS Φ JA1 BUS 1 JA2 BUS 2 JA3 BUS 3
DAT Φ JV1 DAT 1 JV2 DAT 2 JV3 DAT 3
MENB XMIT RAC MATCH
K-2 TSB Φ0 H
K-2 TSB Φ4 H
K-2 TSB Φ5 H
K-2 TSB Φ6 H

K-2 B DAL Φ1 L
K-2 B DAL Φ7 L
K-2 B DAL Φ8 L
K-2 B DAL Φ9 L
AV2 BL2 BM2 BN2
DCΦΦ5 E38
K-2 TSB Φ1 H
K-2 TSB Φ7 H
K-2 TSB Φ8 H
K-2 TSB Φ9 H

K-2 B DAL Φ2 L
K-2 B DAL 1Φ L
K-2 B DAL 11 L
K-2 B DAL 12 L
BE2 BP2 BR2 BS2
DCΦΦ5 E33
K-2 TSB Φ2 H
K-2 TSB 1Φ H
K-2 TSB 11 H
K-2 TSB 12 H

K-2 B DAL 15 L
K-2 B DAL 13 L
K-2 B DAL 14 L
K-2 B DAL Φ3 L
BV2 BT2 BU2 AF2
DCΦΦ5 E28
K-2 TSB 15 H
K-2 TSB 13 H
K-2 TSB 14 H
K-2 TSB Φ3 H

K-2 BS7 L
+5 PP

K-2 SEL Φ L
K-2 SEL 2 L
K-2 SEL 4 L
74S10 E2

+5 PP
K-2 XMIT H
74S10 E2

K-2 TSB Φ2 H
K2 TSB Φ1 H
74Φ1 E32
A5V
R1 1K
C74 Ø.Ø1μF

K-2 SYNC L
K-2 B DAL Φ2 L
K-2 B DAL Φ1 L
K-2 B DAL ΦΦ L
K-2 BWTBT L
K-2 B DOUT L
K-2 B DIN L
AF2 AE2 AH2
B SYNC B DAL 2 B DAL 1 B DAL Φ BWTBT B DOUT B DIN
DCΦΦ4 E22
B APLY SEL 6 SEL 4 SEL 2 SEL Φ OUT HB OUT LB INWD ENB RXCX VECTOR H
AF2 K-2 B APLY L
K-2 SEL 4 L
K-2 SEL 2 L
K-2 SEL Φ L
K-2 OUT HB L
K-2 OUT LB L
K-2 XMIT L
K-2 XMIT H

K-6 MIC H
7407 E3
7427 E8
SEL 4 H
K-2 CE B L
K-2 CE A L
K-2 SEL 2 H
K-6 SØ2 L
K-2 LDLB H
K-6 MIC L
74S51 E9
K-2 CKLB L
K-2 LDHB H
K-2 CKHB L
7432 E6
7432 E7
K-2 34LB L
K-2 S2HB L
K-2 S2LB L
K-2 LDNB L
7Ø4 E11
K-2 LDHB H
K-2 LDLB L
K-2 LDLB H
K-2 X XMIT L
K-2 DCOK L
8640 E16
K-2 B DCOK H
K-2 DCOK H
K-2 B BS7 L
K-2 B SYNC L
K-2 BS7 L
K-2 SYNC L
K-2 SYNC H

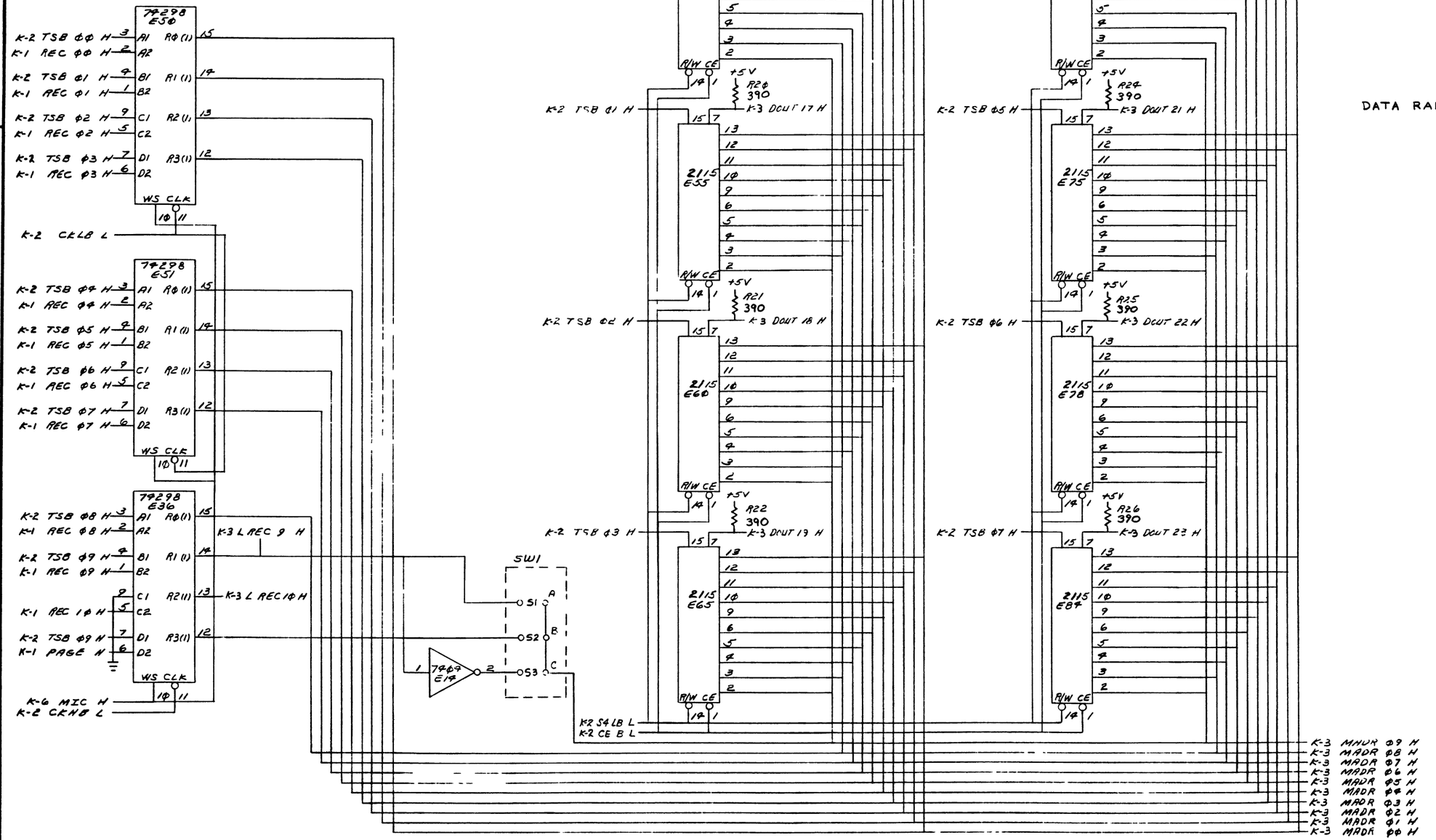
REVISIONS
CHK | CHANGE NO. | REV.

TITLE WRITEABLE CONTROL STORE (WCS-LSI-11)
SIZE D CODE CS NUMBER M8Ø18-Ø-1 REV. E
SCALE SHEET 2 OF 6 DIST.

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RAM ADDRESS MUX AND LATCH

DATA RAMS



REVISIONS		
CHK	CHANGE NO.	REV.

(K-3)

TITLE	SIZE	CODE	NUMBER	REV.
WRITEABLE CONTROL STORE (WCS-LSI-11)	D	DCS	M8018-0-1	E
SCALE	SHEET 3 OF 6	DIST.		

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DATA RAMS

K-2 TSB Ø0 H — K-4 DOUT Ø0 H — R3 390 +5V — 2115 E97
K-2 TSB Ø1 H — K-4 DOUT Ø1 H — R4 390 +5V — 2115 E53
K-2 TSB Ø2 H — K-4 DOUT Ø2 H — R5 390 +5V — 2115 E58
K-2 TSB Ø3 H — K-4 DOUT Ø3 H — R6 390 +5V — 2115 E63
K-2 TSB Ø4 H — K-4 DOUT Ø4 H — R7 390 +5V — 2115 E69
K-2 TSB Ø5 H — K-4 DOUT Ø5 H — R8 390 +5V — 2115 E73
K-2 TSB Ø6 H — K-4 DOUT Ø6 H — R9 390 +5V — 2115 E76
K-2 TSB Ø7 H — K-4 DOUT Ø7 H — R10 390 +5V — 2115 E82
K-2 TSB Ø8 H — K-4 DOUT Ø8 H — R11 390 +5V — 2115 E78
K-2 TSB Ø9 H — K-4 DOUT Ø9 H — R12 390 +5V — 2115 E54
K-2 TSB 10 H — K-4 DOUT 10 H — R13 390 +5V — 2115 E59
K-2 TSB 11 H — K-4 DOUT 11 H — R14 390 +5V — 2115 E67
K-2 TSB 12 H — K-4 DOUT 12 H — R15 390 +5V — 2115 E70
K-2 TSB 13 H — K-4 DOUT 13 H — R16 390 +5V — 2115 E74
K-2 TSB 14 H — K-4 DOUT 14 H — R17 390 +5V — 2115 E77
K-2 TSB 15 H — K-4 DOUT 15 H — R18 390 +5V — 2115 E83

Each 2115 RAM: pins 15, 7, 13, 12, 11, 10, 9, 6, 5, 4, 3, 2; R/W CE; +5V; 14, 1

K-2 CE A L
K-2 S2 L0 L
K-2 S2 H0 L

K-3 MADR Ø9 H
K-3 MADR Ø8 H
K-3 MADR Ø7 H
K-3 MADR Ø6 H
K-3 MADR Ø5 H
K-3 MADR Ø4 H
K-3 MADR Ø3 H
K-3 MADR Ø2 H
K-3 MADR Ø1 H
K-3 MADR Ø0 H

(K-4)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV
WRITEABLE CONTROL STORE (WCS-LST-11)	D	DCS	M8Ø18-Ø-1	E
SCALE	SHEET 4 OF 6	DIST.		

M8Ø18-Ø-1 REV E

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DAL OUTPUT MUX's (TO DCØØ5's)

K-2 XXMIT L

K-5 SA Ø0 H
K-3 MADR Ø0 H
K-4 DOUT 00 H
K-3 DOUT 16 H
→ K-2 TSB ØØ H

K-5 SA Ø1 H
K-3 MADR Ø1 H
K-4 DOUT Ø1 H
K-3 DOUT 17 H
→ K-2 TSB Ø1 H

K-5 SA Ø2 H
K-3 MADR Ø2 H
K-4 DOUT Ø2 H
K-3 DOUT 18 H
→ K-2 TSB Ø2 H

K-5 SA Ø3 H
K-3 MADR Ø3 H
K-4 DOUT Ø3 H
K-3 DOUT 19 H
→ K-2 TSB Ø3 H

K-5 SA Ø4 H
K-3 MADR Ø4 H
K-4 DOUT Ø9 H
K-3 DOUT 20 H
→ K-2 TSB Ø4 H

K-5 SA Ø5 H
K-3 MADR Ø5 H
K-4 DOUT Ø5 H
K-3 DOUT 21 H
→ K-2 TSB Ø5 H

K-5 SA Ø6 H
K-3 MADR Ø6 H
K-4 DOUT Ø6 H
K-3 DOUT 22 H
→ K-2 TSB Ø6 H

K-5 SA Ø7 H
K-3 MADR Ø7 H
K-4 DOUT Ø7 H
K-3 DOUT 23 H
→ K-2 TSB Ø7 H

K-6 SEL B H
K-6 SEL A H

K-5 SA Ø8 H
K-3 MADR Ø8 H
K-4 DOUT Ø8 H
→ K-2 TSB Ø8 H

K-5 SA Ø9 H
K-3 LREC 9 H
K-4 DOUT Ø9 H
→ K-2 TSB Ø9 H

K-5 SA 10 H
K-4 DOUT 10 H
→ K-2 TSB 10 H

K-5 SA 11 H
K-6 CSR 11 H
K-4 DOUT 11 H
→ K-2 TSB 11 H

K-5 SA 12 H
K-6 CSR 12 H
K-4 DOUT 12 H
→ K-2 TSB 12 H

K-5 SA 13 H
K-6 CSR 13 H
K-4 DOUT 13 H
→ K-2 TSB 13 H

K-5 SA 14 H
K-6 CSR 14 H
K-4 DOUT 14 H
→ K-2 TSB 14 H

K-5 SA 15 H
K-6 CSR 15 H
K-4 DOUT 15 H
→ K-2 TSB 15 H

All MUX's: STBI STBØ, AØ BØ CØ DØ, fØ, AI BI CI DI, f1, S1 SØ — 74LS253 E39 / E29 / E23 / E24 / E49 / E34 / E35 / E30

TRACE MODE LOGIC

K-6 STWE H → 74SØ4 E27 → K-6 WE L
K-6 WE L, +5PP → 74S11 E21

74193 E25 (CRY BRW, DØ D1 D2 D3, RØ(1) R1(1) R2(1) R3(1), CLR LD CUP CDN)
K-6 CSR 15 H
+5PP
K-6 CKUP L
K-6 CKDN L

74S189 E17 (WR ENB, DØ D1 D2 D3, MØ(1) M1(1) M2(1) M3(1), A1 A2 A3 AØ)
K-3 MADR ØØ H
K-3 MADR-Ø1 H
K-3 MADR Ø2 H
K-3 MADR Ø3 H
→ 74SØ4 E12 → K-5 SA ØØ H, K-5 SA Ø1 H, K-5 SA Ø2 H, K-5 SA Ø3 H

74S189 E18
K-3 MADR Ø4 H
K-3 MADR Ø5 H
K-3 MADR Ø6 H
K-3 MADR Ø7 H
→ 74SØ4 E12 → K-5 SA Ø4 H, K-5 SA Ø5 H
→ 74SØ4 E13 → K-5 SA Ø6 H, K-5 SA Ø7 H

74S189 E19
K-3 MADR Ø8 H
K-3 MADR Ø9 H
K-6 LREC 10 H
K-6 DABL L
K-5 SA 12 H
K-5 SA 13 H
K-5 SA 14 H
K-5 SA 15 H
→ 74SØ4 E13 → K-5 SA Ø8 H, K-5 SA Ø9 H, K-5 SA 10 H, K-5 SA 11 H

SEL BH	SEL AH	OUTPUT
Ø	Ø	TRACE
Ø	1	CSR
1	Ø	LO WORD
1	1	HI WORD

(K-5)

REVISIONS		
CHK	CHANGE NO	REV

TITLE: WRITEABLE CONTROL STORE (WCS-LSI-11)
SIZE D | CODE CS | NUMBER M8Ø18-Ø-1 | REV. E
SCALE — H | SHEET 5 OF 6 | DIST.

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DAL OUTPUT MUX SELECTION

K-2 SEL 2 L
K-6 CSR 14 H
7432 E4
K-6 SE2 L
74S04 E5
74148 E1
K-2 SEL Ø L
K-6 SL2 L
K-2 SEL 4 L
I3 I2 I1 IØ A1 AØ
K-6 SEL B H
K-6 SEL A H

CONTROL/STATUS REGISTER

74174 E31
D0 D1 D2 D3 D4 D5 CLK CLR
R0(1) R1(1) R2(1) R3(1) R4(1) R5(1) CLR
K-6 CSR11 H
K-2 TSB 12 H
K-2 TSB 13 H
K-2 TSB 14 H
K-2 TSB 15 H
K-2 LDHB H
K-6 MIC H
K-6 CSR 12 H
K-6 CSR 13 H
K-6 CSR 14 H
K-6 CSR 15 H
K-6 STOP H
7432 E4
74S04 E5
K-6 R01 H
K-6 R02 H
74S00 E26
K-6 WE L
K-6 CKUP L
K-6 CKDN L

MIB I/O TIMING

SW1
K-3 LREC 1Ø H
K-3 LREC 9 H
+5PP
K-6 RC 1Ø H
74S04 E5
K-1 REC 16 H
74S10 E2
74S00 E26
74S74 E27
K-6 MIBE L
K-6 HOOK H
K-6 MIC H
K-6 MIC L
K-2 DCOK H
74S74 E2Ø
K-6 DABL L
K-6 DABC L
K-6 DABB L
AM2 AN2
CM2 CN2
AR2 AS2
CR2 CS2

+5V
R2 47Ø
+5PP
+5V AA2, BA2, CA2, DA2
C1 THRU C73 .22 uf
AC2, AJ1, AM1, AT1
BC2, BJ1, BM1, BT1
CC2, CJ1, CM1, CT1
DC2, DJ1, DM1, DT1

K-1 Ø4 H
K-6 P04 L
K-6 P04 H
K-6 R04 L
K-6 R04 H
K-6 P23 H
K-6 R01 L
K-6 R01 H
K-6 MIBE H
K-6 CSR 11 H
K-6 STOP H
K-3 DOUT 23 H
K-6 STWE H
74S11 E46
R63 47Ø
C75 47PF

K-1 Ø2 H
K-6 P02 L
K-6 P02 H
K-6 R02 L
K-6 R02 H
K-6 S02 L
74S04 E15
74Ø4 E14
74S74 E1Ø
PØ1 H

K-6 CSR 15 H
K-6 CSR 15 L

SPARE LOGIC

NOTE:
THERE ARE THREE SPARE I.C. LOCATIONS

74S04 E5
74Ø4 E11
74S74 E2Ø
7427 E8
74S11 E21
74S15 E86
R28 27Ø
R27 27Ø
SD5101 E85
8640 E16
74Ø1 E32
SW1 0580

(K-6)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
WRITEABLE CONTROL STORE (WCS-LSI-11)	D	CS	M8Ø18-Ø-1	E
SCALE —H—	SHEET 6 OF 6	DIST.		

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ECO #2
REWORK INSTRUCTIONS

ETCH CUTS, SIDE 2 AS SHOWN

2-1 AT E45(3)
2-2 AT PTH TO THE LEFT OF J1(B)
2-3 ON ETCH TO THE LEFT OF J1(B)
2-4 AT E45(2)

WIRE ADDS SIDE 1, AS SHOWN

2-5 E45(3) TO PTH TO THE RIGHT OF J1(B)
2-6 E45(2) TO PTH TO THE LEFT OF D4

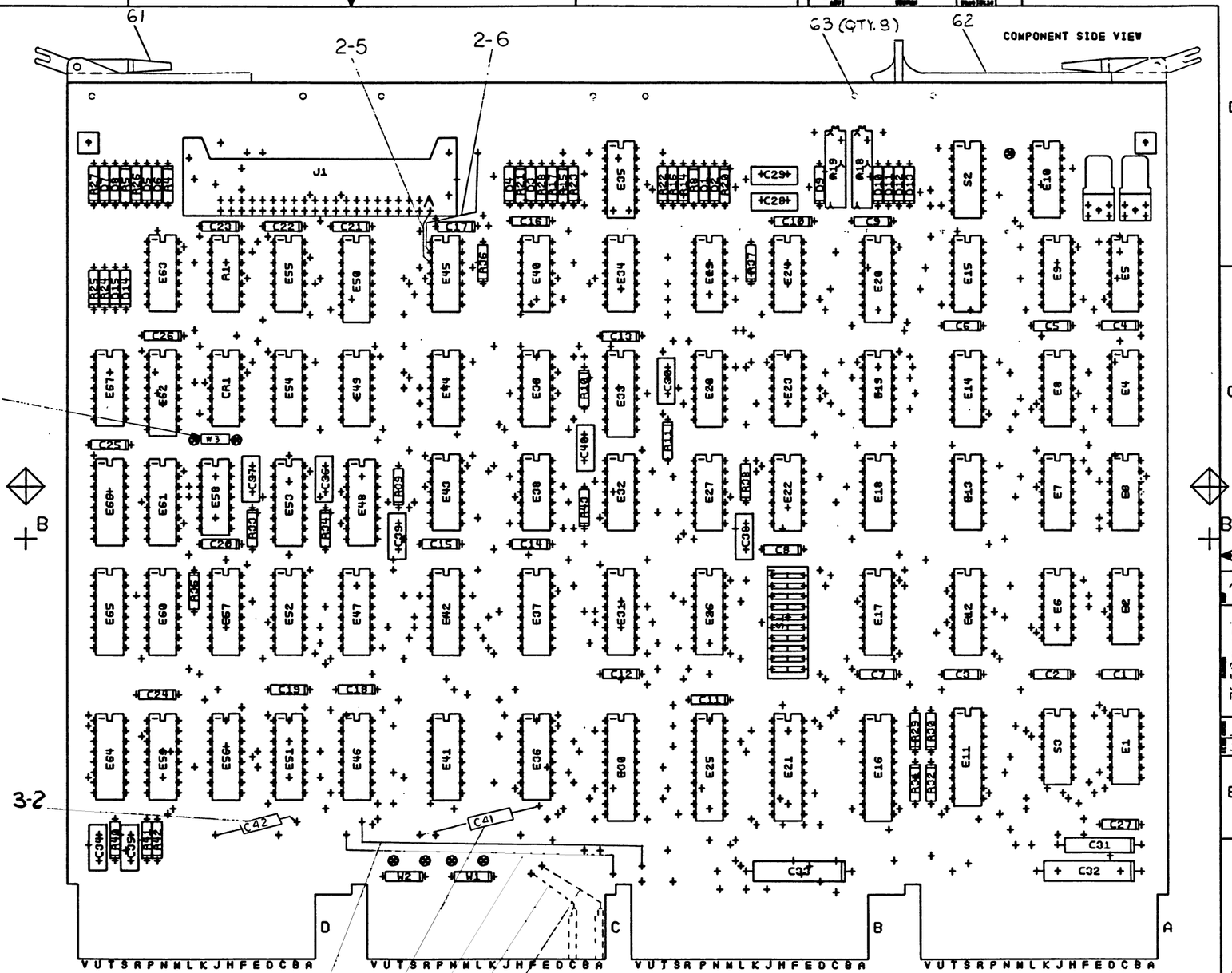
ECO #3
REWORK INSTRUCTIONS

COMPONENT **ADDS**, SIDE 1 AS SHOWN:
3-1 C41 FROM PTH BELOW E36 TO PTH BELOW E41
3-2. C42 FROM PTH BELOW E51 TO PTH BELOW E56

WIRE ADDS, SIDE 1 AS SHOWN:
3-3 FROM PTH BELOW E30-10 TO PTH BELOW E46 (USING ITEM #71)
3-4 FROM PTH BELOW E30-11 TO PTH BELOW E46 (USING ITEM #72)

WIRE ADDS, SIDE 2 AS SHOWN:
3-5 FROM CA2 TO PTH ABOVE CE2 (USING ITEM #72)
3-6 FROM CC2 TO PTH ABOVE CF2 (USING ITEM #71)

SEE NOTE 1



NOTES: 1. W3 INSERTED AFTER GR TEST.

CHG	CHANGE NO.	REV
	WITHDRAWN	B
		C
	M4003	

J. ZEMON
M7952 MRV D
A-FIL
22-FEB-79

ETCH REV. BP1
P.C. DESIGN DATA BASE REV.

SIGNATURES	DATE
DRN.	22-FEB-79
CHK'D.	
ENG.	
PROJ. ENG.	
PROD.	

SCALE 2/1
SHT. 1 OF 3
NEXT HIGHER ASSY. B-DD-M7952-0

digital

TITLE FROG REAL TIME CLOCK

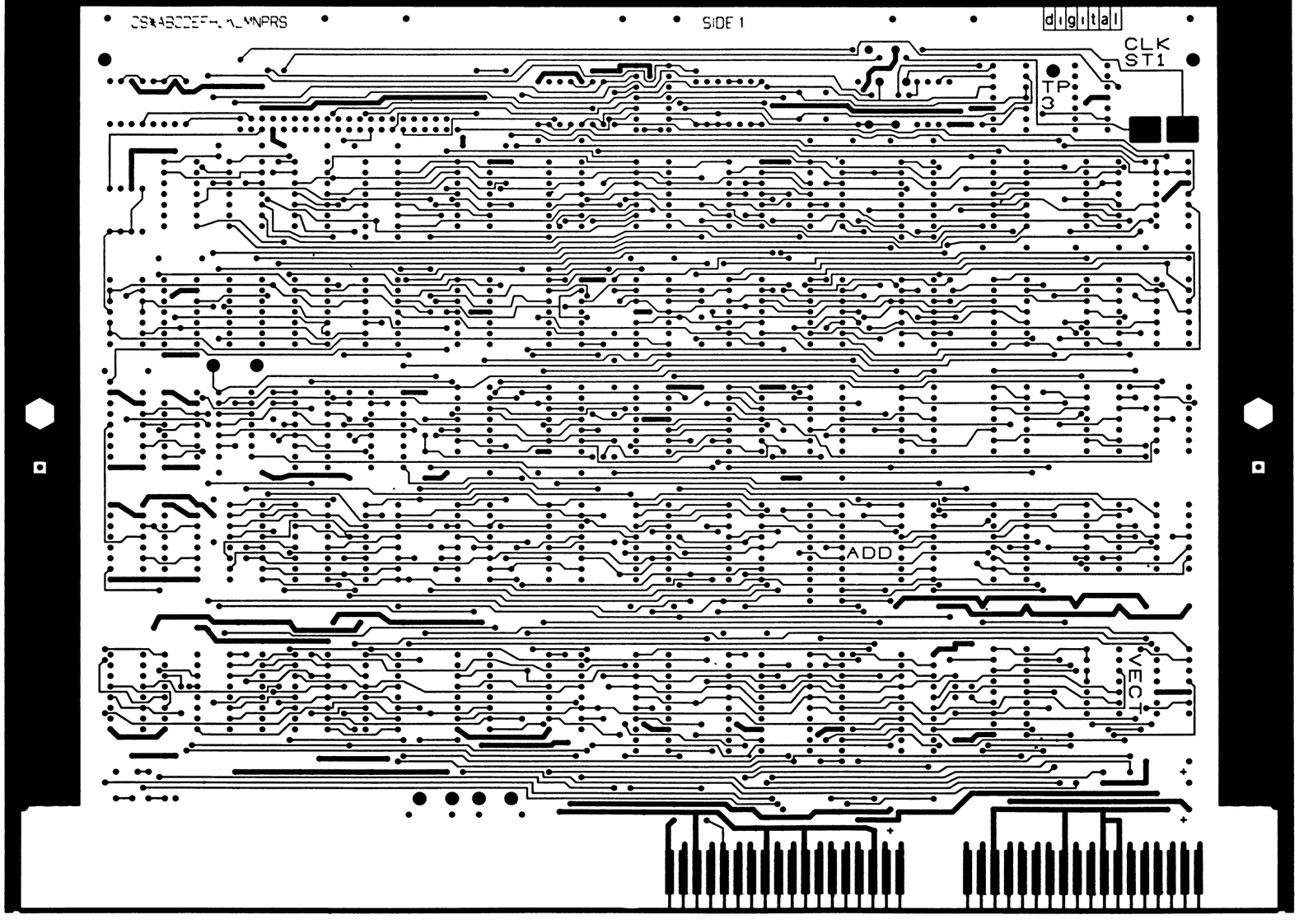
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D	UA	M7952-0-0	D

MS#

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L 1

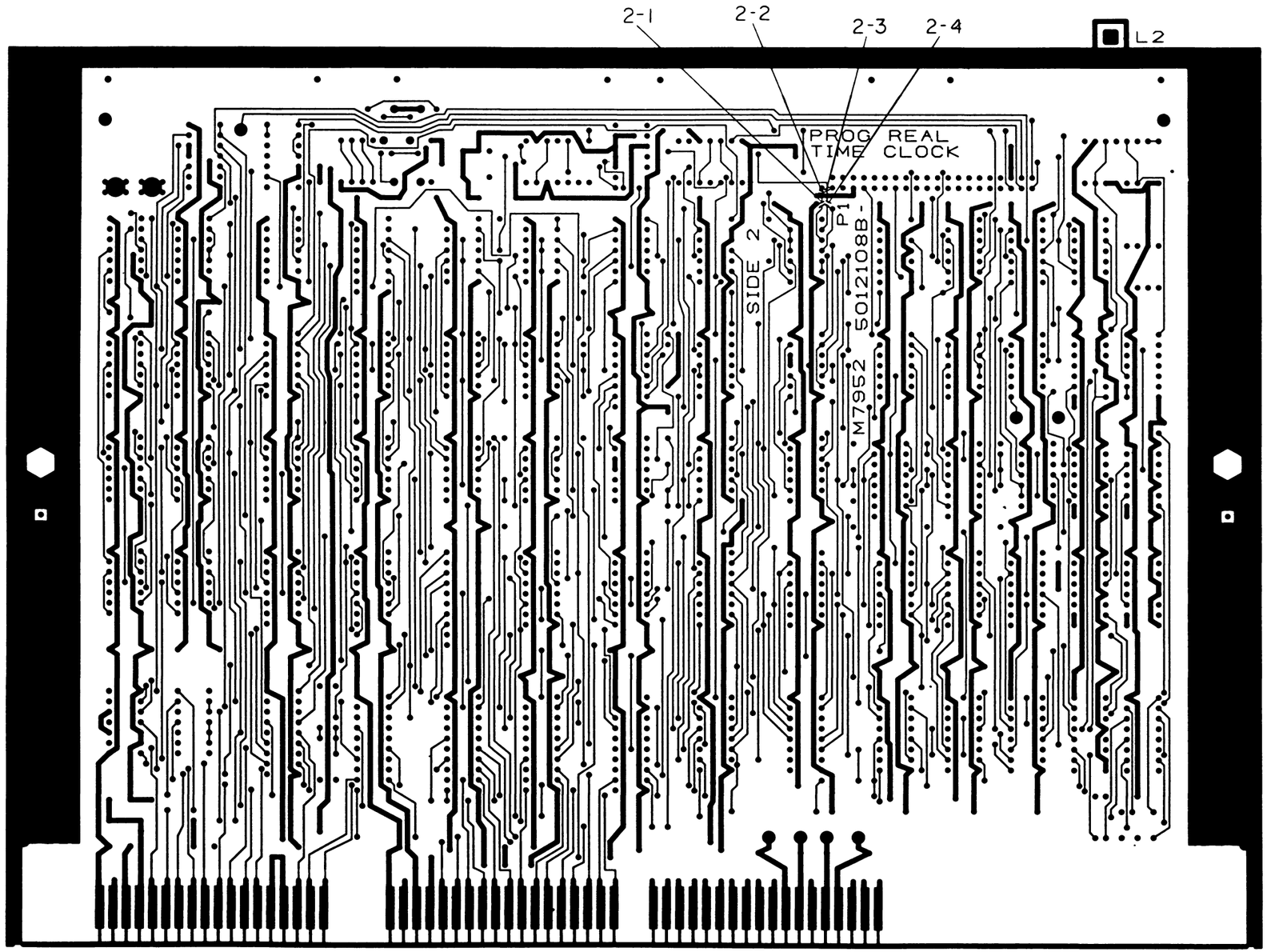
M7952 5012108B-P1



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
PROG REAL TIME CLOCK	D	UA	M7952-0-0	D
SCALE 2/1	SHEET 2 OF 3		DIST	

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
PROG REAL TIME CLOCK	D	UA	M7952-0-0	D
SCALE 2 1	SHEET 3 OF 3	DIST		

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ATC BTØ H
ATC DIN H
ATC BT1 H
ATC DIN L
ATC BT2 H
ATC DOUT H
ATC BT3 H
ATC DOUT L
74S64 E45

FIN INIT L
74S74 E47
74S00 E39
74LS194A E50
ATC OUT H
ATC IN H
ATC BT3 H
ATC BT2 H
ATC BT1 H
ATC BTØ H
8815 E9
ATC REST H
FIN 5 MHZ H

PU PRØ1
RWTBT L AK2
8640 E1
ATC WT BT H
7474 E55
ATC OUT H
ATC IN H
ATC SYNADD H
FIN INIT L
ATC REST H
7408 E29

SSO ADDR COMP H
ATC SYNC H
7474 E55
ATC SYNADD H
FIN 5 MHZ L
7474 E24

ATC BT2 H
ATC SYNC L
7400 E24
FIN INIT L
7408 E29

74175 E20
SSO RDAB Ø H
SSO RDAB 1 H
ATC LDAB Ø H
ATC LDAB Ø L
ATC LDAB 1 H
ATC LDAB 1 L
FIN INIT L
ATC SYNADD H

ATC BT3 H
ATC BT1 H
FIN VECTOR H
7432 E15
8881 E67
13(AF2) ATC BRPLY L

PU PRØ1
7474 E19
ATC PUL BT3 H
FIN 5 MHZ L
7400 E24
ATC BT3 H
7408 E22
FIN INIT L

ATC LDAB 1 L
ATC LDAB Ø L
7410 E23
ATC WR LO CSR1 L
ATC LDAB Ø H
7410 E23
ATC WR HI CSR1 L
ATC PUL BT3 H
ATC LDAB 1 H
7400 E24
ATC WR BPR L

BSYNC L AJ2
8640 E1
ATC SYNC H
7405 E43
R37 1K
+5V
ATC SYNC L

BDOUT L AE2
8640 E1
ATC DOUT H
7405 E43
R36 1K
+5V
ATC DOUT L

BDIN L AH2
8640 E1
ATC DIN H
7404 E8
ATC DIN L

ATC BTØ H
7408 E29
ATC BTØB H

NOTE:
1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
IC 8640	1	8
DC ØØ3	16	8
DC ØØ5	20	10

ATC
ADDR & TIMING CONTROL

REVISIONS	CHK	CHANGE NO.	REV.
		M7952-00001	A
		M7952-MR0002	B
		M7952-MR0003	C
		M7952-MR0004	D

T. ARRIGHI
V. FILZ
M. Powell 20 MAR 80
J. ZEMCIK
A. FILZ

DRN. E Wilson	20 DEC 76
CHK'D M Arrighi	5 APR 76
ENG. Q Amiga	14 MAY 76
PROJ. ENG. Q Amiga	14 MAY 76
PROD. M Arrighi	14 MAY 76
NEXT HIGHER ASSY	B-DD-M7952-Ø
SCALE NONE	
SHEET 1 OF 7	

FIRST USED ON digital
TITLE: PROG REAL TIME CLOCK
SIZE D | CODE CS | NUMBER M7952-Ø-1 | REV. D
DIST

DEC FORM NO. 6NO 1650

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ST SET ST2 L
CSR ST2 GO ENABLE L
7432 E28
SSO RDAB Ø H
ATC WR LO CSR1 L
7404 E8
7474 E39
CSR GO L
CSR GO H
7437 E54
CSR MØ L
BPC SET OVFLO L
7432 E15
FIN INIT L
7408 E29
7474 E36
SSO RDAB 1 H
SSO RDAB 2 H
SSO RDAB 3 H
SSO RDAB 4 H
SSO RDAB 5 H
CSR RATE Ø H
CSR RATE 1 H
CSR RATE 2 H
CSR WR LO CSR1 H
FIN INIT L
ATC IN H
CSR OVFLOFLAB L
7408 E13
SSO RDAB 7 L
ATC WR LO CSR1 H
7410 E7
CSR GO1 + INIT L
7408 E3
PU PRØ2
SSO RDAB 11 H
7474 E19
CSR DISABLE INT OSC H
CSR DISABLE INT OSC L
FIN INIT L
CSR HI BYTE CSR1 H
CSR M3 L
BPC CLK BPR L
CSR GO H
CSR M3BPR L
CSR M3 L
CSR M2 L
CSR M1 L
CSR MØ L
CSR MODE Ø H
CSR MODE 1 H
74175 E48
SSO RDAB 8 H
SSO RDAB 9 H
SSO RDAB 10 H
CSR MAINT ST1 H
CSR MAINT ST2 H
CSR MAINT OSC H
FIN INIT H
ATC REST H
7402 E27
CSR HI BYTE CSR1 H
BPC SET OVFLO L
CSR OVFLO FLAG L
7414 E38
CSR OVFLO FLAG H
ATC BTØB H
CSR OVFLOFLAB H
CSR OVFLOFLAB L
CSR ST2 GO ENABLE L
CSR GO 1 TR H
FIN INIT L
ST SET ST2 L
CSR GO L
CSR PS ST2 L
CSR ST2 FLAG L
ATC IN H
CSR ST2FLAB L
7410 E13
CSR HI BYTE CSR1 H
SSO RDAB 15 L
7410 E7
GO 1 TR L
FIN INIT L
PU PRØ9
7410 E23
+5V
R1Ø 33K
9602 E33
CSR GO 1 TR H
CSR GO 1 TR L
ATC WR HI CSR1 L
SSO RDAB 13 H
CSR ST2 GO ENABLE H
CSR ST2 GO ENABLE L
ATC WR LO CSR1 L
ATC WTBT H
CSR HI BYTE CSR1 H
CSR GO1 TR L
CSR GO1 + INIT L
FIN INIT L
CSR ST2FLAB H
CSR ST2FLAB L
ATC BTØB H
CSR ST2 FLAG H
FIN SET ISA L
CSR ISA H
CSR FOR H
CSR FOR L
ATC IN H
CSR FOR L
CSR HI BYTE CSR1 H
SSO RDAB 12 L
CSR GO1 + INIT L

REVISIONS		
CHK	CHANGE NO.	REV.

CSR

CSR1

TITLE PRCG REAL TIME CLOCK

SIZE D | CODE CS | NUMBER M7952-Ø-1 | REV. D

SCALE | SHEET 2 OF 7 | DIST.

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J1 VV — PU ST1 IN — R20 100K — D1 DGG4 — D2 DGG4 — R8 2K — +5V — +3V — R14 20K 1% — R16 20K 1% — R22 1M — PU PR03 — +12V — LM339 E35 — ST LEVEL 1 — C28 .0047

ST SLOPE 1 — 7486 E63 — ST ST1 H

ST ST1P H — 7432 E49 — ST SET ST1 H

CSR MAINT ST1 H

ST SET ST1 H — 8881 E67 — R26 47Ø — D5 IN4004 — D6 IN4004 — R4 47 FUSIBLE — TP1 — ST ST1 OUT L — J1 UU

LM339 E35

AH1 BC1

+12V AD2, BD2 — C27 .047 — C31 6.8uf

+12 — J1 U — D9 MCL1304 — D10 DGG4 — D11 DGG4 — D12 DGG4 — D13 DGG4 — +3V — TTL REF

J1 TT — PU ST2 IN — R21 100K — +5V — +3V — D3 DGG4 — R15 2ØK 1% — R28 2K — D4 DGG4 — R17 2ØK 1% — R23 1M — PU PR04 — LM339 E35 — ST SLOPE 2 — 7486 E63 — ST ST2 H

J1 P1 — ST POT 1 — J1 P2 — ST POT 2 — S2 — J1 T — ST LEVEL 1 — J1 R — ST LEVEL 2 — +3V — R18 5ØK — R19 5ØK — ST SLOPE 1 — ST SLOPE 2 — C29 .0047

+5V — C37 22ØPF — R33 5.6K — C36 22ØPF — R34 5.6K — 9602 E53 — ST ST1P H — ST ST2 H — 9602 E53 — ST ST2P H — FIN INIT L

ST ST2P H — 7432 E49 — ST SET ST2 H'

CSR MAINT ST2 H — 7450 E58 — ST SET ST2 L

ST SET ST2 H — 8881 E67 — R27 47Ø — D7 IN4004 — D8 IN4004 — R5 47 FUSIBLE — TP3 — ST ST2 OUT L — J1 SS

ST

SCHMITT TRIGGERS

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PROG REAL TIME CLOCK	D	CS	M7952-Ø-1	D
SCALE	SHEET 3 OF 7		DIST.	

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74298 E41
SSO RDAB Ø H — BPC CTR Ø H — BPC BPR Ø H
SSO RDAB 1 H — BPC CTR 1 H — BPC BPR 1 H
SSO RDAB 2 H — BPC CTR 2 H — BPC BPR 2 H
SSO RDAB 3 H — BPC CTR 3 H — BPC BPR 3 H
WS CLK

BPC CLK BPR L

74298 E51
SSO RDAB 4 H — BPC CTR 4 H — BPC BPR 4 H
SSO RDAB 5 H — BPC CTR 5 H — BPC BPR 5 H
SSO RDAB 6 H — BPC CTR 6 H — BPC BPR 6 H
SSO RDAB 7 H — BPC CTR 7 H — BPC BPR 7 H
WS CLK

74298 E52
SSO RDAB 8 H — BPC CTR 8 H — BPC BPR 8 H
SSO RDAB 9 H — BPC CTR 9 H — BPC BPR 9 H
SSO RDAB 1Ø H — BPC CTR 1Ø H — BPC BPR 1Ø H
SSO RDAB 11 H — BPC CTR 11 H — BPC BPR 11 H
WS CLK

74298 E26
SSO RDAB 12 H — BPC CTR 12 H — BPC BPR 12 H
SSO RDAB 13 H — BPC CTR 13 H — BPC BPR 13 H
SSO RDAB 14 H — BPC CTR 14 H — BPC BPR 14 H
SSO RDAB 15 H — BPC CTR 15 H — BPC BPR 15 H
WS CLK

BPC M2 +M3 H, FIN INIT H — 7402 E27 — 7474 E32
ATC BT2 H — 7404 E8

CSR M1 L — 7404 E6 — BPC SET OVRFLO H — 7400 E2 — 7408 E3
CSR MØ L, CSR M1 L — 7400 E2
FIN SEL CLK H — 7403 E43 — R39 2.7K — C39 220pf — 7414 E38 — 7414 E38

+5V — C34 22ØpF — R40 5.6K
FIN SEL CLK L — 9602 E69
BPC CLK BPR L — +5V — C33 33ØpF — R41 5.6K — 7408 E22 — BPC CLBP H
R42 1K — CSR ST2 FLAG H — 9602 E64
FIN INIT L

+5V — C3Ø 22Ø pF — R11 5.6K — 8881 E67 — R24 47Ø — D14 IN4ØØ4 — TP2 FASTON — BPC CLK ØV L
D15 IN4ØØ4 — R25 47 FUSIBLE
BPC OVRFLO H, PU PRØ5 — 9602 E33 — BPC SET OVFLO H, BPC SET OVFLO L
-N INIT L
J1 RR

FIN INIT H, CSR GO L — 7402 E27 — 7408 E22 — R43 56Ω — C40 68Ø pF — 7414 E38
CSR M2 L, CSR M3 L — 7400 E2 — BPC M2+M3 H
BPC CLBP H — 7450 E39 — 7450 E39
ATC WR BPR L — 7432 E49
FIN INIT L — 7405 E43 — C38 22Ø pF
+5V — R38 2.7K — 7402 E27 — BPC CLK BPR L

74193 E42 — BPC BPR Ø H, 1 H, 2 H, 3 H — BPC CTR Ø H, 1 H, 2 H, 3 H — PRØ5
74193 E56 — BPC BPR 4 H, 5 H, 6 H, 7 H — BPC CTR 4 H, 5 H, 6 H, 7 H
74193 E57 — BPC BPR 8 H, 9 H, 1Ø H, 11 H — BPC CTR 8 H, 9 H, 1Ø H, 11 H
74193 E31 — BPC BPR 12 H, 13 H, 14 H, 15 H — BPC CTR 12 H, 13 H, 14 H, 15 H
CRY BRW, CLR LD CUP CDN

REVISIONS

CHK	CHANGE NO.	REV.

BPC BPR & CTR

TITLE	SIZE	CODE	NUMBER	REV.
PROG REAL TIME CLOCK	D	CS	M7952-Ø-1	D
SCALE	SHEET 4 OF 7	DIST.		

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* W3 TO BE INSERTED AFTER GR TEST

BDMG I L AR2.
BDMG O L AS2.

FIN 1 MHZ H
CSR GO H
FIN RC1 L
FIN RC2 L
FIN RC3 L
FIN 10 MHZ H
CR1
CSR DISABLE INT OSC L
CSR MAINT OSC H
+5V
FIN 100 KHZ H
FIN 10 KHZ H
FIN 1 KHZ H
FIN 100 HZ H
BIAKI L
BIAKO L
FIN BIRQ L
FIN INTOV H
FIN VECTOR H
FIN VEC 2 H
FIN INT2 H
FIN INIT H
FIN INIT L
FIN 5 MHZ H
FIN 5 MHZ L
INIT L
CSR OVFLO FLAG H
BPC SET OVFLO L
CSR ST2 FLAG H
CSR PS ST2 L
FIN SEL ISA L
FIN SEL CLK H
FIN SEL CLK L
BEVNT L
ST SET ST1 H
CSR RATE 2² H
CSR RATE 2¹ H
CSR RATE 2⁰ H
CM2
CN2
CR2
CS2
W1
W2
TP6
TP7
TP8
TP9

REVISIONS		
CHK	CHANGE NO	REV

FIN
FREQ. DIVIDER & INTERRUPT CONTROL

TITLE	SIZE	CODE	NUMBER	REV.
PROG REAL TIME CLOCK	D	CS	M7952-0-1	D
SCALE	SHEET 5 OF 7	DIST.		

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SSO RDAB 15 H → 74Ø4 E6 → SSO RDAB 15 L

SSO RDAB 12 H → 74Ø4 E6 → SSO RDAB 12 L

SSO RDAB 7 H → 74Ø4 E6 → SSO RDAB 7 L

S1

1	2Ø	A11
2	19	AIØ
3	18	A9
4	17	A8
5	16	A7
6	15	A6
7	14	A5
8	13	A4
9	12	A3
1Ø	11	A2

S3

VECTOR H 1	14	V8
2	13	V7
3	12	V6
4	11	V5
5	1Ø	V4
6	9	V3
7	8	

DCØØ5 E3Ø

BDAL 15 L	BV2 8	BUS 3	DAT 3 6 → SSO RDAB 15 H
BDAL 12 L	BS2 9	BUS 2	DAT 2 7 → SSO RDAB 12 H
BDAL 11 L	BR2 11	BUS 1	DAT 1 17 → SSO RDAB 11 H
BDAL 14 L	BU2 18	BUS Ø	DAT Ø 18 → SSO RDAB 14 H
+5V	19	JA3	
	2	JA2	
A11	1	JA1	MATCH 3 → SSO ADDR COMP H
	13	MENB	
	16	JAV3	
	15	JAV2	
	14	JAV1	
		XMIT 5	REC 4

PU PRØB

SSO BTI L

DCØØ5 E25

BDAL 1Ø L	BP2 8	BUS 3	DAT 3 6 → SSO RDAB 1Ø H
BDAL 9 L	BN2 9	BUS 2	DAT 2 7 → SSO RDAB 9 H
BDAL 8 L	BM2 11	BUS 1	DAT 1 17 → SSO RDAB 8 H
BDAL 13 L	BT2 12	BUS Ø	DAT Ø 18 → SSO RDAB 13 H
A1Ø	19	JA3	
A9	2	JA2	
A8	1	JA1	MATCH 3
	13	MENB	
	16	JAV3	
	15	JAV2	
V8	14	JAV1	
		XMIT 5	REC 4

DCØØ5 E21

BDAL 7 L	BL2 8	BUS 3	DAT 3 6 → SSO RDAB 7 H
BDAL 6 L	BK2 9	BUS 2	DAT 2 7 → SSO RDAB 6 H
BDAL 5 L	BJ2 11	BUS 1	DAT 1 17 → SSO RDAB 5 H
BDAL 1 L	AV2 12	BUS Ø	DAT Ø 18 → SSO RDAB 1 H
A7	19	JA3	
A6	2	JA2	
A5	1	JA1	3
	13	MENB	
V7	16	JAV3	
V6	15	JAV2	
V5	14	JAV1	
		XMIT 5	REC 4

DCØØ5 E16

BDAL 4 L	BH2 8	BUS 3	DAT 3 6 → SSO RDAB 4 H
BDAL 3 L	BF2 9	BUS 2	DAT 2 7 → SSO RDAB 3 H
BDAL 2 L	BE2 11	BUS 1	DAT 1 17 → SSO RDAB 2 H
BDAL Ø L	AU2 12	BUS Ø	DAT Ø 18 → SSO RDAB Ø H
A4	19	JA3	
A3	2	JA2	
A2	1	JA1	3
BBST L	AP2 13	MENB	
V4	16	JAV3	
V3	15	JAV2	
FIN VEC2 H	14	JAV1	
		XMIT 5	REC 4

74LS257 E37

CSR GO H	2	A1	Y1 4 → SSO RDAB Ø H
BPC BPR Ø H	3	B1	
CSR MODE Ø H	5	A2	Y2 7 → SSO RDAB 1 H
BPC BPR 1 H	6	B2	
CSR MODE 1 H	11	A3	Y3 9 → SSO RDAB 2 H
BPC BPR 2 H	1Ø	B3	
CSR RATE Ø H	14	A4	Y4 12 → SSO RDAB 3 H
BPC BPR 3 H	13	B4	
		SEL	OC 1 15

ATC BTI H → 74Ø4 E6 → ATC LDAB 1 H → SSO BTI L

74LS257 E46

CSR RATE 1 H	2	A1	Y1 4 → SSO RDAB 4 H
BPC BPR 4 H	3	B1	
CSR RATE 2 H	5	A2	Y2 7 → SSO RDAB 5 H
BPC BPR 5 H	6	B2	
FIN INTOV H	11	A3	Y3 9 → SSO RDAB 6 H
BPC BPR 6 H	1Ø	B3	
CSR OVFLOFLAB H	14	A4	Y4 12 → SSO RDAB 7 H
BPC BPR 7 H	13	B4	
		SEL	OC 1 15

74LS257 E47

CSR MAINT ST1 H	2	A1	Y1 4 → SSO RDAB 8 H
BPC BPR 8 H	3	B1	
CSR MAINT ST2 H	5	A2	Y2 7 → SSO RDAB 9 H
BPC BPR 9 H	6	B2	
CSR MAINT OSC H	11	A3	Y3 9 → SSO RDAB 1Ø H
BPC BPR 1Ø H	1Ø	B3	
CSR DIS INT OSC H	14	A4	Y4 12 → SSO RDAB 11 H
BPC BPR 11 H	13	B4	
		SEL	OC 1 15

74LS257 E17

CSR FOR H	2	A1	Y1 4 → SSO RDAB 12 H
BPC BPR 12 H	3	B1	
CSR ST2 GO ENABLE H	5	A2	Y2 7 → SSO RDAB 13 H
BPC BPR 13 H	6	B2	
FIN INT2 H	11	A3	Y3 9 → SSO RDAB 14 H
BPC BPR 14 H	1Ø	B3	
CSR ST2FLAB H	14	A4	Y4 12 → SSO RDAB 15 H
BPC BPR 15 H	13	B4	
		SEL	OC 1 15

REVISIONS		
CHK	CHANGE NO.	REV.

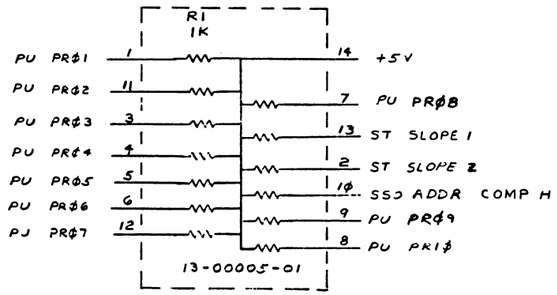
SSO

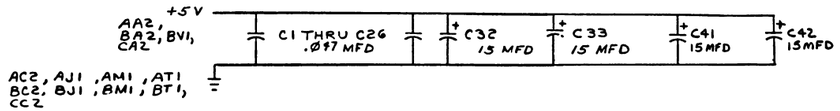
SST & OUT. MUX

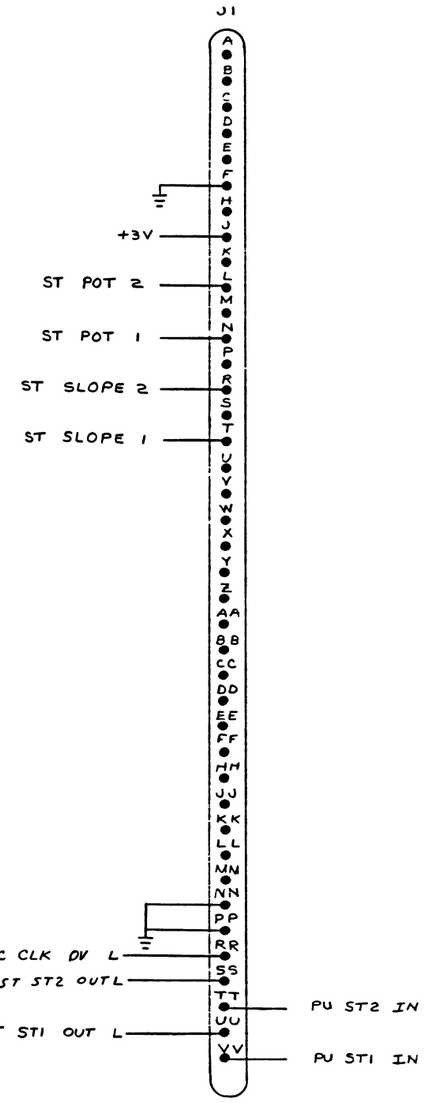
TITLE	SIZE	CODE	NUMBER	REV.
PROG. REAL TIME CLOCK	D	CS	M7952-Ø-1	D
SCALE	SHEET 6 OF 7	DIST.		

DCSM7952-Ø-1 REV D

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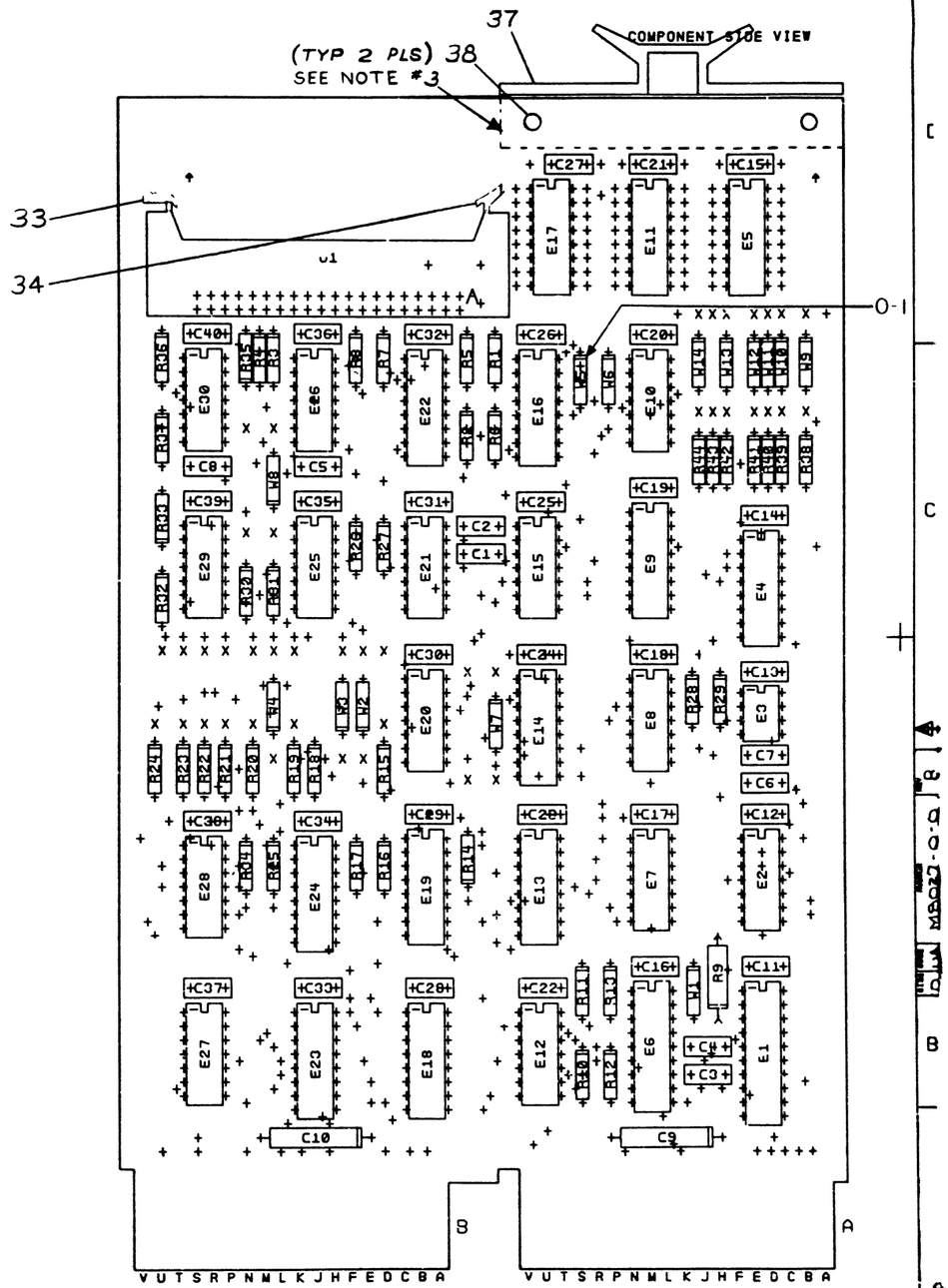




REVISIONS		
CHK	CHANGE NO.	REV.

PULL UPS

TITLE	SIZE	CODE	NUMBER	REV.
PROG REAL TIME CLOCK	D	CS	M7952-Ø-1	D
SCALE	SHEET 7 OF 7	DIST.		



NOTES: 0-1 NOT INSERTED

4. REMOVE THE FOLLOWING UNUSED FINGERS ON ARTWORK: ANI, ANJ, ARI, ASJ, AUI, BDI, BHI, BHJ, BRI, BRJ, CNI, CNJ, CRI, CSJ, CUI, DDI, DHI, DPI, DRJ.

3. ITEM NO 35 UNDERNEATH HANDLE

REV	CHANGE NO	CHK
B	MROZ-ABC02	

ETCH REV. C	
P.C. DESIGN DATA BASE REV. C	

SIGNATURES	DATE
DRN. J FITZGERALD	1/1/77
CHK'D. T Drake	1/1/77
ENG. RW	1/1/77
PROJ.ENG.	1/1/77
PROD.	1/1/77
SCALE 2/1	
SHT. 1 OF 1	

digital

TITLE: PRINTER INTERFACE

SIZE	CODE	NUMBER	REV
D	UA	M8027 0-0	B

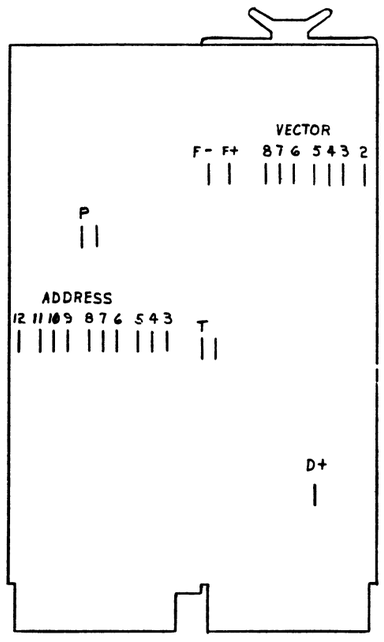
NEXT HIGHER ASSY. 8 DD-M8027 0

M8027-0-0 B

1 MS# 119004

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CROSS REFERENCE DRAWING
(SEE NOTE 3)



JUMPER TABLE		
FUNCTION	DESIGNATION	
ADDRESS SELECTION	A12 - A3	DESIGNATIONS CORRESPOND TO THE BIT POSITION IN THE ADDRESS. HARD WIRE JUMPERS W2, W3 AND W4 BRIDGE A4, A5 AND A7 RESPECTIVELY, AND SPECIFY THE STANDARD ADDRESS OF: 177514 CS 177516 DB JUMPER IN = Ø JUMPER OUT = 1
VECTOR SELECTION	V8 - V2	DESIGNATIONS CORRESPOND TO THE BIT POSITION IN THE VECTOR ALL VECTOR JUMPERS W9 - W14 ARE INSERTED WITH THE EXCEPTION OF V7, TO SPECIFY THE STANDARD VECTOR OF 200. JUMPER IN = Ø JUMPER OUT = 1
CHARACTER TRANSLATION	W7 T	WHEN W7 IS INSERTED DATA FLOWS THROUGH LPV11 WITHOUT TRANSLATION. [STANDARD CONFIGURATION] WHEN T IS INSERTED DATA IS MODIFIED BY THE LPV11: LOWER CASE CHARACTERS ARE TRANSLATED TO UPPER CASE INSERT W7 OR T, DO NOT INSERT BOTH SIMULTANEOUSLY.
PARITY	W8 P	WHEN W8 IS INSERTED, P DATA 8 (LP05 PAPER INSTRUCTION / LA180 PARITY) WILL BE TRANSMITTED DIRECTLY [STANDAND CONFIGURATON] WHEN P IS INSERTED, P DATA 8 WILL BE HELD HIGH IF BOTH W8 AND P ARE REMOVED P DATA 8 WILL BE HELD LOW (USED WITH LP05 IF DAVFU IS PRESENT.) BOTH W8 AND P MUST NEVER BE INSERTED SIMULTANEOUSLY.
FAULT FILTER	F+ F-	WHEN F+ (W6) IS INSERTED, NOISE IS FILTERED ON LP05 FAULT LINE. [STANDARD CONFIGURATION] WHEN F- (W5) IS INSERTED, NOISE IS NOT FILTERED ON LP05 FAULT LINE. INSERT F+ OR F-, DO NOT INSERT BOTH SIMULTANEOUSLY.
DELAY	D	THIS JUMPER (W1) MUST BE INSERTED [STANDARD CONFIGURATION]. REMOVAL CAUSES BRPLY DELAY TO CHANGE, RESERVED FOR FUTURE USE

NOTE: 1. ALL DESIGNATIONS WHICH HAVE A W PREFIX ARE NOT LABELLED IN ETCH, ALL OTHERS ARE LABELLED IN ETCH (ADDRESS DESIGNATIONS SHOW ALTERNATELY, DUE TO A LACK OF SPACE).

NOTES:
1. TERMINATING RESISTORS MUST BE PRESENT ON THE CONNECTOR BOARD WITHIN THE LP05.
2. IN THE EVENT THAT THE LP05 IS EQUIPPED WITH DAVFU, IT IS RECOMMENDED THAT THE PAPER INSTRUCTION (DATA 8) JUMPER W8 BE REMOVED, SINCE THE LPV11 DOES NOT SUPPORT THIS OPTION.
3. SEE UA DRAWING M8027-0-0 FOR W DESIGNATIONS OF JUMPERS.

DRN. Silvia	7-28-77	FIRST USED ON
CHK'D		
ENG.		
PROJ. ENG.		
PROG.		
NEXT ASSY		
SCALE		
SHEET 1 OF 5		

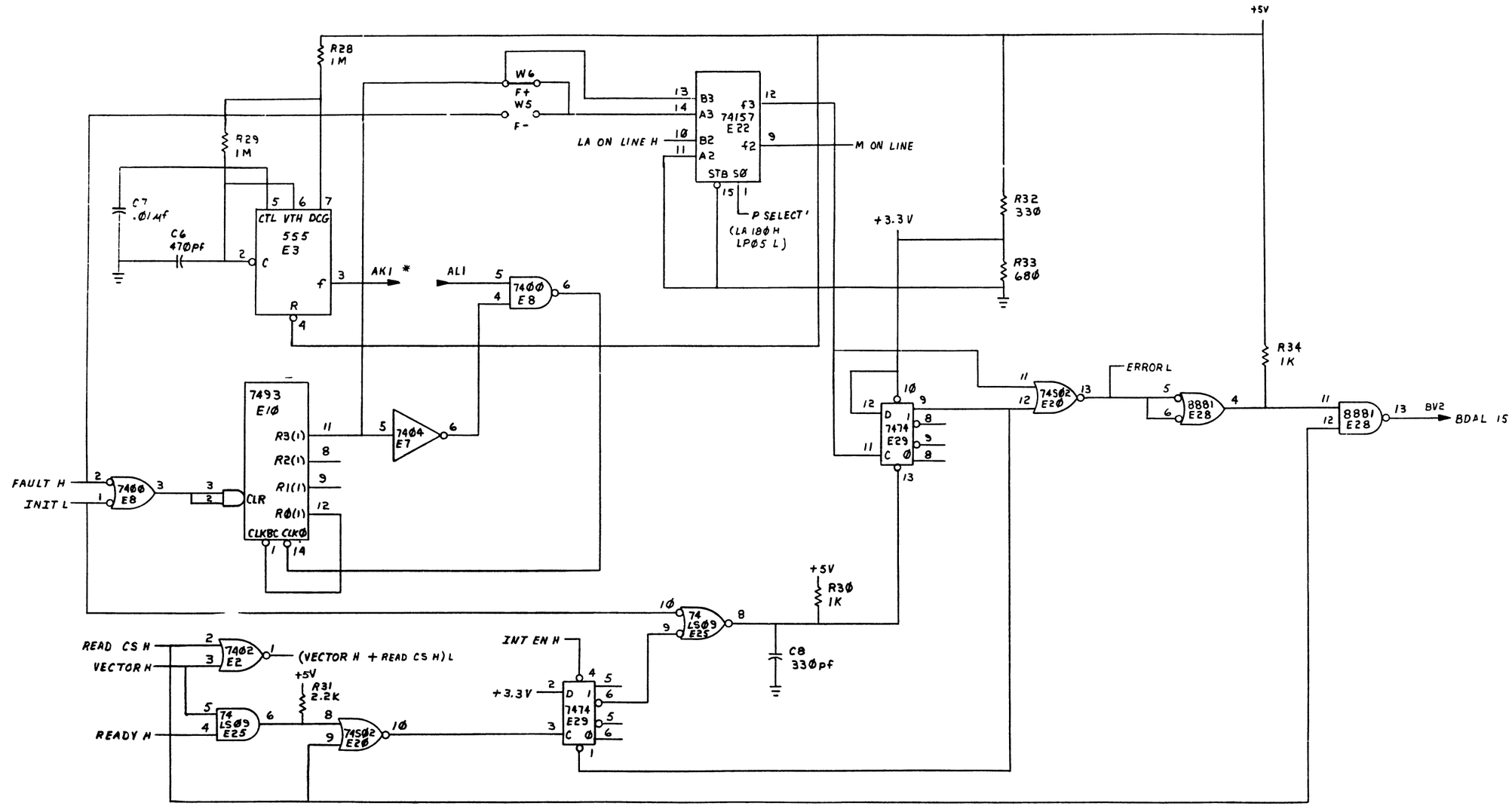
TITLE: LPV11 PRINTER INTERFACE

SIZE	CODE	NUMBER	REV.
D	CS	M8027-0-1	B

DIST.

REV.	CHANGE NO.	
B	M8027-AB002	Antonsen 2 Oct 78 J. CURTIS

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NOTE : * PINS AK1 & AL1 ARE JUMPERED THROUGH THE BACKPLANE.

DRN. Silvia	6-17-77	FIRST USED ON	digital
CHK'D RP	28 JUN 77		
ENG. RP	28 JUN 77	TITLE	LPV-11 PRINTER INTERFACE
PROJ. ENG. RP	28 JUN 77		
PROD.			
NEXT HIGHER ASSY.			
SCALE —/—		SIZE D / CODE CS / NUMBER M8027-0-1 / REV. B	
SHEET 2 OF 5		DIST.	

REVISIONS | REV. | CHANGE NO. | CHK

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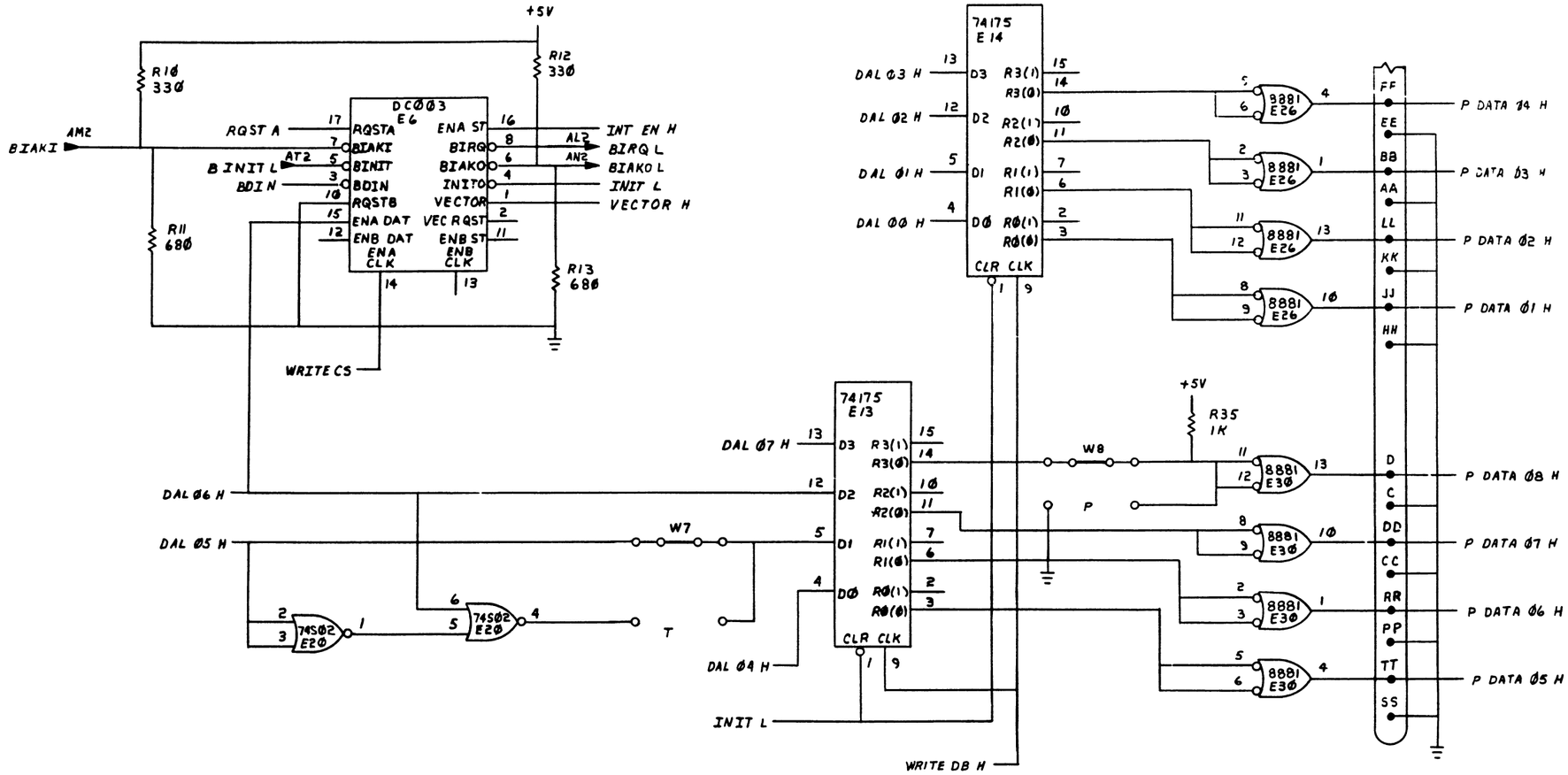
J1
P DEMAND H
P BUSY L
P ON LINE H
P FAULT L
P CONN L
P SELECT (LA 18Ø L) (LP ØS H)
R1 33Ø
R2 33Ø
R3 15Ø
R4 15Ø
R5 15Ø
R6 15Ø
R7 1K
R8 1K
C1 .Ø1mf
C2 .Ø1mf
M CONN L
8641 E16
BUSY H
LA ON LINE H
FAULT H
+5V
R9 4.Ø2K
R27 2.2K
R26 1K
C5 15Øpf
INIT L
READY H
ERROR L
WRITE DB L
LP STROBE L
READY·ERR
RQST A
WRITE DB H
M CONN L
R36 15Ø
R37 33Ø
P STROBE
ENB H
BSYNC
DAL Ø2 H
DAL Ø1 H
DAL ØØ H
BWTBT
BDOUT
BD IN L
VECTOR H
BDIN
W1
C3 18Øpf
C4 15Øpf
BRPLY
WRITE CS
READ CS H
P SELECT' (LA 18Ø H LPØSL)

7493	1Ø	5
555	1	8
8641	8	16
8640	1	8
8136	8	16
74175	8	16
74157	8	16
DC003	9	18
DC004	1Ø	2Ø
IC TYPE	GND	+5

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: LPV-11 PRINTER INTERFACE
SIZE: D | CODE: CS | NUMBER: M8Ø27-Ø-1 | REV: B
SCALE: — | SHEET 3 OF 5 | DIST.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LPV-11 PRINTER INTERFACE	D	CS	M8027-0-1	B
SCALE —H—	SHEET 4 OF 5	DIST.		

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+5V
R39 1K
R38 1K
R43 1K
R42 1K
R41 1K
R40 1K
R44 1K

V10 V3
V9 V2
V7
READY·ERR
W13 V6
INT EN H
W12 V5
W11 V4
W14 V8

74157 E4
74157 E9
M ON LINE
BUSY H
STB S0

(VECTOR H + READ CS H) L
VECTOR H
8881 E28
BM2
BDAL Ø8 L

8641 E18
8641 E23

AU2 BDAL ØØ L DAL ØØ H
AV2 BDAL Ø1 L DAL Ø1 H
BE2 BDAL Ø2 L DAL Ø2 H
BF2 BDAL Ø3 L DAL Ø3 H
BH2 BDAL Ø4 L DAL Ø4
BJ2 BDAL Ø5 L DAL Ø5 H
BK2 BDAL Ø6 L DAL Ø6 H
BL2 BDAL Ø7 L DAL Ø7 H

R19 R18 R17 R16 R15 R14 1K
A7 W4 A6 A5 W3 A4 W2 A3

R25 R24 R23 R22 R21 R20 1K
A12 A11 A10 A9 A8

3136 E13
8136 E24
B1 D1 B2 D2 B3 D3 B4 D4 B5 D5 B6 D6 STB
OUT
ENE H

BDAL Ø8 BM2 8640 E12
BDAL Ø9 BN2 8640 E27
BDAL 10 BP2 8640 E27
BDAL 11 BR2 8640 E27
BDAL 12 BS2 8640 E27
BBS 7 AP2 8640 E12

BDMGI L AR2 AS2 BDMGO L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LPV-11 PRINTER INTERFACE	D	CS	M8027-0-1	B
SCALE	SHEET 5 OF 5	DIST.		

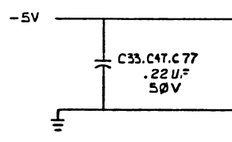
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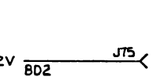
NOTES:

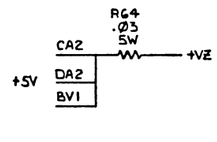
1. 8640. E11 PIN 8 IS +5 *
2. 8837. E1 PIN 16 IS +5 *

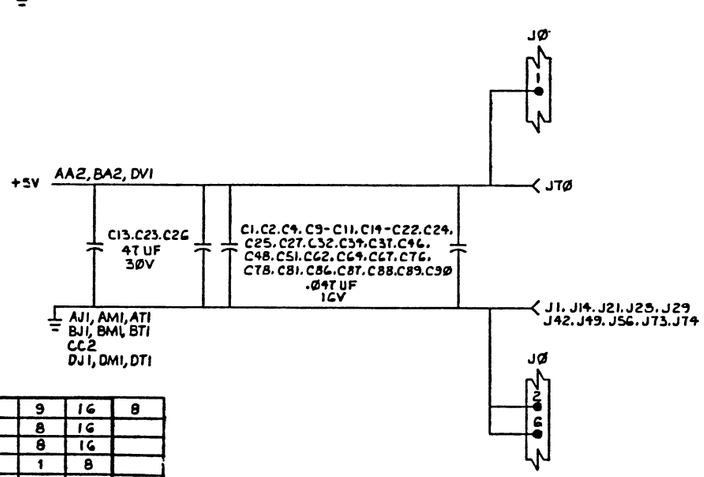
S3	S2	S1	DESIRED BANK
ON	ON	ON	0-4K
ON	ON	OFF	4-8K
ON	OFF	ON	8-12K
ON	OFF	OFF	12-16K
OFF	ON	ON	16-20K
OFF	ON	OFF	20-24K
OFF	OFF	ON	24-28K
OFF	OFF	OFF	28-32K

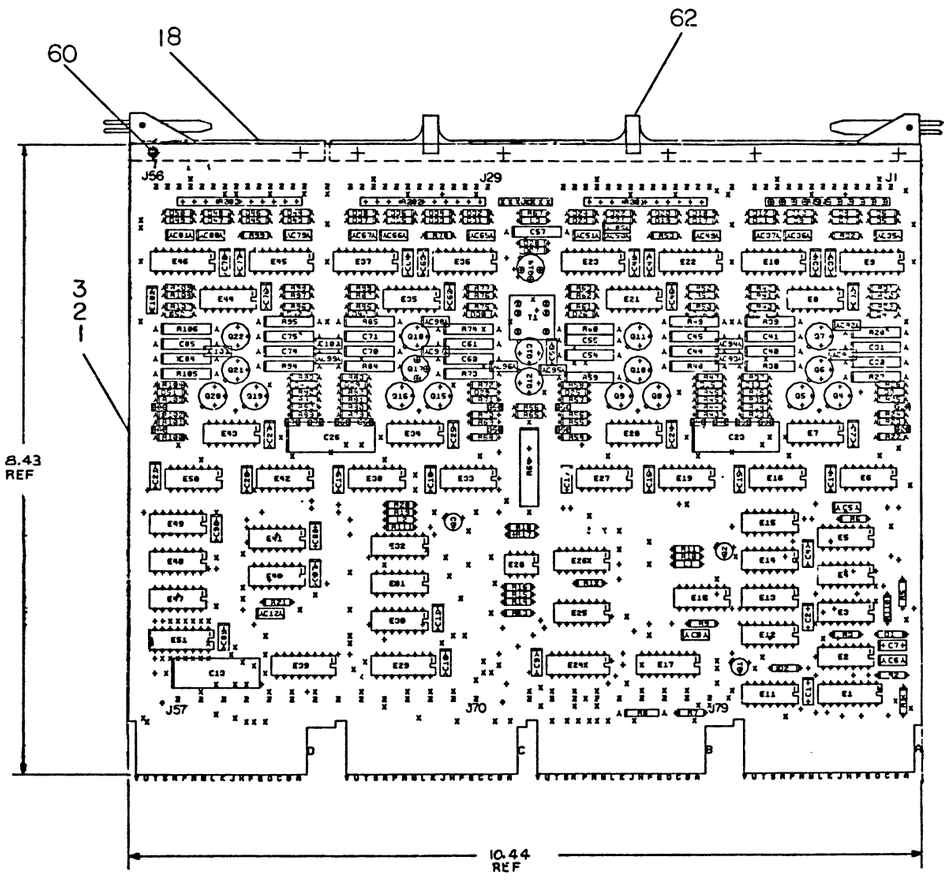
E-28 SWITCH POSITIONS FOR BANK SELECT.











7528	9	16	8
8837	8	16	
8838	8	16	
8640	1	8	
IC TYPE	GND	+5V	-5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV.	CHG.	CHANGE NO.	REVISIONS
C	CHK	G653-00001	P. DURANT 8-21-75
D		G653-00002	P. DURANT 9-22-75
E		G653-00003	P. DURANT 12-8-75
F		G653-00004	P. DURANT 1-6-76

FIRST USED ON OPTION MODEL

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV. C

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.	M. POIRIER	DATE 5-12-75
CHK'D.	Robert Kjenner	DATE 7-1-75
ENG.	C. DUBE	DATE 7-7-75
PROJ. ENG.	W. H. Bell	DATE 7-7-75
PROJ.	C. Lane	DATE 7-7-75
NEXT HIGHER ASSY		
SCALE		
SHEET 1 OF 8		

digital

TITLE MMVII-A
4KX16 BIT MEMORY

SIZE D | CODE CS | NUMBER G653-0-1 | REV. F

DIST.

SIZE D | CODE CS | NUMBER G653-0-1 | REV. F

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PARTS LIST

QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
REF		ASSY/DRILL HOLE LAYOUT	D-AH-G653-0-5	1
REF		MODULE ECO HISTORY	B-MH-G653-0-6	2
1		ETCHED CIRCUIT BOARD	5011632	3
2	C8,12	CAP 82 PF 100V	1000015	4
1	C6	CAP 1000 PF 100V	1000042	5
8	C35,36,49,50,65,66,79,80	CAP 120 PF 100V	1000018	6
2	C5,C7	CAP 820 PF 100V	1000027	7
35	C1,2,4,9,10,11,14-22,24, 25,27,32,34,37,46,76,81, 48,51,62,66,64,67,76,85, 90,87,88	CAP .047 UF 16V	1009678	8
17	C30,31,40,41,44,54,45,55, 60,61,70,71,74,75,84,85, 57	CAP S. TANT 6.8 UF 35V	1005306	9
16	C28,29,36,39,42,43,52,53, 58,59,68,69,72,73,82,83	CAP 3300 PF 50V	1011740-01	10
3	C13,23,26	CAP 47 UF 30V	1012219	11
16	C56,91-102,33,47, ,77	CAP,22 UF 50V	1010274	12
1	D2	DIODE IN752A	1102808	13
51	D1,D3-D52	DIODE D672	1105275	14
1	E28	SWITCH 4 POLE DIP	1211164-00	15
79	J1-J78	CONTACT, FEMALE	1211728	16
1	J0	CONN, PLUG, 7 PIN	1212104	17
1		HANDLE, L.H.	7413828-00	18
1	R64	RES .03 5W 3%	1310676-01	19
16	R23,25,34,36,44 46,55,57, 69,71,80,82,90,92,101,103	RES 120 5% 1/4W	1300247	20
16	R22,24,33,35,43,45,54,56, 68,70,78,81,89,91,100,102	RES 33 5% 1/4W	1300197	21
18	R26,29,37,40,47,50,58,61, 72 75,83,86,93,104,107,96	RES 5.1 5% 1/4W	1309422	22
20	R30,31,41,42,51,52,62,63, 11,78,77,87,88,97,98,108 109,5,111,12	RES 1K 5% 1/4W	1300385	23
5	R9,10,19,21 110	RES 100 5% 1/4W	1300229	24
4	R1,65,7,66	RES 470 5% 1/4W	1300316	25
1	R3	RES 180 5% 1/4W	1301322	26
1	R8	RES 56 5% 1/2W	1309995	27
7	R13-18,20,	RES 4JK 5% 1/4W	1300447	28
1	R2	RES 10K 5% 1/4W	1300479	29
1	R6	RES 75 5% 1/4W	1302379	30
1	R67	RES 5.6% K 1% 1/8W	1306128	31
4	R32,53,78,89	RES 10.0K 1% 1/8W	1303312	32
4	R200,201,202,203	RES PACK 11 PIN #80	1311741	33
16	R27,28,38,39,48,49 59,60 73,74,84,85,94,95,105,106	RES 2.0 1% 3W WW	1312542	34
2	Q2,Q3	TRANS 3009B	1503100	35
1	Q1	TRANS 6531B	1509358	36
18	Q4-11, 15-22	TRANS 3782	1509649-01	37
2	Q12,13	TRANS 3725	1510958	38
2	L1,L2	INDUCTOR 100 UH	1610682	39
1	L3	INDUCTOR 2.2 UH	1609756	40
1	T1	TRANSFORMER	1612523	41
2	E18,40	DELAY LINE 250 NS	1611243	42

PARTS LIST

QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
1	E41	I.C. 7400	1905575	43
1	E5	I.C. 7451	1905828	44
1	E2	I.C. 8881	1909705	45
1	E26	I.C. 74H53	1909062	46
12	E3,6,12,14,16,19,27,32,33, 38,42,50	I.C. 74H74	1909667	47
4	E7,20 34 43	I.C 7437	1910091	48
1	E25	I.C 8242	1909712	49
6	E8,15,21,35,44,48	I.C 74H04	1909931	50
8	E9,10,22,23,36,37,45,46	I.C. 7528	1910687	51
6	E4,13,30,31,47,49	I.C. 74128	1912068	52
1	E1	I.C. 8837	1911116	53
4	E17,24,28,39	I.C. 8641	1911579	54
1	E11	I.C. 8640	1911469	55
1	Q14	DEC 320-5.0	1912541-00	56
19		TRANSIPADS	9007201	57
4		STANDOFF SPACERS	9008213	58
4		NYLON SCREW 8-32 X .250	9009041-1	59
8		EYELET, HANDLE	9006732	60
1		HEAT SINK 2201 RED	1210001-00	61
1		HANDLE RH	7413826-01	62
REF	E51	SPARE		63
1	CG3	CAP 1UF RADIAL	1010274-02	64

REVISIONS

CHK	CHANGE NO.	REV.

TITLE 4KX16 MMVII-A BIT MEMORY
SIZE D CODE CS NUMBER G653-0-1 REV F
SCALE SHEET 2 OF 8 DIST.

8 7 6 5 4 3 2 1

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BUS SYNC L AJ2
BUS REF L AR1
MTDB RESET L
MTDA RESET H
MTDA D SEL H
MTDA F BUSY H
MTDA F BYTE L
MTDA R DOUT H
MTDA RESET H
MTDA F READ H
MTDA RT 50 H
MTDA RT 100 H
MTDA RT 150 H
MTDA RT 200 H
MTDA RT 175 H
MTDA RT 25 H
READ TIMING DELAY CKT
BUS DIN L AH2
BUS DOUT L AE2
BUS WRITE BYTE L AK2
MTDA R DIN H
MTDA R DOUT H
MTDA T INH H
MTDB RESET L
MTDC RAW Ø H
MTDA F BYTE L
MTDA FAØ H
MTDA FAØ L
MTDA R W BYTE L
MTDA DATA OUT L
MTDA F READ H
MTDA RT 50 H
MTDA RT 100 H
MTDA RT 25 H
J79 MTDA F BUSY L
J62 MTDA READ EARLY L
J60 MTDA READ LATE L
(BITS Ø-7) MTDA CLR Ø L
(BITS 8-15) MTDA CLR 1 L
MTDA INH L
MTDA T INH H
MTDA FAØ H
MTDA R W BYTE L
MTDA MDR CLK ØH
MTDA MDR CLK 1H
MTDA R DOUT H
MTDA WRITE TIME ENABLE H
MTDA R DIN H
MTDA WT 175 H
MTDA WT 225 H
J59 MTDA W LATE'
J57 MTDA STK CHQ H
J61 MTDA W EARLY L
BUS TIMING BUFFERS
MTDB LOCKOUT L
MTDF RAW A 13 H
MTDF RAW A 14 H
MTDF RAW A 15 H
MTDA RT 100 H
MTDA RT 150 H
MTDA W CLR L
MTDA R DIN H
MTDA R DOUT H
MTDA RT 150 H
MTDA RESET H
MTDA W CLR L
MTDA WRITE TIME ENABLE H
MTDA WT 225 H
MTDA WT 175 H
BUS REPLY L AFZ
NOT USED
BANK TO BE USED
BANK SELECT CKT
WRITE TIMING DELAY LINE CKT

	SW1	SW2	SW3	
Ø	1	1	1	Ø - 4K
1	Ø	1	1	4 - 8K
2	1	Ø	1	8 - 12K
3	Ø	Ø	1	12 - 16K
4	1	1	Ø	16 - 20K
5	Ø	1	Ø	20 - 24K
6	1	Ø	Ø	24 - 28K
7	Ø	Ø	Ø	28 - 32K

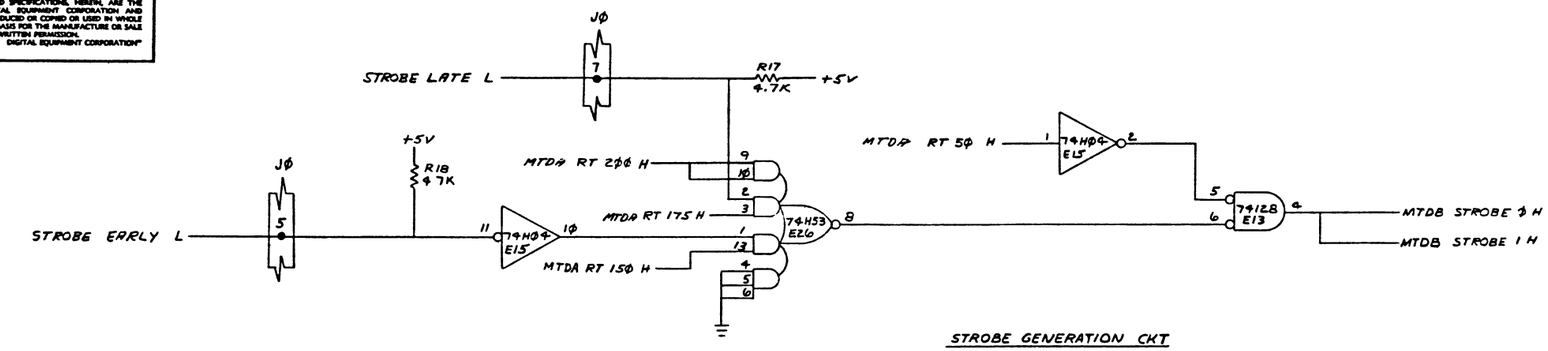
Ø SW OPEN OFF
1 SW CLOSED ON

REVISIONS		
CHK	CHANGE NO	REV

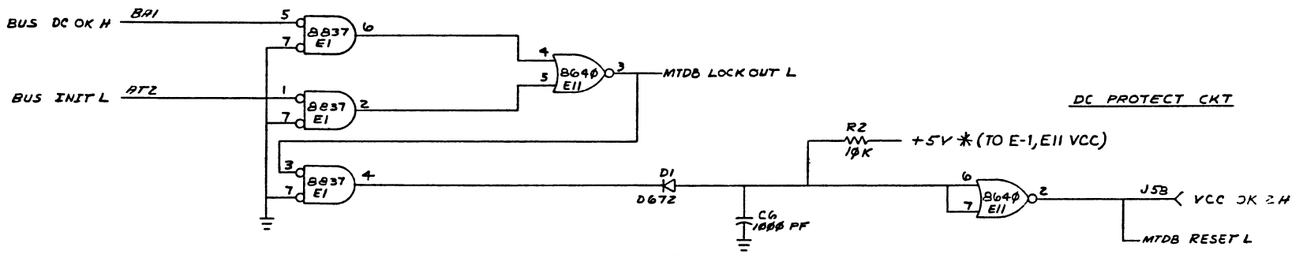
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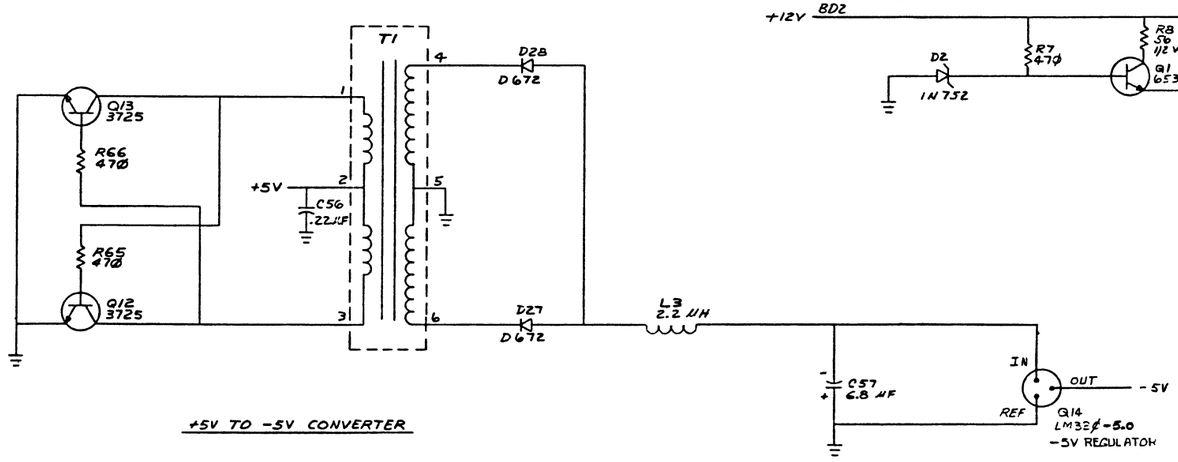
TITLE	SIZE	CODE	NUMBER	REV.
MMVII-A 4KX16 BIT MEMORY (MTDA)	D	CS	G653-Ø-1	F
SCALE — / SHEET 3 OF 8	DIST.			

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STROBE GENERATION CKT





+5V TO -5V CONVERTER

REVISIONS		
CHK	CHANGE NO	REV

(CONTROL TIMING)

TITLE	MMVII-A 4KX16 BIT MEMORY (MTDB)	SIZE	CODE	NUMBER	REV.
SCALE	SHEET 4 OF 8	D	CS	G653-0-1	F
		DIST.			

D CS G653-0-1 F

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MTDC VTH

MTDA INH L — 74H04 E35

BIT ØØ

VTH TEST POINT — J0 — R67 5.62K — +5V — R78 10K 1/8W — C86 .47UF — C67 .047UF — R202

MTDC RAW Ø H — MTDA DATA OUT L — BUS DAL ØL CU2 — 8641 E29 — 74H74 E33 — MTDA MDR CLK Ø H — MTDC CLR Ø L

SB ØØ J31 — SA ØØ J32 — R202 — 7528 E36 — R76 1K — 74H04 E35 — D32 D672 — D31 D672 — C65 120PF — MTDA STROBE Ø H

+5V — C60 6.8 UF — R69 120 — R73 2.0 3W — C58 3300 PF — R68 33 — Q15 3762 — J30 — MTDC INH ØØ — D29 D672 — R72 5.1

7437 E34

BIT Ø1

J69 MTDC STK A1 H — BUS DAL 1L CU2 — 8641 E29 — 74H74 E33 — MTDA MDR CLK Ø H — MTDA CLR Ø L

STKC SB Ø1 J34 — STKC SA Ø1 J35 — R202 — 7528 E36 — R77 1K — 74H04 E35 — D34 D672 — D33 D672 — MTDB STROBE Ø H

+5V — C61 6.8 UF — R71 120 — R74 2.0 3W — C59 3300 PF — R70 33 — Q18 3762 — J33 — MTDC INH Ø1 — D30 D672 — R75 5.1

7437 E34

BIT Ø2

J68 MTDC A2 H — BUS DAL 2L DE2 — 8641 E29 — 74H74 E38 — MTDA MDR CLK Ø H — MTDA CLR Ø L

STKC SB Ø2 J37 — STKC SA Ø2 J38 — R202 — 7528 E37 — R87 1K — 74H04 E35 — D36 D672 — D35 D672 — C66 120PF — MTDB STROBE Ø H

+5V — C71 6.8 UF — R80 120 — R85 2.0 3W — C69 3300 PF — R79 33 — Q17 3762 — J36 — MTDC INH Ø2 — D40 D672 — R86 5.1

7437 E34

BIT Ø3

J67 MTDC A3 H — BUS DAL 3L DF2 — 8641 E29 — 74H74 E38 — MTDA MDR CLK Ø H — MTDA CLR Ø L

STKC SB Ø3 J41 — STKC SA Ø3 J40 — R202 — 7528 E37 — R88 1K — 74H04 E35 — D37 D672 — D38 D672 — MTDB STROBE Ø H

+5V — C70 6.8 UF — R82 120 — R84 2.0 3W — C68 3300 PF — R81 33 — Q16 3762 — J39 — MTDC INH Ø3 — D39 D672 — R83 5.1

7437 E34

(SENSE INHIBIT BITS ØØ-Ø3)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	MXVII-A 4KX1E 3T MEMORY (MTDC)			
SIZE	CODE	NUMBER		REV
D	CS	G653-Ø-1		F
SCALE		SHEET 5 OF 8	DIST	

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BIT Ø4

MTDA INH L — 74H04 E44

J66 MTDD RAW Ø H

MTDC VTH — R99 MK 1ØW — C81 .047MF — R201

MTDA DATA OUT L — 8641 E39 — 74H74 E42 — BUS DAL 4 L DH2

MTDA MDR CLK Ø H

MTDA CLR Ø L

STKC SBØ4 J44

STKC SAØ4 J45

R2Ø3 — 7528 E45 — D44 D672 — D43 D672 — C79 12ØPF

+5V — R97 1K — 74H04 E44

MTDB STROBE Ø H

7437 E43 — C74 6.8MF — R9Ø 12Ø — R94 2.Ø 3W — C73 33ØØ PF — R89 33 — Q19 3762 — J43 MTDD INH Ø 4

D41 D672 — R93 5.1

BIT Ø5

J65 MTDD A5 H

BUS DAL 5 L DJ2

MTDA MDR CLK Ø H

MTDA CLR Ø L

STKC SBØ5 J47

STKC SAØ5 J48

R2Ø3 — 7528 E45 — D46 D672 — D45 D672

MTDB STROBE Ø H

+5V — R98 1K — 74H04 E44

7437 E43 — C75 6.8MF — R92 12Ø — R95 2.Ø 3W — C72 33ØØPF — R91 33 — Q22 3762 — J46 MTDD INH Ø5

D42 D672 — R96 5.1

BIT Ø6

J63 MTDD A6 H

BUS DAL 6L DK2

MTDA MDR CLK Ø H

MTDA CLR Ø L

STKC SBØ6 J51

STKC SAØ6 J52

R2Ø3 — 7528 E46 — D48 D672 — D47 D672 — C86 12ØPF

MTDB STROBE Ø H

+5V — R1Ø8 1K — 74H04 E44

7437 E43 — C85 6.8MF — R1Ø1 12Ø — R1Ø6 2.Ø 3W — C82 33ØØPF — R1Ø6 33 — Q21 3762 — J5Ø MTDD INH Ø6

D52 D672 — R1Ø7 5.1

BIT Ø7

J64 MTDD A7 H

BUS DAL 7L DL2

MTDA MDR CLK Ø H

MTDA CLR Ø L

STKC SBØ7 J55

STKC SAØ7 J54

R2Ø3 — 7528 E46 — D49 D672 — D5Ø D672

MTDB STROBE Ø H

+5V — R1Ø9 1K — 74H04 E44

7437 E43 — C84 6.8MF — R1Ø3 12Ø — R1Ø5 2.Ø 3W — C83 33ØØ PF — R1Ø2 33 — Q2Ø 3762 — J53 MTDD INH Ø7

D51 D672 — R1Ø4 5.1

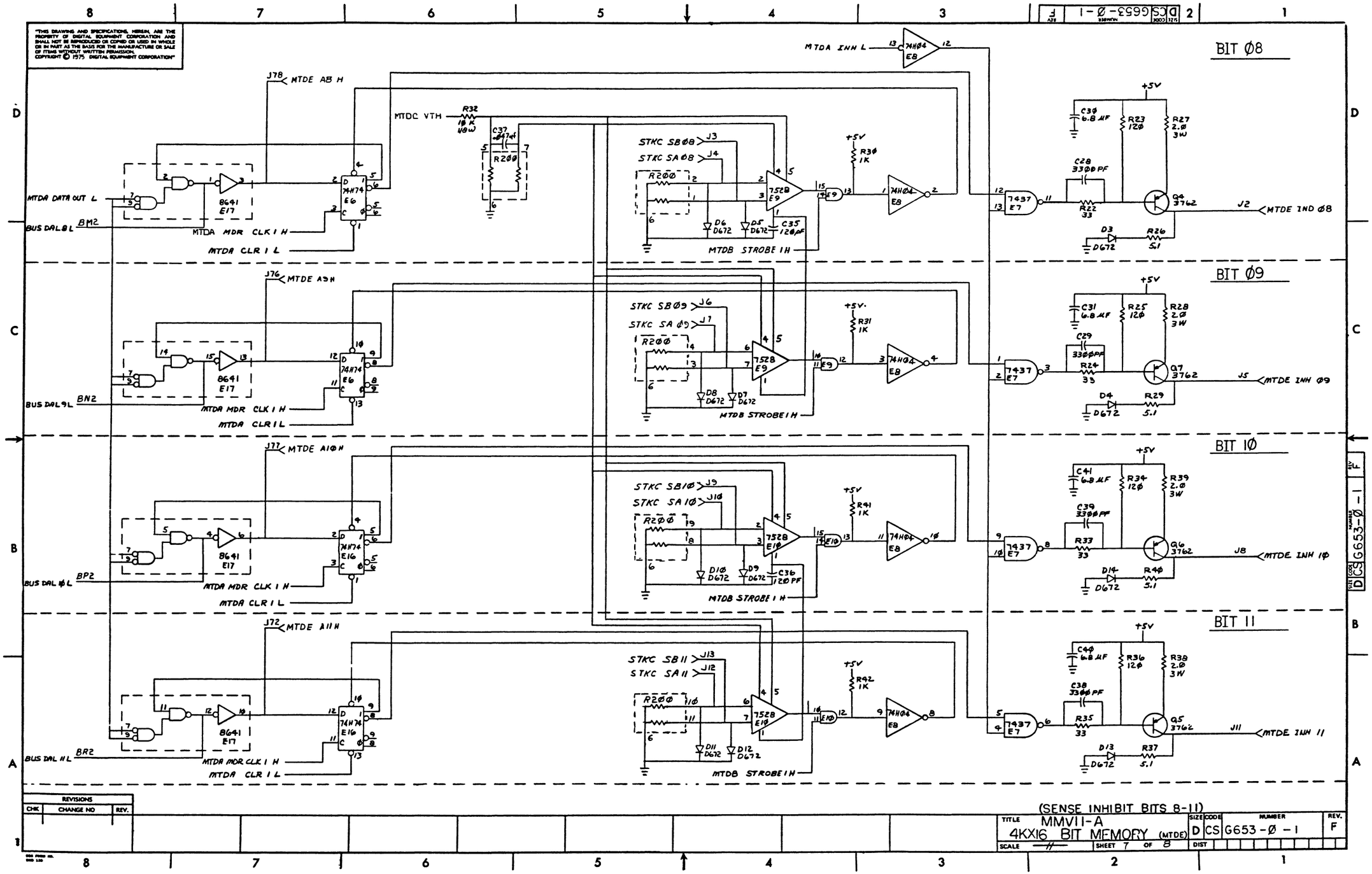
REVISIONS

CHK	CHANGE NO	REV.

(SENSE INHIBIT BITS 4 -7)

TITLE	SIZE	CODE	NUMBER	REV.
MMVII-A 4KX16 BIT MEMORY (MTDD)	D	CS	G653-Ø-1	F
SCALE — //	SHEET 6 OF 8	DIST.		

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REVISIONS		
CHK	CHANGE NO	REV.

(SENSE INHIBIT BITS 8-11)

TITLE	MMV11-A 4KX16 BIT MEMORY (MTDE)	SIZE	CODE	NUMBER	REV.
		D	CS	G653-Ø-1	F
SCALE	SHEET 7 OF 8	DIST			

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MTDA INH L — 74H04 E21

BIT 12

J71 MTDFA12H — MTDC VTH — R53 10K 1/8W — C51 .047UF — R201

MTDA DATAOUT L — BUS DAL12L BS2 — 8641 E24 — 74H74 E19

MTDA MDR CLK I H — MTDA CLR I L

STKC SB12 J16 — STKC SA12 J17 — R201 — 7528 E22 — D18 D672 — D17 D672 — C49 120PF — MTDB STROBE I H

+5V — R51 1K — 74H04 E21

+5V — C44 6.8 MF — R44 120 — R48 2.0 3W — C43 3300 PF — R43 33 — 7437 E20 — Q19 3762 — J15 MTDF INH 12 — D15 D672 — R47 5.1

BIT 13

MTDF RAW A13 H — BUS DAL13L BS2 — 8641 E24 — 74H74 E19

MTDA MDR CLK I H — MTDA CLR I L

STKC SB13 J19 — STKC SA13 J20 — R201 — 7528 E22 — D20 D672 — D19 D672 — MTDB STROBE I H

+5V — R52 1K — 74H04 E21

+5V — C45 6.8 MF — R46 120 — R49 2.0 3W — C42 3300 PF — R45 33 — 7437 E20 — Q11 3762 — J18 MTDF INH 13 — D16 D672 — R50 5.1

BIT 14

MTDF RAW A14 H — BUS DAL14L BU2 — 8641 E24 — 74H74 E27

MTDA MDR CLK I H — MTDA CLR I L

STKC SB14 J23 — STKC SA14 J24 — R201 — 7528 E23 — D22 D672 — D21 D672 — C50 120PF — MTDB STROBE I H

+5V — R62 1K — 74H04 E21

+5V — C55 6.8 MF — R55 120 — R60 2.0 3W — C52 3300 PF — R54 33 — 7437 E20 — Q16 3762 — J22 MTDF INH 14 — D26 D672 — R61 5.1

BIT 15

MTDF RAW A15 H — BUS DAL15L BV2 — 8641 E24 — 74H74 E27

MTDA MDR CLK I H — MTDA CLR I L

STKC SB15 J27 — STKC SA15 J26 — R201 — 7528 E23 — D23 D672 — D24 D672 — MTDB STROBE I H

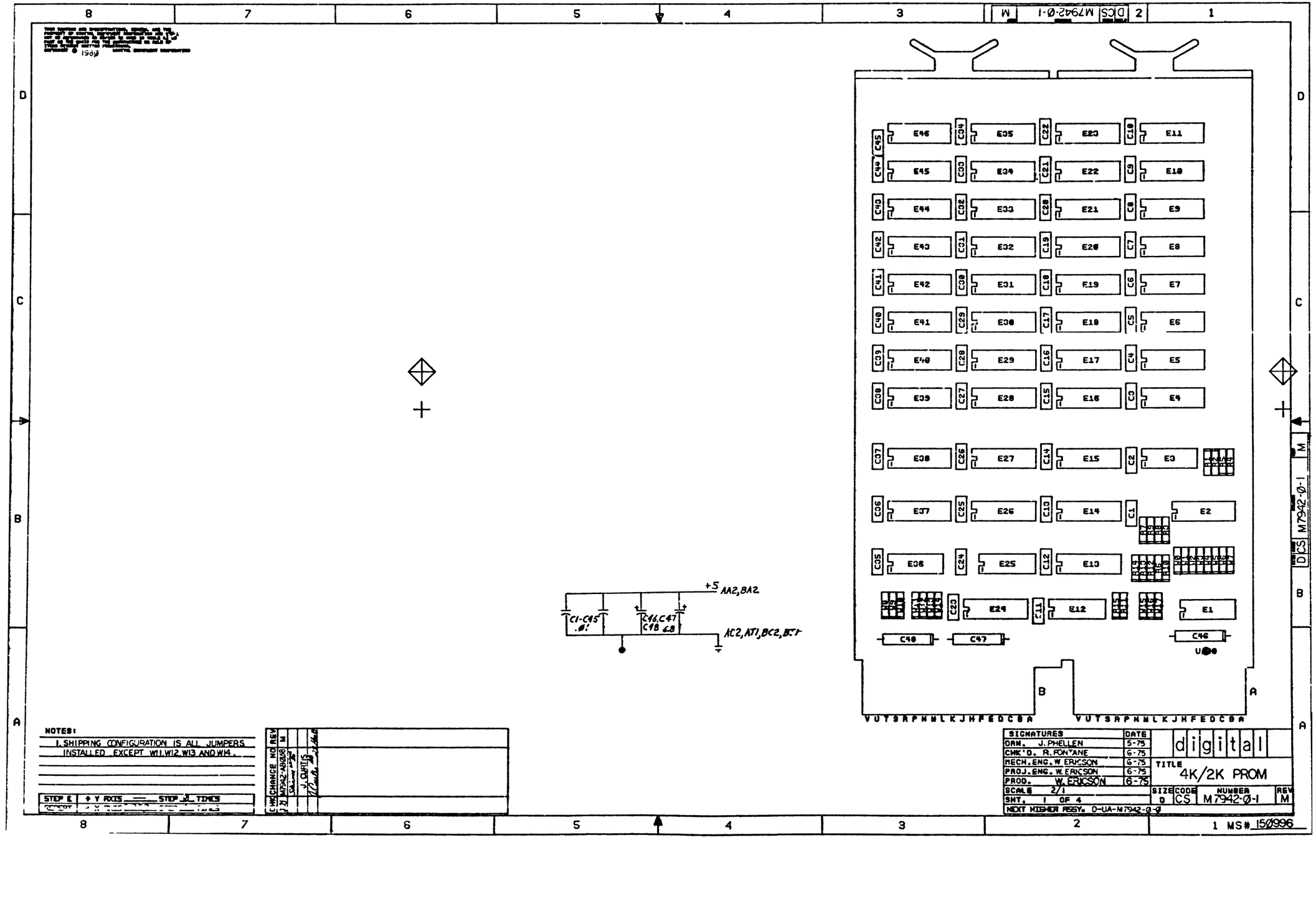
+5V — R63 1K — 74H04 E21

+5V — C54 6.8 MF — R57 120 — R59 2.0 3W — C53 3300 PF — R56 33 — 7437 E20 — Q9 3762 — J25 MTDF INH 15 — D25 D672 — R58 5.1

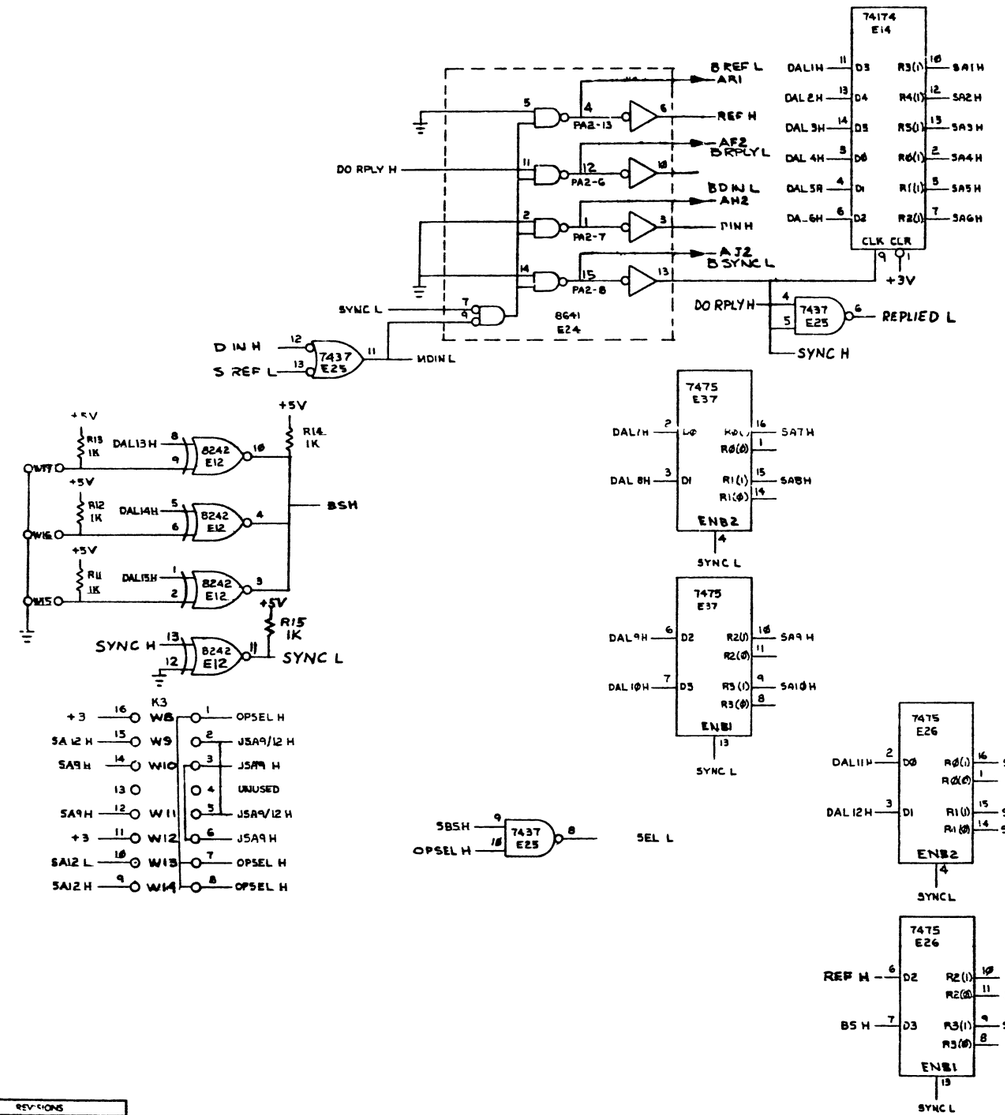
(SENSE INHIBIT BIT-12-15)

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	MMV11-A 4KX16 BIT MEMORY (MTDF)	SIZE	CODE	NUMBER / REV.
		D	CS	G653-0-1 F
SCALE	SHEET 8 OF 8	DIST.		


8
7
6
5
4
3
2
1
M
DCS M7942-0-1
D
C
B
A
E46 C34 E35 C22 E23 C10 E11
C45 C44 E45 C33 E34 C21 E22 C9 E10
C43 E44 C32 E33 C20 E21 C8 E9
C42 E43 C31 E32 C19 E20 C7 E8
C41 E42 C30 E31 C18 E19 C6 E7
C40 E41 C29 E30 C17 E18 C5 E6
C39 E40 C28 E29 C16 E17 C4 E5
C38 E39 C27 E28 C15 E16 C3 E4
C37 E38 C26 E27 C14 E15 C2 E3
C36 E37 C25 E26 C13 E14 C1 E2
C35 E36 C24 E25 C12 E13
C23 E24 C11 E12 E1
C48 C47 C46
B A
V U T S R P N M L K J H F E D C B A
+5
AA2,BA2
C1-C45 .01
C46,C47 C48 6.8
AC2,AT1,BC2,BT1
NOTES:
1. SHIPPING CONFIGURATION IS ALL JUMPERS INSTALLED EXCEPT W11,W12,W13 AND W14.
STEP E
+Y PCOS
STEP -X TIMES
CHG NO
CHANGE NO
REV
J1 M7942-A60/08
M
J. CURTIS
SIGNATURES
DATE
DRN. J. PHELLEN 5-75
CHK'D. R. FONTANE 6-75
MECH. ENG. W ERICSON 6-75
PROJ. ENG. W. ERICSON 6-75
PROD. W. ERICSON 6-75
SCALE 2/1
SHT. 1 OF 4
NEXT HIGHER ASSY. D-UA-M7942-0-0
digital
TITLE
4K/2K PROM
SIZE D
CODE CS
NUMBER M7942-0-1
REV M
MS# 150996

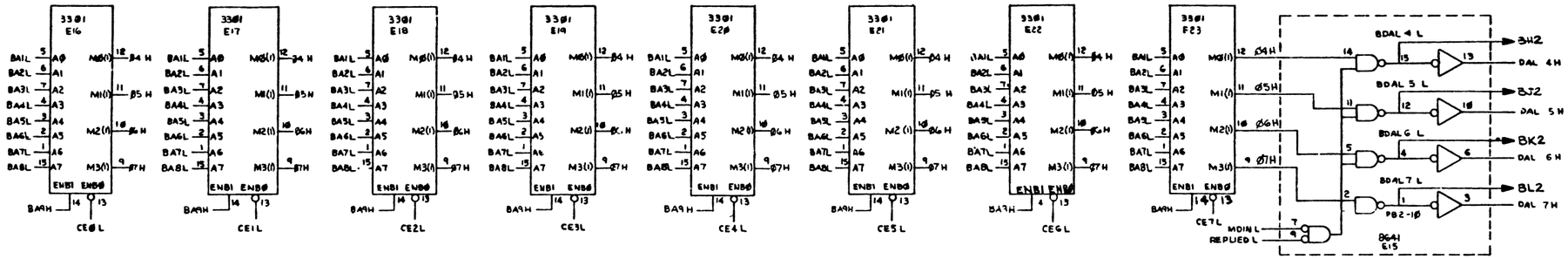
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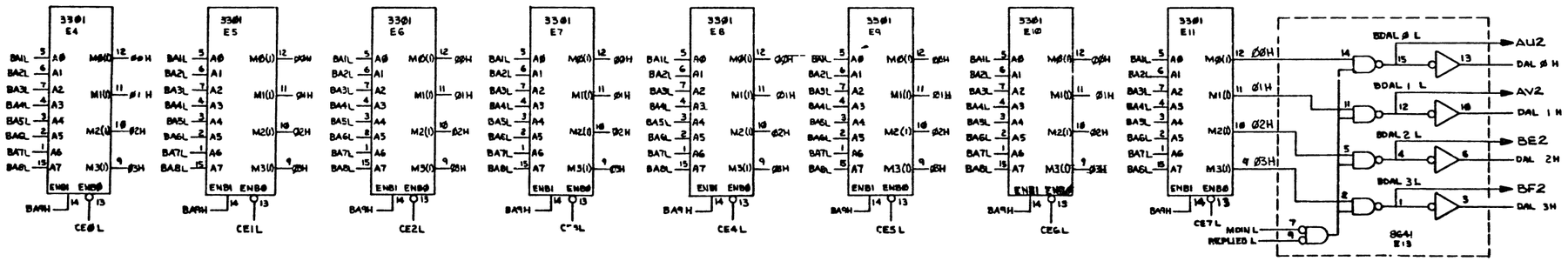


REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
4K/2K PROM	D	CS	M7942-0-1	M
SCALE —	SHEET 2 OF 5	DIST		

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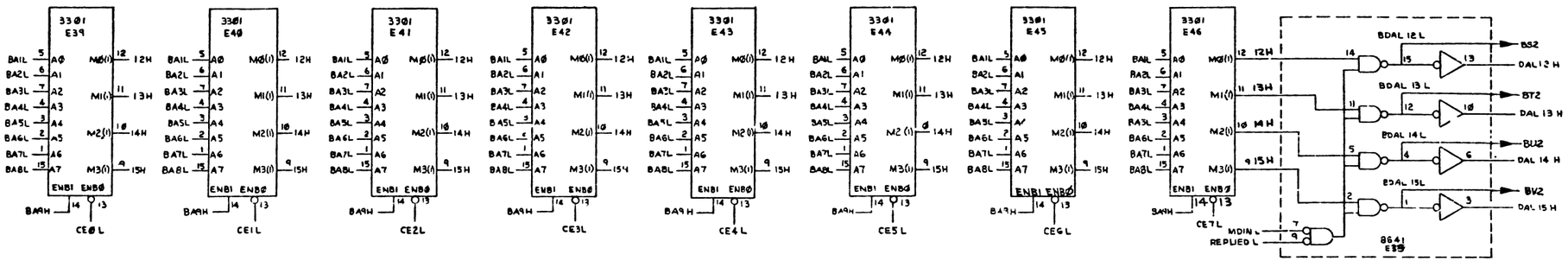


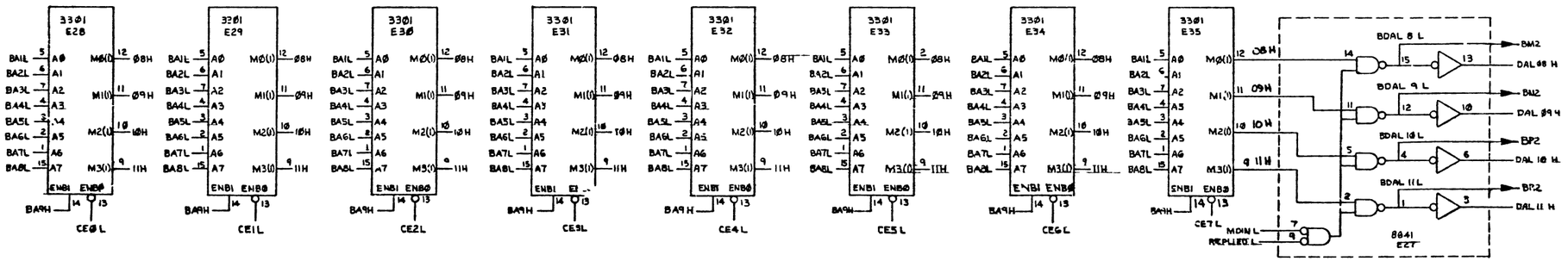
REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
4K/2K PROM	D	CS	M7942-Ø-1	M
SCALE —	SHEET 3 OF 4	DIST.		

8 7 6 5 4 3 2 1

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REV SIGNS		
CHK	CHANGE NO	REV

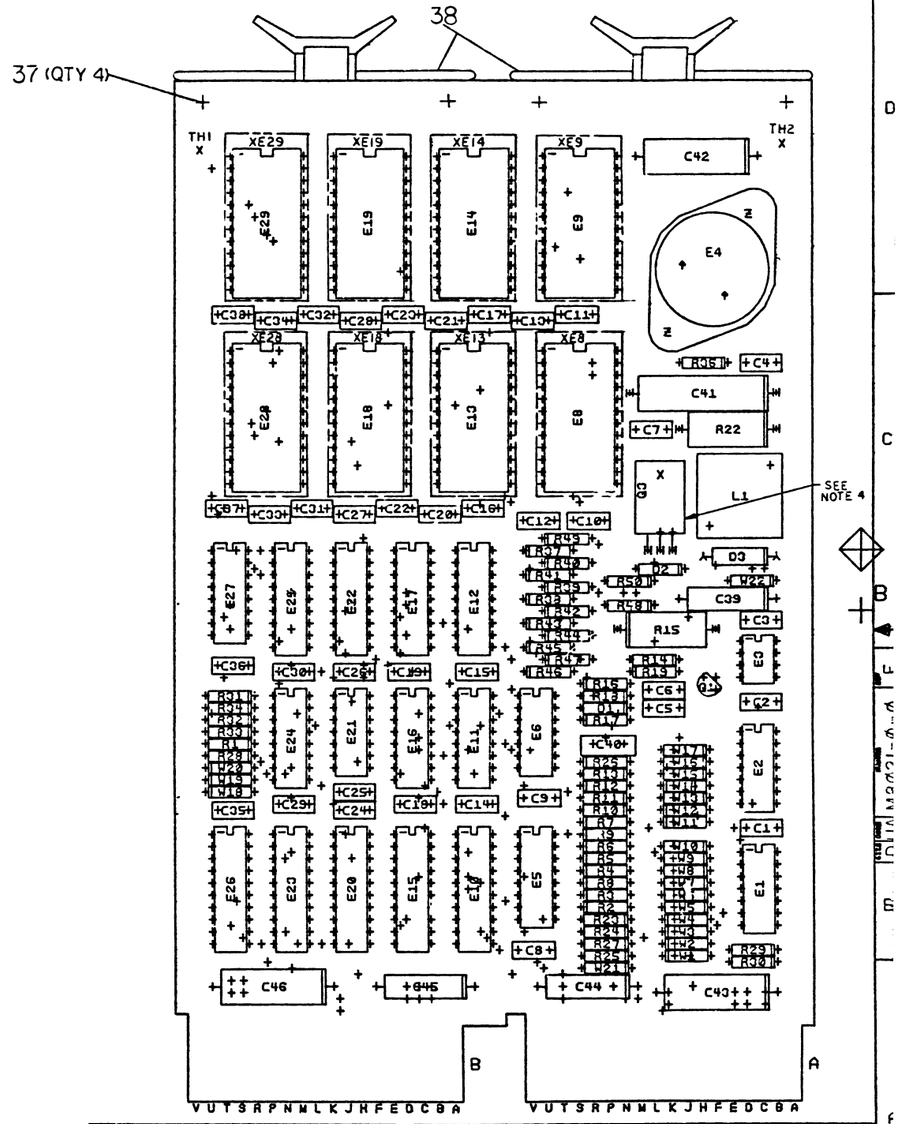
DEC FORM NO. DNS 330

TITLE	SIZE	CODE	NUMBER	REV
4K/2K PROM	D	CS	M7942-0-1	M
SCALE — SHEET 4 OF 4	DIST			

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NOTES CONT.

5. PART NO 1001610-01 IS AN ALLOWABLE SUBSTITUTE FOR PART NO 10016 0-00
6. PART NO. 2113106-00 FOR PAN DESIGNATIONS E12, E17, E22, E25, IS ACCEPTABLE AS A VENDOR TYPE "3111A4 OR "2111A4.
7. REMOVE THE FOLLOWING UNUSED FINGERS ON ARTWORK: AB1, AE1, AF1, AH1, AL1, AN1, AP1, AR1, AS1, AU1, BB1, BC1, BD1, BE1, BF1, BH1, BK1, BL1, BN1, BP1, BR1, BS1, AL2.



NOTES:
1. AT SOLDER WAVE TIME, MASK OFF X HOLES (TH1 & TH2)
2. W7, W10, W16, W19 W20 & W22 ARE OPTIONAL
3. E8, E9 E13, E14, E18, E19, E28 & E29 ARE OPTONAL AND IS PICKED UP AT A HIGHER ASSEMBLY
4. PLACE INSULATOR (ITEM #43) UNDER Q3 (TRANSISTOR) BEFORE MOUNTING.

CHG	CHANGE NO	REV
	M8021-1	D
	M8021-A0004	E
	M8021-A0004	F

ETCH REV.	E-P1
P.C. DESIGN DATA BASE REV.	E

SIGNATURES	DATE
DRN. E. WILSON	16FEB77
CHK'D. R.W. CAUMTER	23FEB77
ENG. T. WITOWSKI	27FEB77
PROJ.ENG. R.FITCH	4APR77
PROD. W. SIPILA	4APR77

digital

TITLE LSI 11 UV PROM RAM

SCALE = 2/1 | SHT. 1 OF 1 | NEXT HIGHER ASSY. 8-00-M8021-0

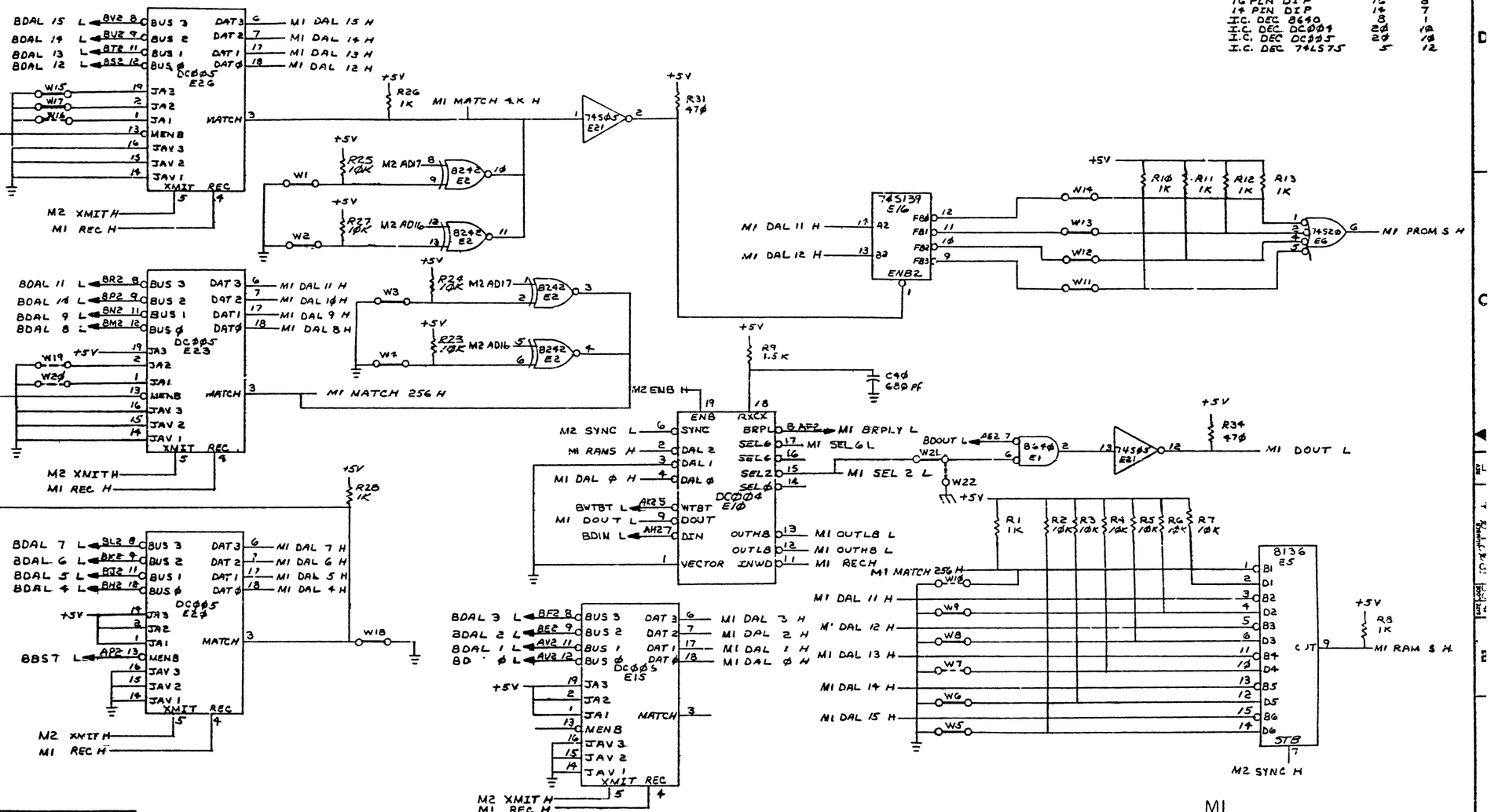
SIZE	CODE	NUMBER	REV
D	UA	M8021-0-0	F

MS#

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NOTE:
1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
I.C. DEC 8640	8	1
I.C. DEC DC0004	20	10
I.C. DEC DC0005	20	10
I.C. DEC 74LS75	5	12



REVISIONS		
DW	CHANGE NO.	REV.
CSM8021-00001		C
J. WITOWSKI SEPT 77		
M8021-MR002		D
S. EARLS Feb 78		
M8021 - A8004		E
PAPA		
M8021 ABOSA		F
S. CURTIS 28 April 78		

M1

DRN. J. Wilson	14 Feb 77	FIRST USED ON MRV11-BA
CHK'D R. Scott	4 MAR 77	digital
ENG.	4 APR 77	TITLE
PROJ. ENG.	4 MAR 77	LSI 11 UV PROM RAM
PROD.	4 APR 77	
NEXT HIGHER ASSY.	B-DD-M8021-0	SIZE D CODE CS NUMBER M8021-0-1 REV. -
SCALE	NONE	
SHEET	1 OF 4	DIST.

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74LS75 E27
M1 DAL 1 H
M1 DAL 2 H
M1 DAL 3 H
M1 DAL 4 H
M2 SYNC L
R49 1.5K R38 1.5K R39 1.5K R40 1.5K +5V
M2 BA1 H
M2 BA2 H
M2 BA3 H
M2 BA4 H

74LS75 E27
M1 DAL 5 H
M1 DAL 6 H
M1 DAL 7 H
M1 DAL 8 H
R41 1.5K R42 1.5K R43 1.5K R44 1.5K +5V
M2 BA5 H
M2 BA6 H
M2 BA7 H
M2 BA8 H

74LS75 E11
M1 DAL 9 H
M1 DAL 10 H
M1 DAL 11 H
M1 DAL 12 H
R45 1.5K R47 1.5K +5V
M2 BA9 H
M2 BA10 H

M1 SEL 2 L
M1 SEL 6 L
7432 E6
M2 XMIT H

M1 RAM S H
M1 PROM S H
74S03 E21
R33 470 +5V
M2 ENB H

BAD 17
BAD 16
R29 10K +5V
R30 10K +5V
864 E1
M2 ADI7
M2 ADI6

BSYNC L AJ2
M2 SYNC H
74S03 E21
M2 SYNC L
R32 470 +5V

74S139 E16
M1 SEL 6 L
M2 CE0 (1K)
M2 CE1 (2K)
M2 CE2 (3K)
M2 CE3 (4K)
R46 1.5K R48 1.5K R37 1.5K

BDMG I L AR2 AS2 BDMGO L
BIAK I L AM2 AN2 BIAKO L

8111A-4 E12
M2 BA1 H
M2 BA2 H
M2 BA3 H
M2 BA4 H
M2 BA5 H
M2 BA6 H
M2 BA7 H
M2 BA8 H
M1 DAL 15 H
M1 DAL 14 H
M1 DAL 13 H
M1 DAL 12 H
M1 REC H
M1 OUT HB L
M1 SEL 2 L

8111A-4 E17
M2 BA1 H
M2 BA2 H
M2 BA3 H
M2 BA4 H
M2 BA5 H
M2 BA6 H
M2 BA7 H
M2 BA8 H
M1 DAL 11 H
M1 DAL 10 H
M1 DAL 9 H
M1 DAL 8 H
M1 REC H
M1 OUT HB L
M1 SEL 2 L

8111A-4 E22
M2 BA1 H
M2 BA2 H
M2 BA3 H
M2 BA4 H
M2 BA5 H
M2 BA6 H
M2 BA7 H
M2 BA8 H
M1 DAL 7 H
M1 DAL 6 H
M1 DAL 5 H
M1 DAL 4 H
M1 REC H
M1 OUT LB L
M1 SEL 2 L

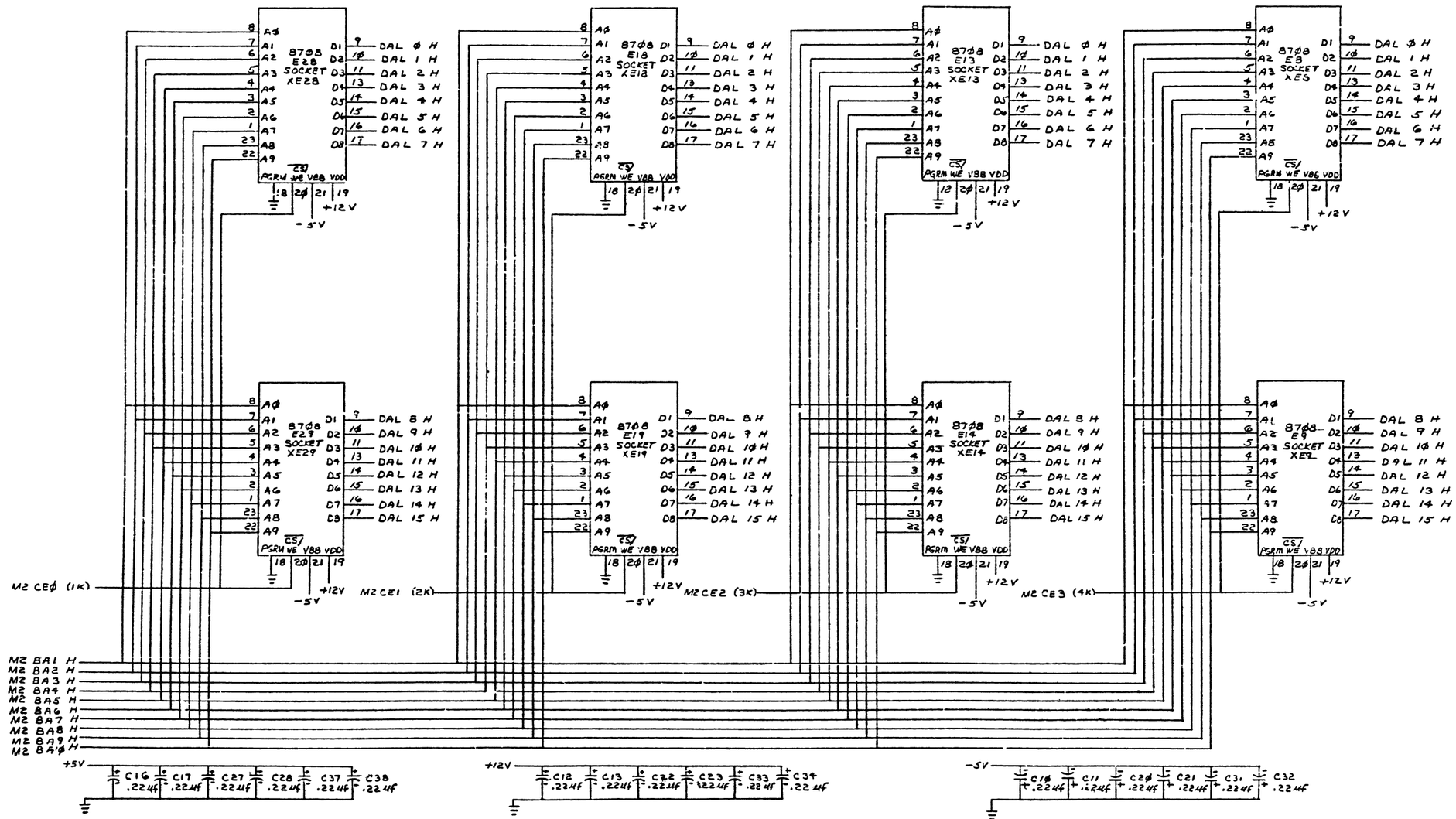
8111A-4 E25
M2 BA1 H
M2 BA2 H
M2 BA3 H
M2 BA4 H
M2 BA5 H
M2 BA6 H
M2 BA7 H
M2 BA8 H
M1 DAL 3 H
M1 DAL 2 H
M1 DAL 1 H
M1 DAL 0 H
M1 REC H
M1 OUT LB L
M1 SEL 2 L

REVISIONS
CHK | CHANGE NO. | REV.

M2
TITLE LSI11 UV PROM RAM
SCALE NONE SHEET 2 OF 4
SIZE D CODE DCSM8021-0-1 REV F
DIST.

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NOTES:
2. ALL I.C.'S SHOWN ON THIS PAGE ARE OPTIONAL.
3. SOURCE FOR "DAL Ø H" THRU "DAL 7 H" S SHT 1 (M11).

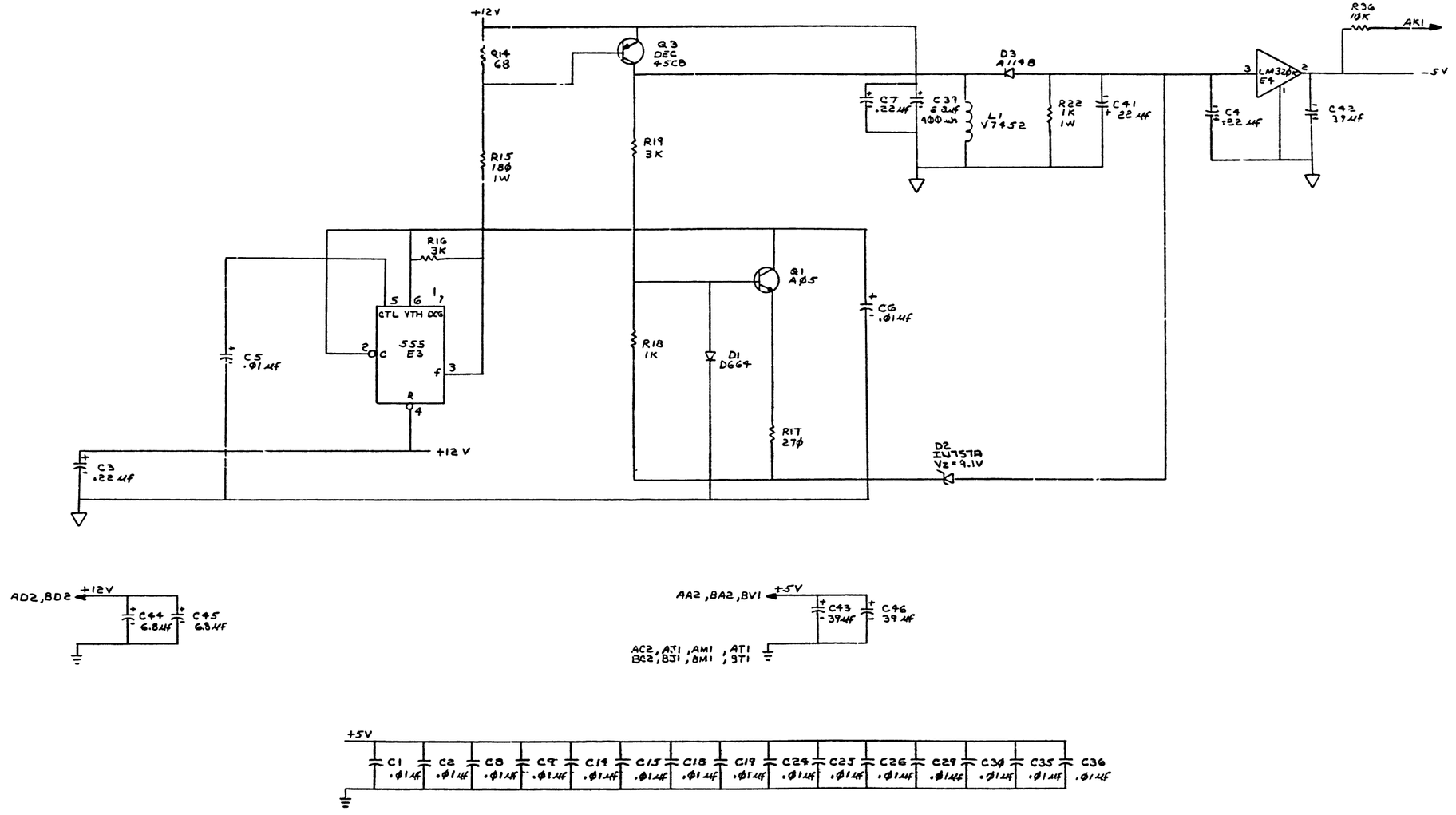


M3: UV PROM

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 UV PROM RAM	D	CS	M8Ø21-Ø-1	F
SCALE NONE SHEET 3 OF 4	DICT.			

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REVISIONS		
CHK	CHANGE NO.	REV.

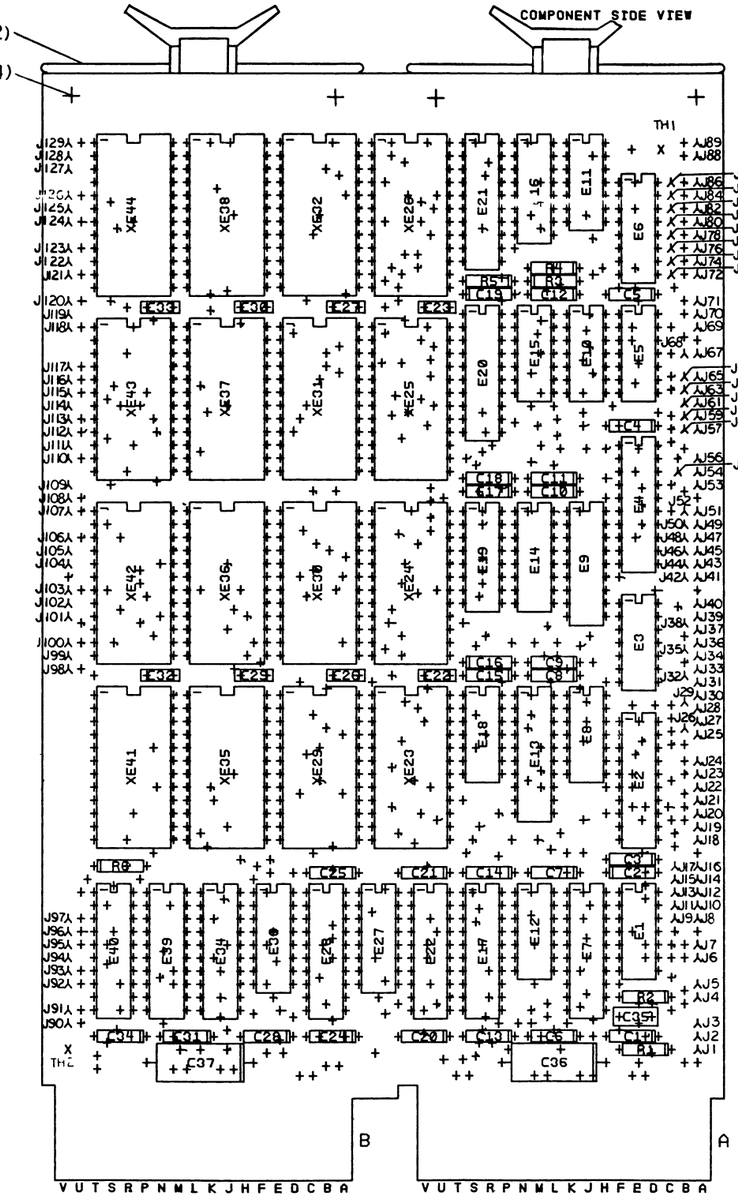
M4: -5V PWR SUPPLY

TITLE	LSI11 UV PROM RAM				
SIZE	CODE	NUMBER			REV.
D	CS	M8021-0-1			F
SCALE	NONE	SHEET 4 OF 4			

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26(QTY 2)
27(QTY 4)

COMPONENT SIDE VIEW



NOTES:

CHK	CHANGE NO	REV
mp	M8048-1	B

M. Moore 4 Feb 81
B. LOCKE
Hugh Reid 9 Feb 81

ETCH REV.
P.C. DESIGN DATA BASE REV. B

SIGNATURES	DATE
DRN.	27 FEB 81
CHK'D. M. Pecault	28 Feb 81
ENG. Leon Locke	3-16-81
PROJ. ENG. Leon Locke	3-16-81
PROD. AL JOHNS	2 SEP 81
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-CD-M8048-0	

digital

TITLE: LSI 11 ROM

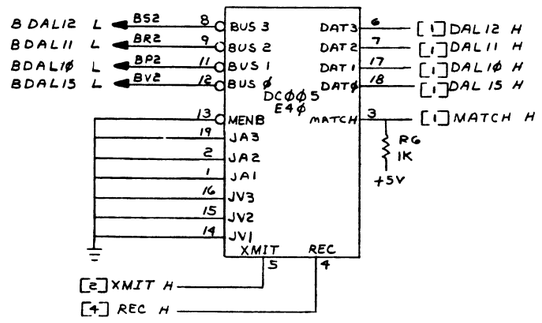
SIZE	CODE	NUMBER	REV
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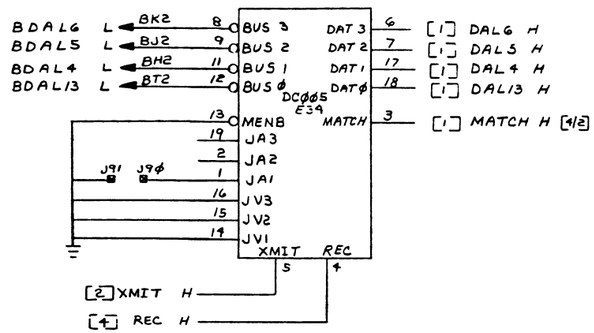
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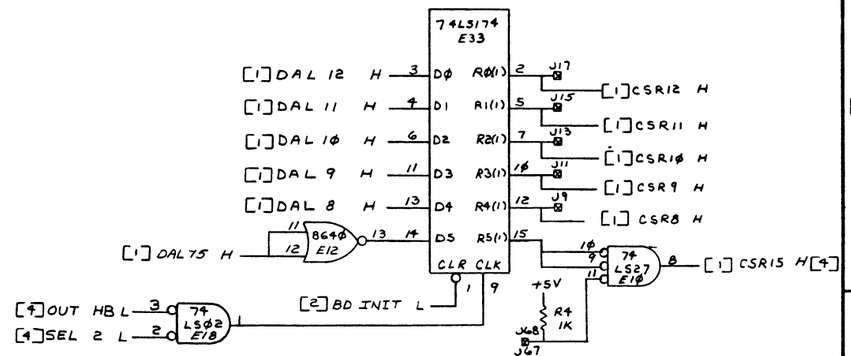
D | UA | M8048-0-0 | B

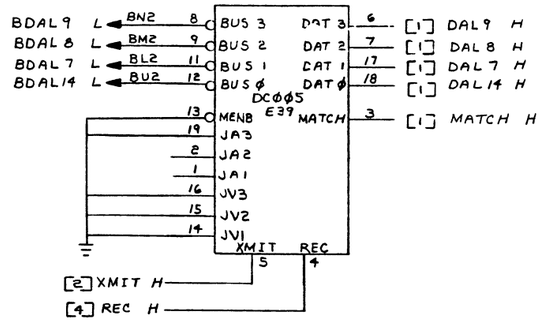
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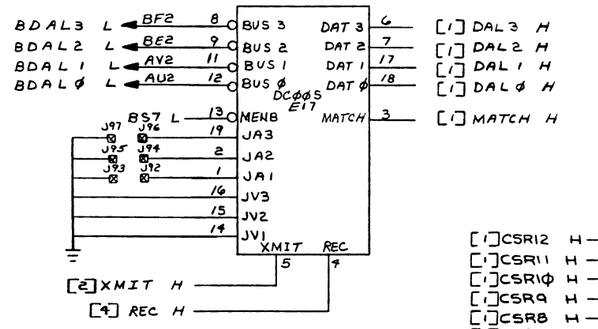
CSR

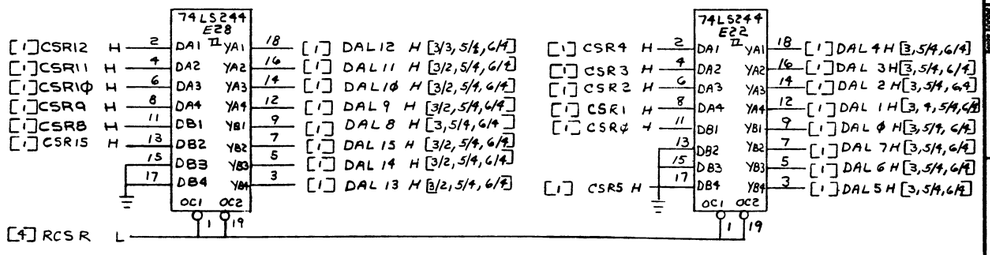












REVISIONS		
CHK	CHANGE NO.	REV.
MF	MR001	B

B-LOCKE

DRN.	E. Wilson	10/16/78
CHK.		
ENG.		
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.	B-DD-M8Ø48-Ø	
SCALE	NONE	
SHEET	1 OF 6	

FIRST USED ON LSI11/2

TITLE: LSI11 ROM

SIZE	CODE	NUMBER	REV.
D	CS	M8Ø48-Ø-1	B

DIST.

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74LS244 E4 — RA12 H, RA11 H, RA1Ø H, RA9 H, RA4 H, RA3 H, RA2 H, RA1 H

[4]PADR H, [3] AD11 H → 74 LS ØØ E8

RA8 H → 74 LS125 E3

[4] DADR L, [4]PADR H, [2 AD11 L → 74 LS ØØ E8

RAØ H → 74 LS125 E5

+5V → E15 1K

74 LS240 E2

74 LS125 E5

74LS138 E6 — SEL C, SEL B, SEL A; DØ D1 D2 D3 D4 D5 D6 D7

[4]PADR H, [3] BOOT H, [2]DADR H → 74 LS27 E10 → [3]WRITE H, [3] SYNC H → EN

[1]CE7 [4], [2]CE6 [4], [2]CE5 [6], [2]CE4 [6], [2]CE3 [5], [2]CE2 [5], [2]CE1 [5], [2]CEØ [5]

+5V → E15 1K

74 LS ØØ E11 → [2] ENB H [4]

[4]DADR L → 74 LS240 E13 → [2]DADR H

[3] AD11 H → 74 LS240 E13 → [2]AD11 L

[3]BS7 H → 74 LS240 E13 → [2]BS7 L

[4]RXCX → 74 LS240 E13 → [2]XMIT H [1/7]

[3]BOOT H → 74 LS240 E13 → [2] BOOT L

[4]INWD L → 74 LS240 E13 → [2]INWD H [4/2]

[3]WTBT H → 74 LS240 E2 → [2] WTBT L [4]

[3]BD INIT H → 74 LS240 E2 → [2] BD INIT L [1/2]

SSPARE 3 → AH1 → +5V E15 1K

74 LS240 E2 → [2] BD OFF [3]

[3]SYNC H → 74 LS240 E2 → [2] SYNC L [3/2,4/2]

[2] BOOT L → 74 LS125 E5 → [2] A11 H [3,5,6]

[2] A12 H [5/6]

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 ROM	D	CS	M8Ø43-Ø-1	B
SCALE	SHEET 2 OF 6	DIST.		

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BAD16 L ← AC1 — 8640 E1 — [3] AD16 H [4]

BAD17 L ← AD1 — 8640 E1 — [3] AD17 H [4]

BDCOK H ← BA1 — 8640 E1 — [3] BD INIT H [1]

BSYNC L ← AT2 — 8640 E1 — [3] SYNC H [2/2]

BD OFF

BBS7 L ← AP2 — 8640 E12 — [3] BS7 H [2]

BWTBT L ← AK2 — 8640 E12 — [3] WTBT H [2]

74LS373 E21

[1] DAL1 H → D6 → R6(1) → [3] AD1 H [5/6]
[1] DAL2 H → D1 → R1(1) → [3] AD2 H [5/6]
[1] DAL3 H → D2 → R2(1) → [3] AD3 H [5/6]
[1] DAL4 H → D3 → R3(1) → [3] AD4 H [5/6]
[1] DAL5 H → D4 → R4(1) → [3] AD5 H [5/6]
[1] DAL6 H → D5 → R5(1) → [3] AD6 H [5/6]
[1] DAL7 H → D6 → R6(1) → [3] AD7 H [5/6]
[1] DAL8 H → D7 → R7(1) → [3] AD8 H [5/6]
OC, EN
[2] SYNC L

74LS373 E20

[1] DAL9 H → D6 → R6(1) → [3] AD9 H [5/6]
[1] DAL10 H → D1 → R1(1) → [3] AD10 H [5/6]
[1] DAL11 H → D2 → R2(1) → J25
[1] DAL12 H → D3 → R3(1) → J28
[1] DAL13 H → D4 → R4(1) → J31
[1] DAL14 H → D5 → R5(1) → J34
[1] DAL15 H → D6 → R6(1) → J37
[3] WTBT H → R7(1) → [3] WRITE H [2]
OC, EN
[2] SYNC L

[3] AD11 H
[3] AD12 H
[3] AD13 H [4]
[3] AD14 H [4]
[3] AD15 H [4]

+5V — E3 10K

[1] DAL12 H — J51 J52 — 13
[1] DAL13 H — J41 J42 — 12
[1] DAL14 H — J43 J44 — 11
[1] DAL15 H — J45 J46 — 16
[1] AD16 H — J47 J48 — 9
[1] AD17 H — J49 J50 — 8

8136 E14

B1 ← 1
D1 ← 2
B2 ← 3
D2 ← 4
B3 ← 5
D3 ← 6
B4 ← 11
D4 ← 10
B5 ← 13
D5 ← 12
B6 ← 15
D6 ← 14
S78 ← 7
OUT → 9 → [3] P ADR H [2/3,4]

+5V — E15 1K — J7
J6

[3] SYNC H

+5V — R5 1K

[3] BS7 H → 1
[1] DAL12 H → 3
[1] DAL10 H → 5
[1] DAL9 H → 7
[1] DAL11 H → 13

8136 E16

B1 ← 1
D1 ← 2
B2 ← 3
D2 ← 4
B3 ← 5
D3 ← 6
B4 ← 11
D4 ← 10
B5 ← 13
D5 ← 12
B6 ← 15
D6 ← 14
S78 ← 7
OUT → 9 → [3] BOOT H [2/2,4]

+5V — E15 1K — J88 J89 — 3

+5V — R3 1K

[3] SYNC H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 ROM	D	CS	M8048-0-1	B
SCALE	SHEET 3 OF 6		DIST.	

DCS M8048-0-1 REV B

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74LS75 E19

[3] AD16 H — 2 D0 — R0(1) 16 — [4] A16 H
R0(0) 1
[3] AD17 H — 3 D1 — R1(1) 15 — [4] A17 H
R1(0) 14
[1] MATCH H — 6 D2 — R2(1) 10
R2(0) 11 — [4] L MATCH H / [4] L MATCH L
[1] CSR15 H — 7 D3 — R3(1) 9
R3(0) 8
ENB1 13 ENB2 4
[2] SYNC L

74LS125 E5: 12 → 11 [3] PADR H [2/3]; 13

J59 J57 J61 J63 J65

+5V
E3 10K
J60 6 5 1 3 4 15
1K X 4 PROM E9
D9 16 D8 17 D7 1 D6 2 D5 3 D4 4 D3 7 D2 6 D1 5 D0
[4] A17 H
[4] A16 H
[3] AD15 H
[3] AD14 H
[3] AD13 H
CE1 8 CE2 18
[3] PADR H
[3] BOOT H
M4 11 M3 12 M2 13 M1 14
J53 J54 J56

+5V
E15 1K
J55 2 [4] DADR L [2/2]

+5V
R2 3.83K
+5V
R1 3.83K
J1
J3 [4] RXCX [2]
J2
C35 220 pf

[2] ENB H — 74LS02 E18 (8, 9 → 10)
[2] SYNC L — 11
[2] L MATCH L — 12
74LS02 E18 (11, 12 → 13)

74LS04 E7 (19 / 18)
ENB 6 — 74LS02 E18 (10)
SYNC
DC004
DAL2 2 — [1] MATCH H
DAL1 3
DAL0 4 — [1] DAL0 H
WTBT 5 — [2] WTBT L
DOUT 9
DIN 7 — BDIN L AH2
VECTOR 1
RXCX 18
BRPLY 8 AF2 — BRPLY L
SEL6 17
SEL4 16
SEL2 15 — [4] SEL 2 L [1/2]
SEL0 14
OUTHB 13 — [4] OUT L8 L [1]
OUTLB 12 — [4] OUT H8 L [1]
INWD 11 — [4] INWD L [2]

BDOUT L — AE2 9 — 8640 E12 (14, 10) — 74LS00 E8 (10, 9 → 8)

[4] L MATCH H — J5 — J4 — 7 — E3 10K — +5V

[2] ENB H — 3, 4, 5 — 74LS27 E10 — 6 — [4] REC H [1/8]
[2] INWD H

[4] L MATCH H — 5 — 74LS00 E8 — 6 — [4] RCSR L [1]
[2] INWD H — 4

BDMG1 L — AR2 → AS2 — BDMGO L

BIAK1 L — AM2 → AN2 — BIAKO L

REVISIONS

CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 ROM	D	CS	M8048-Ø-1	B

SCALE — SHEET 4 OF 6 — DIST

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SOCKET XE43
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
19 21 18 20
D1 D2 D3 D4 D5 D6 D7 D8
9 10 11 13 14 15 16 17
[1] DAL0 H
[1] DAL1 H
[1] DAL2 H
[1] DAL3 H
[1] DAL4 H
[1] DAL5 H
[1] DAL6 H
[1] DAL7 H
[2] CE0

SOCKET XE44
[1] DAL8 H
[1] DAL9 H
[1] DAL10 H
[1] DAL11 H
[1] DAL12 H
[1] DAL13 H
[1] DAL14 H
[1] DAL15 H

SOCKET XE37
[2] CE1

SOCKET XE38
J118 J120 J119 J121 J123 J122

SOCKET XE31
[2] CE2

SOCKET XE32
J124 J126 J125

SOCKET XE25
[2] CE3

SOCKET XE26
J127 J129 J128

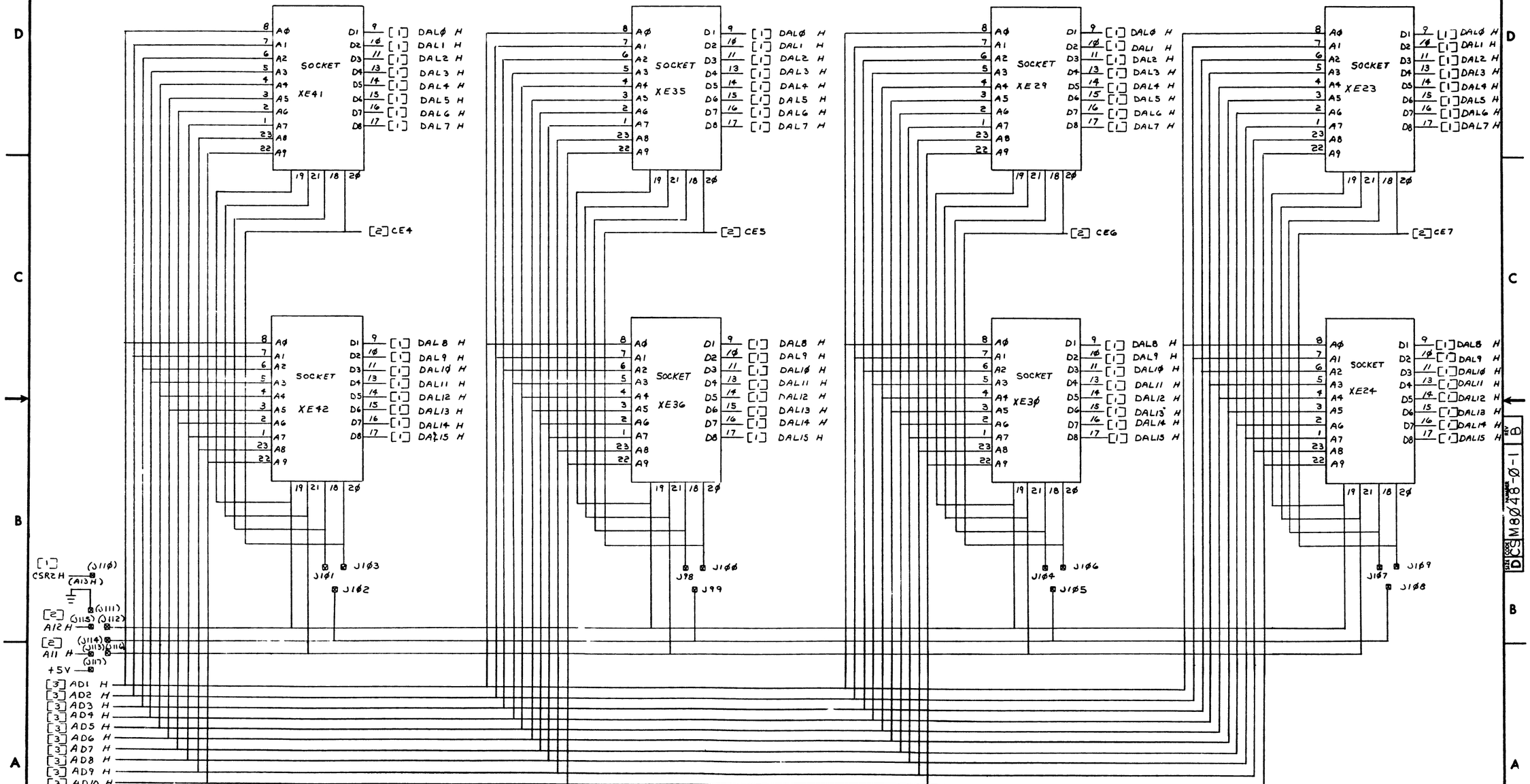
[1] CSR2 H (A13H) — J110
J111 J115 J112
[2] A12 H
J114 J116
[2] A11 H — J113
+5V — J117

[3] AD1 H
[3] AD2 H
[3] AD3 H
[3] AD4 H
[3] AD5 H
[3] AD6 H
[3] AD7 H
[3] AD8 H
[3] AD9 H
[3] AD10 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
LSI11 ROM	D	CS	M8Ø48-Ø-1	B
SCALE	SHEET 5 OF 6	DIST.		

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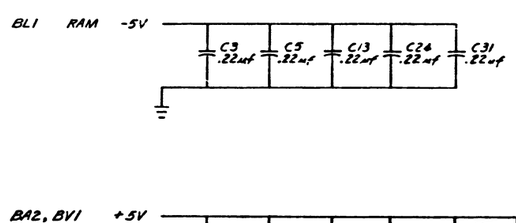
REVISIONS		
CHK	CHANGE NO	REV

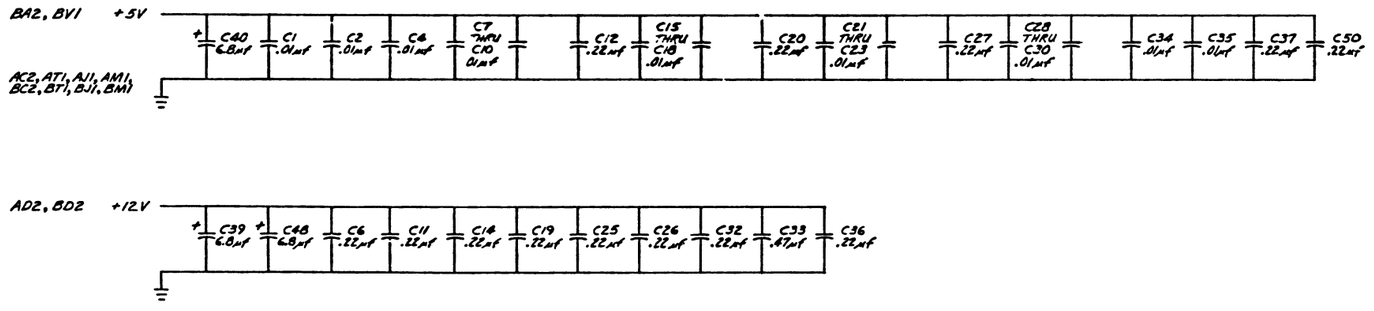
TITLE	SIZE	CODE	NUMBER	REV.
LSI11 ROM	D	CS	M8048-0-1	B
SCALE	SHEET 6 OF 6	DIST.		

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NOTES:

1. W4 IS A CUSTOMER OPTION NOT TO BE INSERTED
2. DIP SWITCH, 1211164, WILL REPLACE W1 THROUGH W4 ON MODULES RETURNED TO MRC WOBURN ONLY.





4K RAM	16	9	8			1
I.C. MH0026C	3		6			
I.C. DEC 75107	7	14		13		
I.C. DEC 74123	8	16				
I.C. DEC 8641	8	16				
I.C. DEC 745257	8	16				
I.C. DEC 7475	12	5				
IC TYPE	GND	+5V	+12	-5	-9	-5 RAM
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE						
IC PIN LOCATIONS						

REV.	CHANGE NO.	CHK	DESCRIPTION
J	M7344-00007		
K	M7944-A0010		
L	M7944-A0011		
M	M7944 — PN012		

SEE OFF SHEET PARTS LIST

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO

PARTS LIST

FIRST USED ON OPTION MODEL: LSI 11

ETCH BOARD REV. C

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.		DATE 3 Nov 77
CHK'D.		DATE 12-13-77
ENG.		DATE 30 Nov 77
PROJ. ENG.		DATE 30 Nov 77
PROD.		DATE 30 Nov 77

NEXT HIGHER ASSY: MSV11-B

SCALE

SHEET 1 OF 4

digital

TITLE: 4K RAM

SIZE	CODE	NUMBER	REV.
D	CS	M7944-0-1	M

DIST.

M7944-0-1 CS D M

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SEE NOTE 1
+5V R3 1K
RPLY H
S REF L
74S00 E15
8641 E7
AH2 BDIN L
DIN H
AE2 BDOUT L
DOUT H
AJ2 BSYNC L
SYNC H
AF2 BRPLY L
7400 E16
SYNC L

+5V R13 1K
W1
DAL 15 H
8242 E28
BS H
+5V R14 1K
W2
DAL 14 H
+5V R18 1K
W3
DAL 13 H

7475 E17
REF H
S REF H
S REF L
BS H
LBS H
LBS L
DAL 0 H
SA0 H
SA0 L
SYNC L
ENBL E.80

7400 E16
WTBT H
LBS H
74S10 E8
WØ L
DOUT H
WI L

AH2 BWTBT L
WTBT H
AR1 CREF L
REF H
BA1 BDCOK H
DCOK L
8644 E2
+3V

C43 22Øpf
R11 20K +5V
3045
2µS
74123 E1
FLOP (1) L
R12 20K +5V
C44 100pf
FLCP(1)L
FLIP (1) L
74S03 E21
R16 47Ø
R15 47Ø
MM-ØØØ26C E33
C45 .47µf
C47 .47µf
D2 D664
D1 D664
D3 D664
C46 .47µf
R17 33Ø
-5V
D4 IN751A
R10 68Ø
BK1
BL1
-5 RAM
D5 IN757A

AF1 RAS L
R21 47
LBS L
S REF L
7400 E16
SYNC H
BS OR REF H
74S140 E9
74S03 E21
+5V R4 93Ø
R5 6.8K
75107 E3
PCAS H
BS OR REF H
SYNC H
74S140 E9
AE1 CAS L
R22 47
74S03 E21
+5V R9 1.2K
R2Ø
74LS132 E15
DIN H
DRIVE L
PCAS H
DOUT H
RPLY H

+5V R1 33K
+3V R2 5.6K
AM1
AL1
R6 133
R7 39.3
C50 .22µf
-5V
+3V
AMX L
C42 22Øpf
R8 133
C3 .22µf
-5V

AR2 BOMGIL — AS2 BOMGOL
AM2 BIAKIL — AN2 BIAKOL

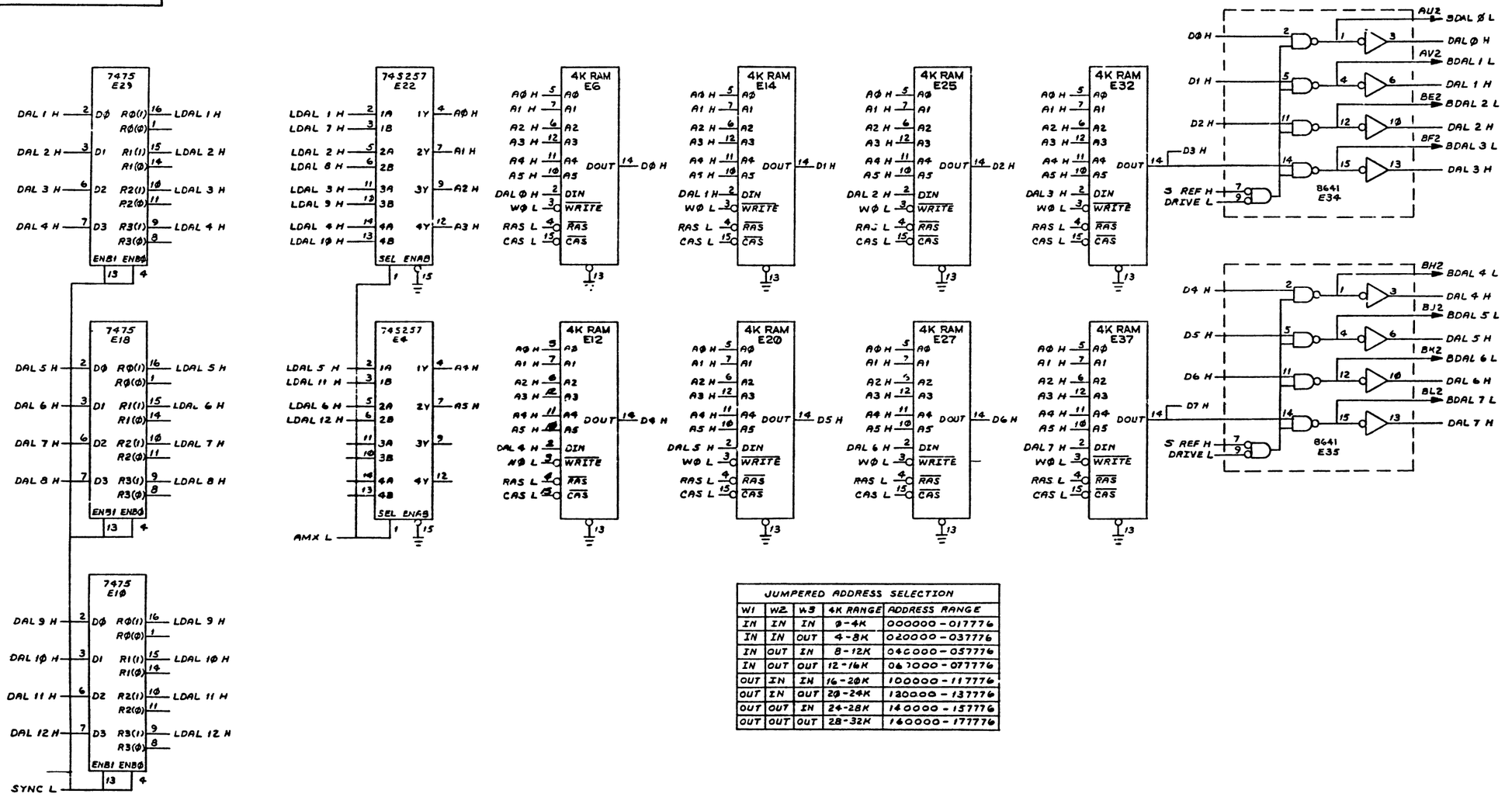
(TIMING GENERATOR & CHARGE PUMP)

REVISIONS
CHK | CHANGE NO | REV

TITLE 4K RAM
SIZE D CODE DCS NUMBER M7944-Ø-1 REV M
SCALE — SHEET 2 OF 4 DIST.

DEC FORM NO. D40 120

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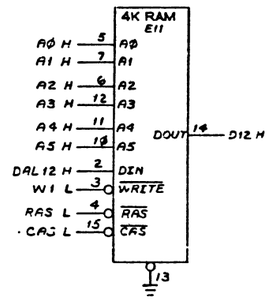
JUMPERED ADDRESS SELECTION				
W1	W2	W3	4K RANGE	ADDRESS RANGE
IN	IN	IN	0-4K	000000 - 017776
IN	IN	OUT	4-8K	020000 - 037776
IN	OUT	IN	8-12K	040000 - 057776
IN	OUT	OUT	12-16K	060000 - 077776
OUT	IN	IN	16-20K	100000 - 117776
OUT	IN	OUT	20-24K	120000 - 137776
OUT	OUT	IN	24-28K	140000 - 157776
OUT	OUT	OUT	28-32K	160000 - 177776

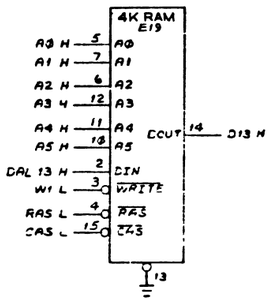
(RAM & DRIVER)

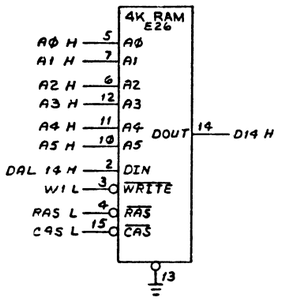
REVISIONS		
CHK	CHANGE NO	REV

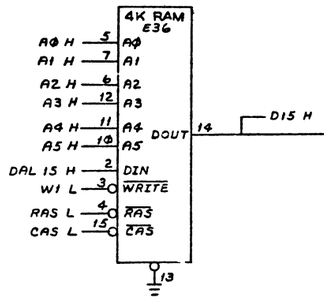
TITLE	SIZE	CODE	NUMBER	REV.
4K RAM	D	CS	M7944-0-1	M
SCALE — // — SHEET 3 OF 4	DIST.			

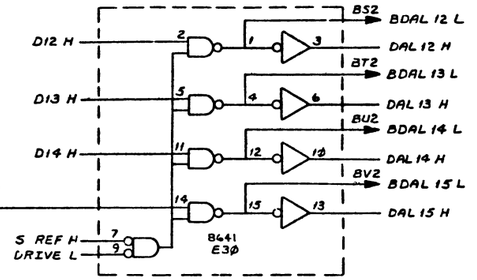
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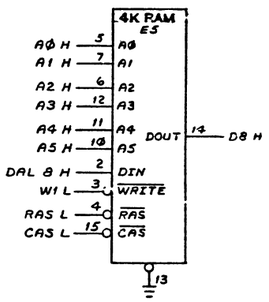


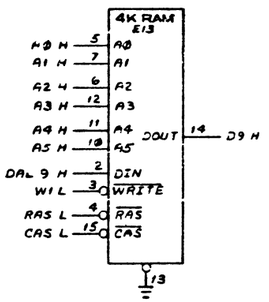


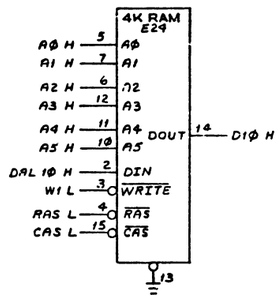


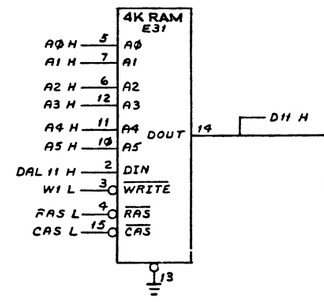


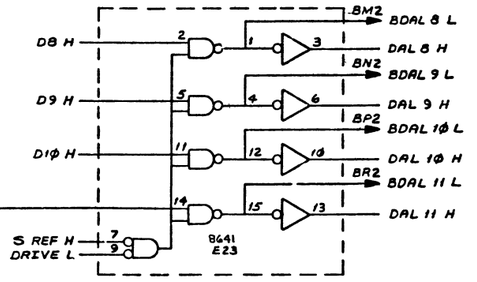












(RAM & DRIVER)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE 4K RAM
SCALE — SHEET 4 OF 4
SIZE D CODE CS NUMBER M7944-0-1 REV M
DIST.

DEC FORM NO. DEC-128

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M7955-0-0 D UA D 2

COMPONENT SIDE VIEW

63 56 62 56

MODULE VARIATION: M7955-AD

NOTE: 1. FOR M7955-AC, SEE SH. 2
2. FOR M7955-AB, SEE SH. 3
3. FOR M7955-AA, SEE SH. 4

8.44 REF

57,58 61 60 61

FOR PL, SEE B-PL-M7955-0-0

NOTES: 1. M7955-AD=M7955-YD&YJ

CHK	CHANGE NO	REV
JMC	M7955-0001A	C
	M7955-0000B	D

SIGNATURES	DATE
DRN. J. CARTER	11-11-77
CHK'D	23 NOV 77
ENG.	7 JAN 78
PROJ. ENG.	7 JAN 78
PROD.	

ETCH REV. D-P2
P.C. DESIGN DATA BASE REV. D

digital

TITLE MSVII-C MOS MEMORY, LSI

SCALE 2/1 | SHT. 1 OF 9 | SIZE D | CODE UA | NUMBER M7955-0-0 | REV D

NEXT HIGHER ASSY. B-DD-M7955-0

D UA M7955-0-0 D

1 MS#_____

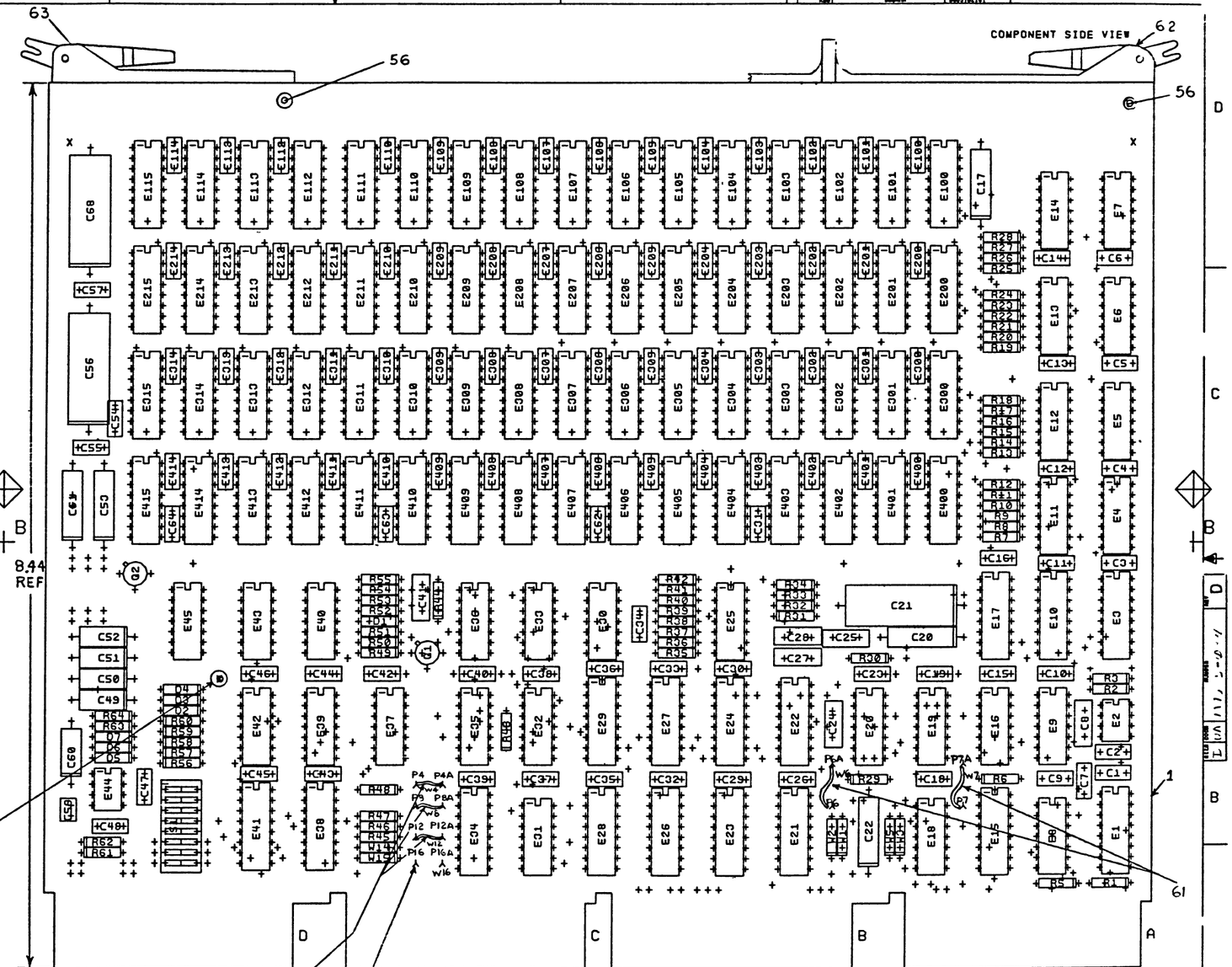
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MODULE VARIATION: M7955-AC

NOTE: 1. FOR M7955-AC, SEE SH. 2

2. FOR M7955-AB, SEE SH. 3

3. FOR M7955-AA, SEE SH. 4



NOTES: 1. M7955-AC = M7955-YC & YH

REV	CHANGE NO	CHK
C	M7955-0A01A	J.STEVENS

FOR PL, SEE B-PL-M7955-0-0

SIGNATURES	DATE
DRN. J.CARTLP	11-11-77
CHK'D. W. Jim Rita	12-NOV-77
ENG.	
PROJ.ENG.	
PROD.	
SCALE 2/1	
SHT. 2 OF 9	

ETCH REV. D-02
P.C. DESIGN DATA BASE REV. E

digital

TITLE M8VII-C MOS MEMORY, LSI

SIZE	CODE	NUMBER	REV
D	UA	M7955-0-0	D

NEXT HIGHER ASSY. B-[illegible]-0

MS#

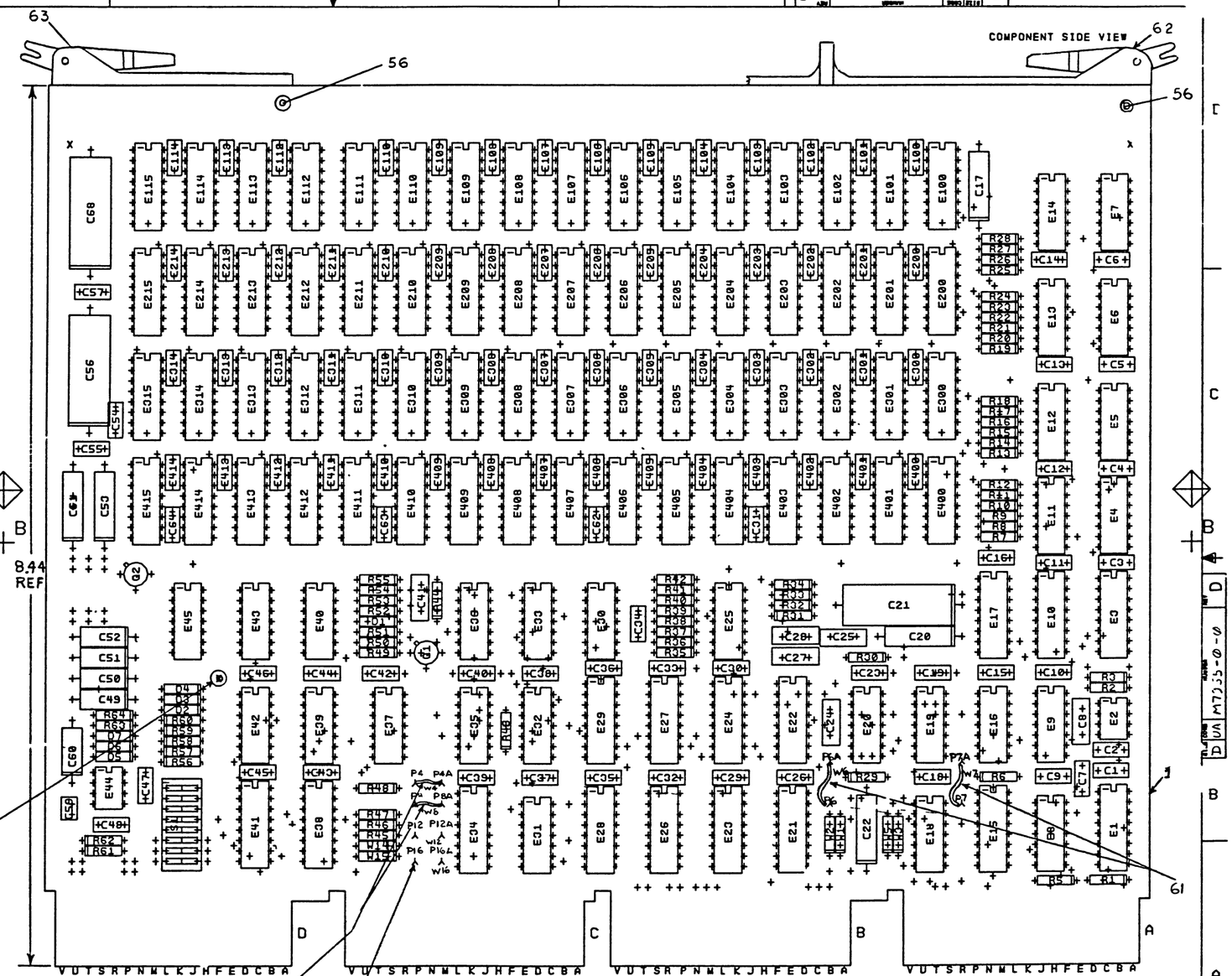
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MODULE VARIATION: M7955-AB

NOTE: 1. FOR M7955-AC, SEE SH. 2

2. FOR M7955-AB, SEE SH. 3

3. FOR M7955-AA, SEE SH. 4



NOTES: 1. M7955-AB = M7955-YB&YE

CHK	CHANGE NO	REV
JMC	M7955-0001A	C

SIGNATURES	DATE
DRN. J.CARTER	11-11-77
CHK'D. W. Smith	12-NOV-77
ENG.	
PROJ.ENG.	
PROD.	

ETCH REV. D-PL
P.C. DESIGN DATA BASE REV. D

digital

TITLE MSVII-C MOS MEMORY, LSI

SCALE 2/1 SHT. 3 OF 9

SIZE	CODE	NUMBER	REV
D	UA	M7955-0-0	D

NEXT HIGHER ASSY. B-DD-M7955-0

M7955-0-0 D UA

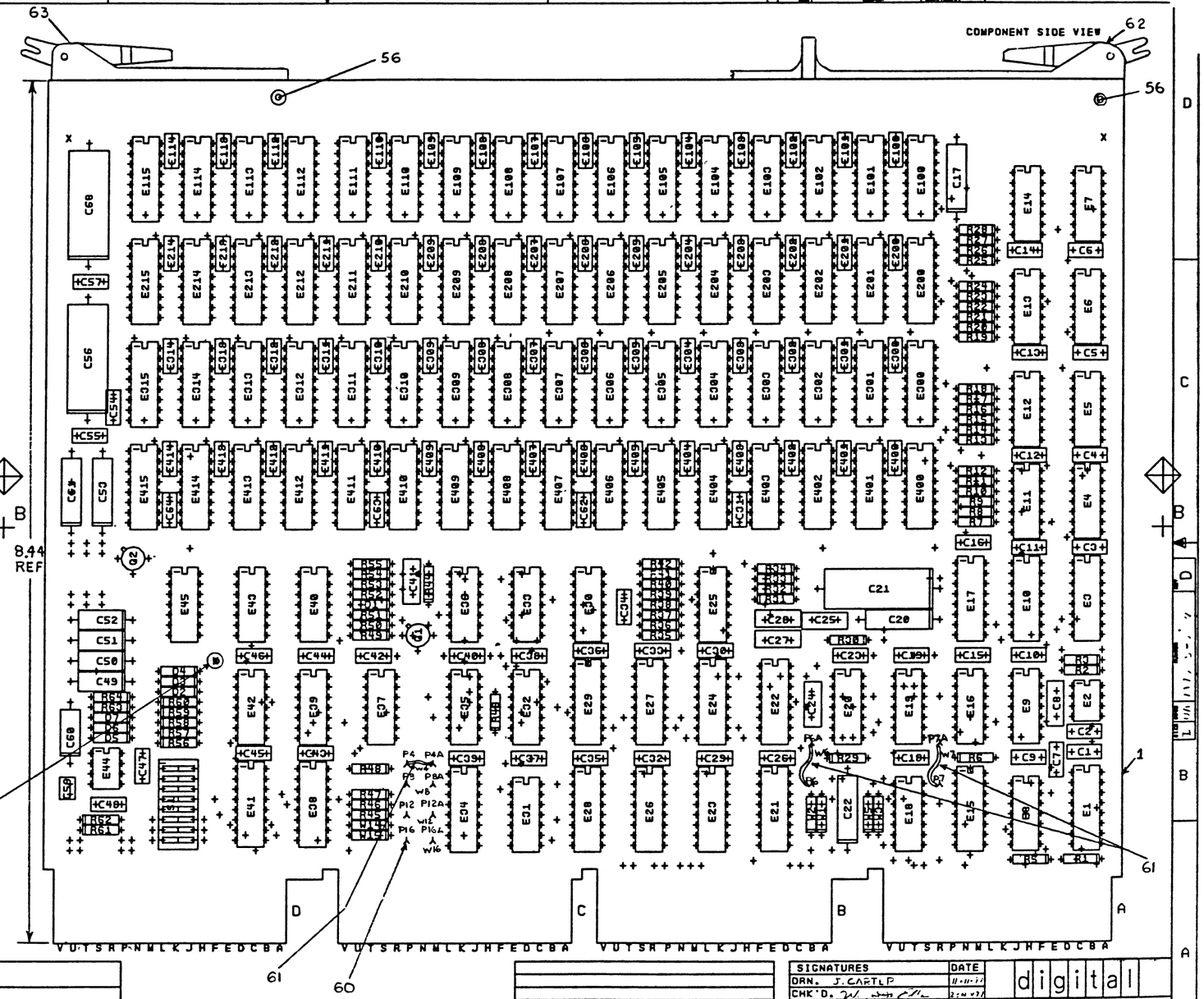
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MODULE VARIATION: M7955-AA

NOTE: 1. FOR M7955-AC, SEE SH. 2

2. FOR M7955-AB, SEE SH. 3

3. FOR M7955-AA, SEE SH. 4



NOTES: 1. M7955-AA - M7955-YA & YE

CHK	CHANGE NO	REV
	M7955-0-YA	C

FOR PL, SEE B PL-M7955-0-0

ETCH REV. D-Pc
P.C. DESIGN DATA BASE REV. I

SIGNATURES	DATE
DRN. J.CARTLP	11-11-77
CHK'D.	12-14-77
ENG.	
PROJ.ENG.	
PROD.	
SCALE 2/1	
SHT. 4 OF 9	
NEXT HIGHER ASSY.	

digital

TITLE MSVII-C MOS MEMORY, LSI

SIZE	CODE	NUMBER	REV
D	UA	M7955-0-0	D

1 MS#

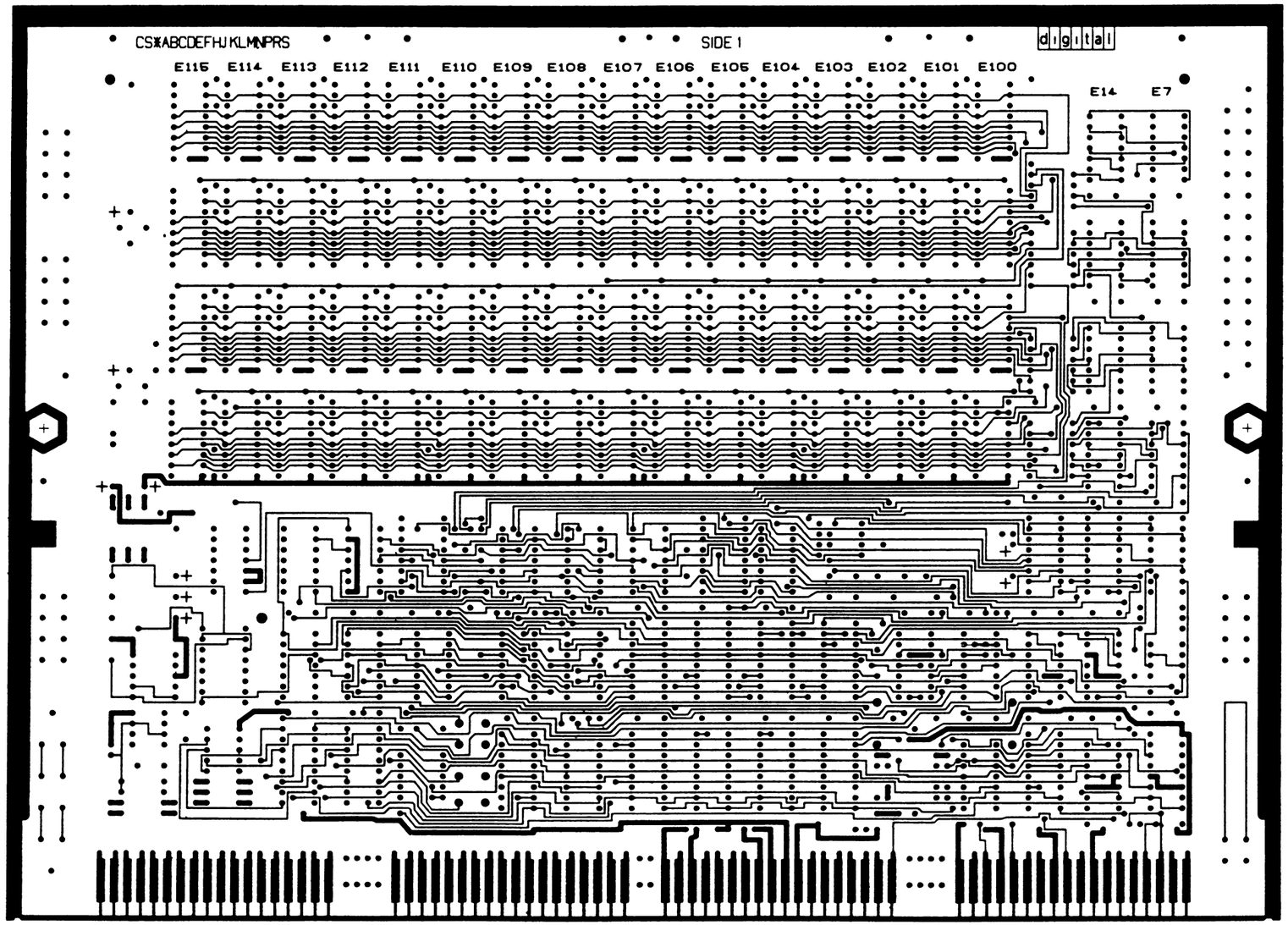
8 7 6 5 4 3 2 1

D-D-5561W DUA D

6012203D-P2
M7955

L1

LAYER 1



D UA M7955-0-0 D

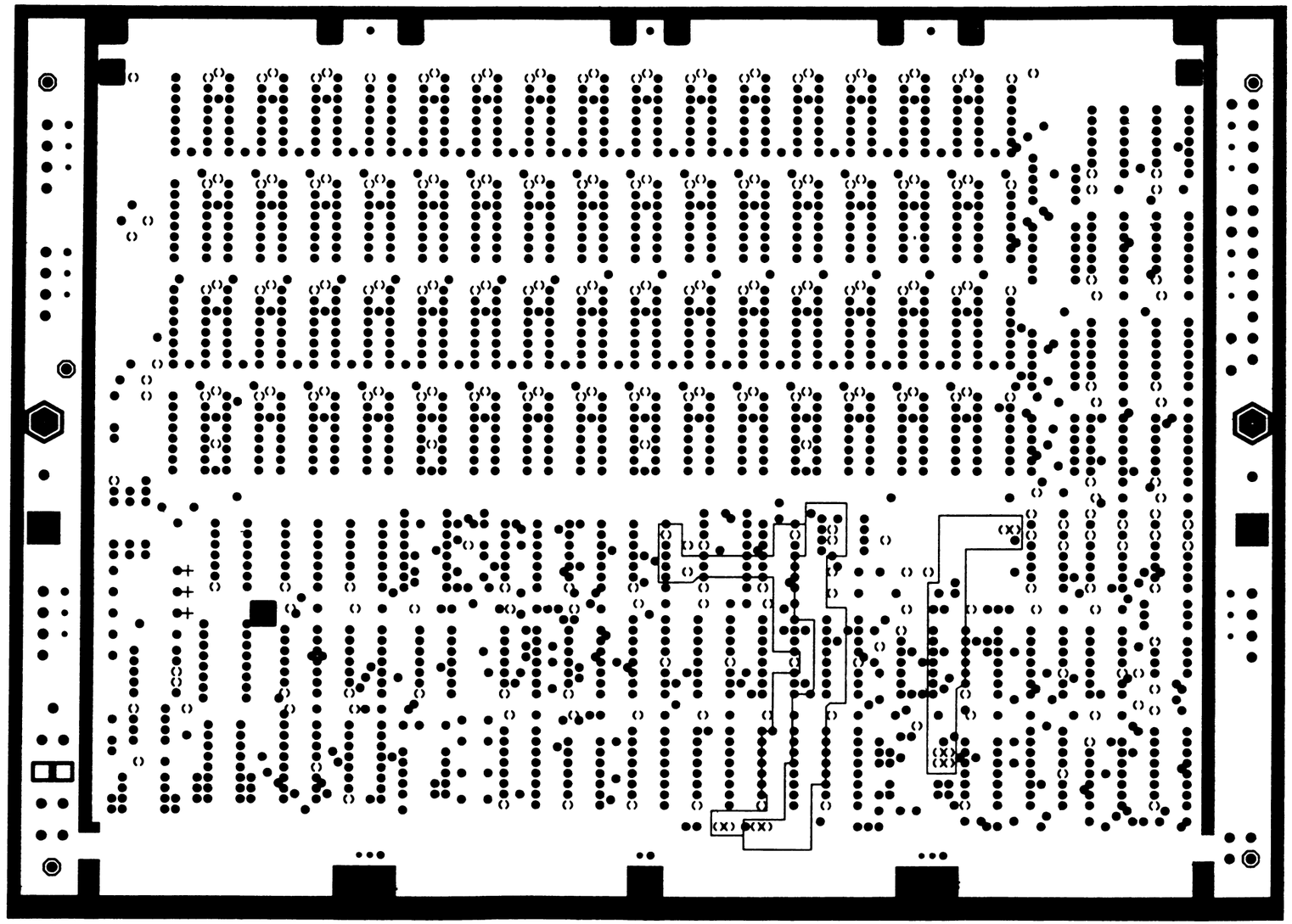
TITLE	SIZE	CODE	NUMBER	REV
MSV11-C MOS MEMORY, LSI	D	UA	M7955-0-0	D
SCALE 2/1 SHEET 5 OF 9	DIST			

8 7 6 5 4 3 2 1

6012203D-P2
M7955

L2

LAYER 2



TITLE	SIZE	CODE	NUMBER	REV
MSVII-C MOS MEMORY, LSI	D	UA	M7955-0-0	D
SCALE 2/1 SHEET 6 OF 9	DIST			

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LAYER 3

LC

TITLE	SIZE	CODE	NUMBER	REV
MSVII-C MOS MEMORY, LSI	D	UA	M7955-0-0	D
SCALE 2/1 SHEET 7 OF 9	DIST			

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LAYER [redacted]

L4

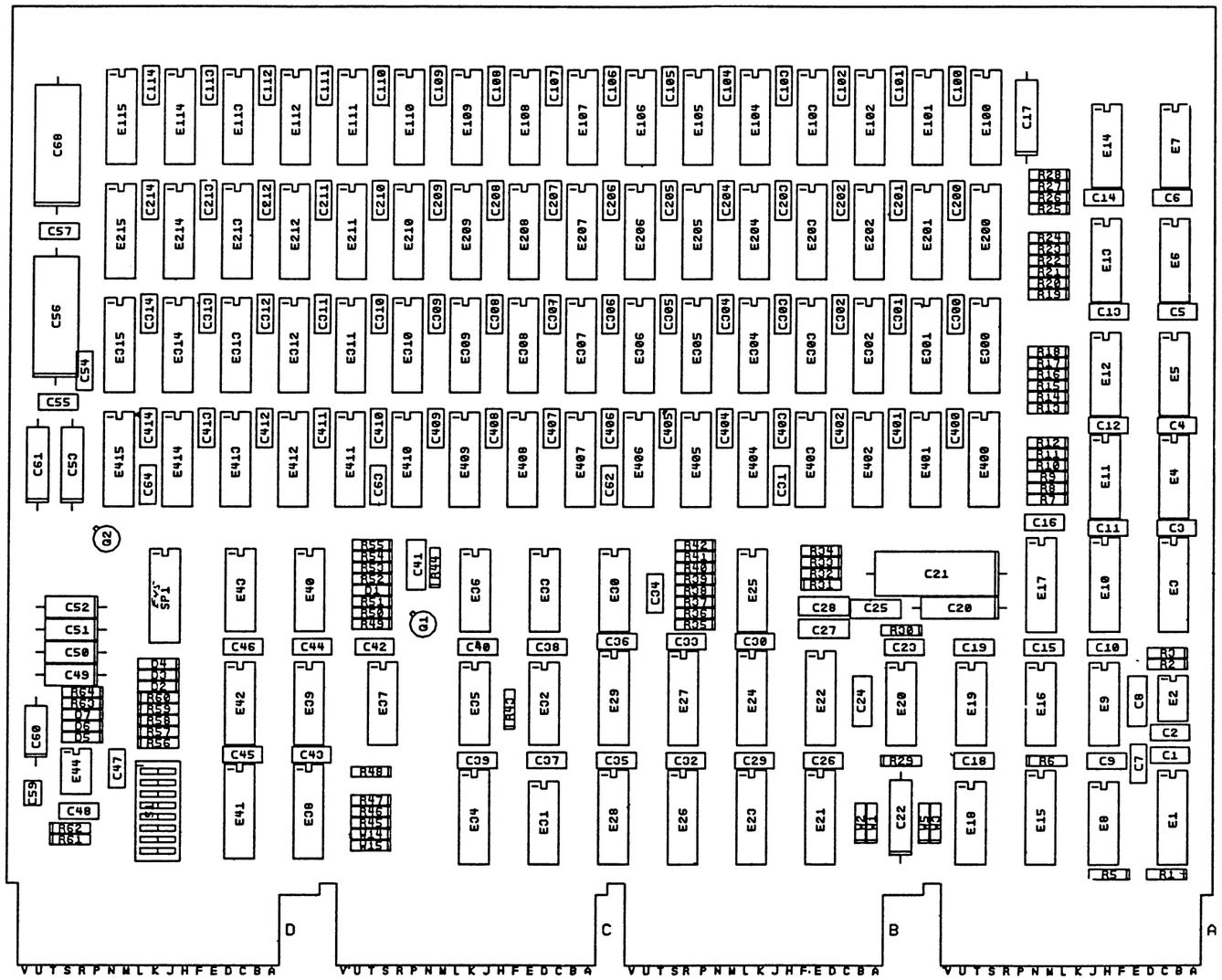
M7955-0-0

M7955 6012203D-P2 SIDE 2 MSV11-C L8I MOS MEMORY

REVISIONS		
CHK	[redacted]	REV.

TITLE: MSVII-C MOS MEMORY, LSI							SIZE: D	CODE: UA	NUMBER: M7955-0-0 REV: D
SCALE: 2/1	SHEET: 8 OF 9						DIST		

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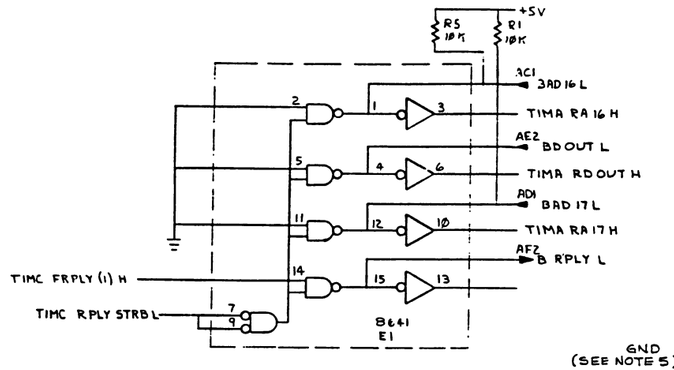
REFERENCE DOCUMENT

REVISIONS		
CHK	CHANGE NO.	REV

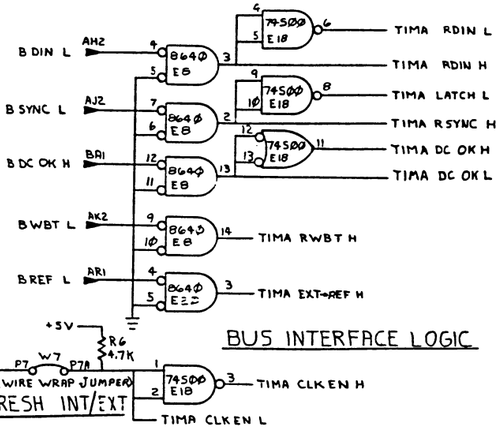
TITLE	SIZE	CODE	NUMBER	REV
MSVII-C MOS MEMORY LSI	D	UA	M7955-Ø-Ø	D
SCALE 2/1 SHEET 9 OF 9	DIST			

DUA M7955-Ø-Ø D

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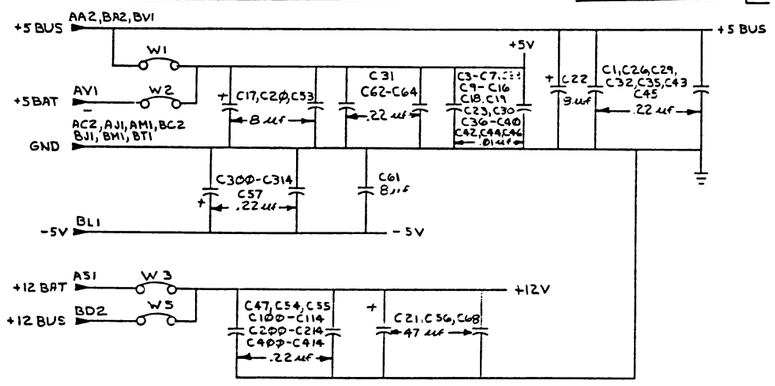
BUS INTERFACE LOGIC

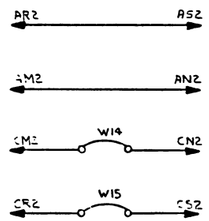


BUS INTERFACE LOGIC



SPARES





BUS GRANT CONTINUITY JUMPERS

W6	W7	REFRESH OPTIONS
IN	IN	INTERNAL REFRESH WITH NO B R'PLY
IN	OUT	EXTERNAL REFRESH WITH NO B R'PLY
OUT	IN	ILLEGAL
OUT	OUT	EXTERNAL REFRESH WITH B R'PLY

REFRESH SELECTION

STARTING ADDRESS	SWITCH S1 SETTINGS -1	-2	-3	-4	-5	
0	1	1	1	1	1	
4K	0	1	1	1	1	
8K	1	0	1	1	1	
12K	0	0	1	1	1	
16K	1	1	0	1	1	
20K	0	1	0	1	1	
24K	1	0	0	1	1	
28K	0	0	0	1	1	
32K	1	1	1	0	1	
36K	0	1	1	0	1	
40K	1	0	1	0	1	
44K	0	0	1	0	1	
48K	1	1	0	0	1	
52K	0	1	0	0	1	
56K	1	0	0	0	1	
60K	0	0	0	0	1	
64K	1	1	1	1	0	
68K	0	1	1	1	0	
72K	1	0	1	1	0	
76K	0	0	1	1	0	
80K	1	1	0	1	0	
84K	0	1	0	1	0	
88K	1	0	0	1	0	
92K	0	0	0	1	0	
96K	1	1	1	0	0	
100K	0	1	1	0	0	
104K	1	0	1	0	0	
108K	0	0	1	0	0	
112K	1	1	0	0	0	
116K	0	1	0	0	0	EXCEPT M7955-AD
120K	1	0	0	0	0	EXCEPT M7955-AC & AD
124K	0	0	0	0	0	EXCEPT M7955-AB, AC, & AD

OVER LAPPING IS NOT ALLOWED IN ANY PERIPHERAL PAGE

1 = ON
0 = OFF

STARTING ADDRESS SELECTION

M7955 VARIATIONS

JUMPERS	-AA	-AB	-AC	-AD
W4	1	1	1	1
W8	0	1	1	1
W12	0	0	1	1
W16	0	0	0	1

ALL JUMPERS NOTED AS 0 MUST NOT BE INSTALLED

IC PIN LOCATIONS

I.C. TYPE	GND	+5	+12
555 @ E2	1	8	
555 @ E44	1		8
7493	10	5	
7483A	12	5	
74LS75	12	5	
8640	1	8	
OTHER 16 PIN I.C.'S	8	16	
OTHER 14 PIN I.C.'S	7	14	

NOTES:

1. OPTION DESIGNATION:
 M7955-AA = M7955-YA OR M7955-YE
 M7955-AB = M7955-YB OR M7955-YF
 M7955-AC = M7955-YC OR M7955-YH
 M7955-AD = M7955-YD OR M7955-YJ
2. ALL 8641 BUS REC/DR PLUS 7483A ADDER AND 74S138 DECODER ARE POWERED BY +5 BUS. ALL OTHER CIRCUITS GO TO +5V AS SELECTED BY W1 & W2.
3. W1, W2, W3, W5, W14, W15 ARE MACHINE INSERTABLE JUMPERS. W4, W6, W7, W8, W12, W16 ARE WIRE WRAP JUMPERS.
4. ALL BDAL -XX CONNECTIONS ARE BI-DIRECTIONAL LINES
5. DURING MANUFACTURING TEST, GROUND MAY BE REMOVED

NOT USED REF DES

C100-C114, C200-C214, W3, W12, W16
C100-C114, C200-C214, W12, W16
C100-C114, W16

REVISIONS	CHK	CHANGE NO.	REV.
	MC	M7955-0000414	C
		J. CARTER 10-28-77	
		J. STEGEMAN,	
	JM	M7955-00002	D
		STEVE WILLIAMSON	
		R. DURANT	

ETCH REV	D-P2
DRN.	
CHK'D	11/18/76
ENG.	
PROJ. ENG.	
PROD.	
NEXT HIGHER ASSY.	
B-DD-M7955-D	
SCALE	
SHEET 1 OF 8	

FIRST USED ON M5VII-C

digital

TITLE M5VII-C MOS MEMORY, LSI (TIMA)

SIZE	CODE	NUMBER	REV.
D	CS	M7955-0-1	D

DIST.

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ROW SELECTION

TIMC LA 17 L
TIMC LA 16 L
TIMC LA 15 L
TIMC LA 14 L
TIMB CIN H
TIMC LAT REF L
74S10 E19
74S83A E41
74S138 E39
P4 W4 P4A
P8 W8 P8A
P12 W12 P12A
P16 W16 P16A
(WIREWRAP JUMPERS)
TIMB ROW 0 L
TIMB ROW 1 L
TIMB ROW 2 L
TIMB ROW 3 L
+5V
R48 4.7K
R47 4.7K
R46 4.7K
R45 4.7K

FAILING ROW	MEMORY SIZE			
	M7955-AA(4K)	M7955-AB(8K)	M7955-AC(12K)	M7955-AD(16K)
ROW 0	NO SWAPPING POSSIBLE	P4 TO P8A	REMOVE W4 ADD JUMPER P4 TO P12A	REMOVE W4 ADD JUMPER P4 TO P16A
ROW 1		* REMOVE W8	REMOVE W8 ADD JUMPER P8 TO P12A	REMOVE W8 ADD JUMPER P8 TO P16A
ROW 2			* REMOVE W12	REMOVE W12 ADD JUMPER P12 TO P16A
ROW 3				* REMOVE W16

1. DETERMINE MEMORY SIZE & REMOVE UPPER 4K ROW JUMPER. (INDICATED BY *)
2. LOCATE FAILING ROW, REMOVE SPECIFIED ROW JUMPER, ADD SWAPPING JUMPER IF FAILING ROW IS UPPER ADDRESS SPACE ROW, THERE IS NO SWAPPING JUMPER
3. THIS RECONFIGURED MEMORY BLOCK STILL HAS THE SAME STARTING ADDRESS AS BEFORE IT OCCUPIES 4K LESS ADDRESS SPACE THAN BEFORE RECONFIGURE STARTING ADDPESSES OF MEMORIES ABOVE THIS ONE IF NECESSARY SO THERE WILL BE CONTICUOUS ADDRESS SPACE.

ROW SWAPPING MATRIX

VALID DEVICE SELECTION ADDRESS SPACE

S1
-1 -2 -3 -4 -5
R56 4.7K
R57 4.7K
R58 4.7K
R59 4.7K
R60 4.7K
+5V

ADDRESS SPACE SIZE & MAPPING

TIMC LAT SXTREF L
74S133 E34
TIMA RSYNC H
74S00 E42
TIMB BSEL H
TIMB ENDOUT H

MEMORY CYCLE TYPE

TIMC GO REF H
TIMC F RPLY(I) L
TIMC LOCKOUT L
TIMB BSEL H
TIMA RSYNC H
TIMC NO DIN L
TIMA RDOUT H
TIMB ENDOUT H
TIMC FRPLY(I) L
TIMC LOCKOUT AL
74S10 E37
74S20 E31
74S03 E33
TIMB GO TIM H

REFRESH SYNCHRONIZATION

TIMC GO REF L
+5V
R53 1B
R52 220
Q1 2N3904
D1 6T2
TIMB START L
R51 330
R50 1K
R44 1B
R49 1K
C41 100PF
-5V
TIMB OFF L
74S74 E36
TIMB TRAS (I) H
TIMB TRAS (I) L
R31 1B
C28 220 PF
C27 220PF
TIMD -5V
C34 .22 uF

TIMING CHAIN GENERATOR

TIMB PULL 2 H
R40 75
R39 226
R38 316
R37 1K
C33 .01uF
R36 31.6
R35 121
R42 1K
R41 196
R32 121K
R33 14.7K
R34 6.81K
TIMB PULL 2H
TIMB OFF L
TIMING MARGIN TEST POINT
*TIMD-5V
75107 E30
75107 E25
TIMB SRPLY H
TIMB CAS H
TIMB MUX H

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
M5V11-C MOS MEMORY, LSI (TIMB)	D	CS	M7955-0-1	D
SCALE	SHEET 2 OF 8	DIST		

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TIMD DI_ØØ H
TIMD DI Ø1 H
TIMD DI Ø2 H
TIMD DI Ø3 H
TIMA LATCH L
74LS75 E22
TIMC LA ØØ H
TIMC LA Ø1 H
TIMC LA Ø2 H
TIMC LA Ø3 H

TIMD DI Ø4 H
TIMD DI Ø5 H
TIMD DI Ø6 H
TIMD DI Ø7 H
74LS75 E24
TIMC LA Ø4 H
TIMC LA Ø5 H
TIMC LA Ø6 H
TIMC LA Ø7 H

IMD DI Ø8 H
TIMD DI Ø9 H
TIMD DI 1Ø H
TIMD DI 11 H
74LS75 E27
TIMC LA Ø8 H
TIMC LA Ø9 H
TIMC LA 1Ø H
TIMC LA 11 H

TIMD DI 12 H
TIMD DI 13 H
TIMD DI 14 H
TIMD DI 15 H
74LS75 E29
TIMC LA 12H
TIMC LA 13L
TIMC LA 14L
TIMC LA 15L

TIMA RA 16 H
TIMA RA 17 H
TIMA RWBT H
TIMA EXT REF H
74LS75 E15
TIMC LA 16 L
TIMC LA 17 L
TIMC LWAT H
TIMC LAT REF L
TIMC LAT EXT REF I

ADDRESS+ CONTROL LATCHES

TIMD RA Ø H
TIMC LA Ø7 H
TIMC LA Ø1 H
TIMD RA 1 H
TIMC LA Ø8 H
TIMC LA Ø2 H
74S153 E3
TIMC MA Ø H
TIMC MA 1 H

TIMD RA 2 H
TIMC LA Ø9 H
TIMC LA Ø3 H
TIMD RA 3 H
TIMC LA 1Ø H
TIMC LA Ø4 H
74S153 E1Ø
TIMC MA 2 H
TIMC MA 3 H

TIMD RA 4 H
TIMC LA 11 H
TIMC LA Ø5 H
TIMD RA 5 H
TIMC LA 12 H
TIMC LA Ø6 H
74LS153 E17
TIMC MA 4 H
TIMC MA 5 H

TIMC INTREF(1) H
TIMB MUX H

ADDRESS MUX'S

TIMB PULL 2H
TIMB TRAS(1) L
74S74 E36
TIMC RESET L
74S03 E33
+5V
R55 2.61K
R54 14.7K
C24 220 PF
8640 E20
TIMB OFF L
TIMB TRAS (1) L
74S10 E19
TIMC LOCKOUT L
TIMA DC OK L
8640 E20
TIMC LOCKOUT AL

BUS CYCLE HOLD OFF

TIMC INTREF (1) H
TIMC LAT EXT REF H
74S02 E39
TIMC REF L
P6 P6A W6 (WIRE WRAP JUMPER)
+5V
R29 4.7 K
74S10 E37
TIMB SRPLY H
8640 E20
R30 10
C25 100 PF
74S74 E40
TIMC FRPLY (1) H
TIMC FRPLY (1) L
TIMA RDOUT H
TIMA RDIN H
74S02 E43
TIMC RPLY STRB L
TIMA RSYNC H

REFRESH RPLY SELECT

TIMC PULL 1H
R43 1K
TIMA CLK EN H
74S74 E32
TIMC GO REF H
74S00 E35
TIMC GO REF L
TIMB GOTIM H
74S74 E40
TIMB OFF L
TIMC INTREF(1) H
74S00 E35
TIMB SRPLY H
TIMD REF CLK H
TIMA CLK EN L
74S00 E35
TIMC LAT EXT REF L
TIMB TRAS(1) L
74S02 E39
TIMC PULL 1 H
TIMC LWBT H
74S02 E43
TIMC NODIN L
74S74 E32
TIMA RSYNC H

REVISIONS

CHK	CHANGE NO	REV

TITLE		SIZE	CODE	NUMBER	REV.
MSV11-C MOS MEMORY, LSI (TIMC)		D	CS	M7955-Ø-1	D
SCALE	SHEET 3 OF 8	DIST			

DRAWING M7955-Ø-1 D

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MTX 3 DOUT Ø2 H
MTX 3 DOUT Ø3 H
MTX 3 DOUT Ø1 H
MTX 3 DOUT ØØ H
TIMC FRFLY (1) L
TIMA RDIN L
BE2 BDAL 02 L
TIMD DI Ø2 H
BF2 BDAL Ø3 L
TIMD DI Ø3 H
AV2 BDAL Ø1 L
TIMD DI Ø1 H
AU2 BDAL ØØ L
TIMD DI ØØ H
8641 E21

MTX 2 DOUT Ø6 H
MTX 2 DOUT Ø7 H
MTX 2 DOUT Ø5 H
MTX 2 DOUT Ø4 H
BK2 BDAL Ø6 L
TIMD DI Ø6 H
BL2 BDAL Ø7 L
TIMD DI Ø7 H
BJ2 BDAL Ø5 L
TIMD DI Ø5 H
BH2 BDAL Ø4 L
TIMD DI Ø4 H
8641 E23

MTX 1 DOUT 1Ø H
MTX 1 DOUT 11 H
MTX 1 DOUT Ø9 H
MTX 1 DOUT Ø8 H
BP2 BDAL 1Ø L
TIMD DI 1Ø H
BR2 BDAL 11 L
TIMD DI 11 H
BN2 BDAL Ø9 L
TIMD DI Ø9 H
BM2 BDAL Ø8 L
TIMD DI Ø8 H
8641 E26

MTX Ø DOUT 14 H
MTX Ø DØUT 15 H
MIX Ø DOUT 13 H
MTX Ø DOUT 12 H
BU2 BDAL 14 L
TIMD DI 14 H
BV2 BDAL 15 L
TIMD DI 15 H
BT2 BDAL 13 L
TIMD DI 13 H
BS2 BDAL 12 L
TIMD DI 12 H
8641 E28

B DAL TRANSCEIVERS

TIMB ROW 3 L
TIMB ROW 2 L
TIMB ROW 1 L
TIMB ROW Ø L
TIMC REF L
TIMB TRAS(1) H
74S00 E4
74S37 E6
R26 18 TIMD RAS D L
R25 18 TIMD RAS C L
R21 18 TIMD RAS B L
R20 18 TIMC RAS A L

ROW ADDRESS STROBE DRIVERS

REFRESH OSC

+5V
R3 100K
R2 12.1K
C2 .01 µF
C8 220 PF
555 E2 VTH DCG CTL
E45 7414
TIMA CLK EN H
+12V
R62 2.61K
R61 1.21K
C48 .01 µF
555 E44
C59 5600 PF
Q2 G534
C52 2.2 µF
D2 DG72
C50 2.2 µF
D4 DG72
D3 DG72
C51 2.2 µF
D5 DG72
R63 120
R64 120
TIMD-5V BK1
C60 2.2 µF
D6 DG72
C49 2.2 µF
D7 IN751A
TIMD REF CLK H

+12 TO -5V CONVERSION

7493 E16 CLR CLKØ CLKBC R3(1) R2(1) R1(1) RØ(1)
TIMD RA 5 H
TIMD RA 4 H
7493 E9
TIMD RA 3 H
TIMD RA 2 H
TIMD RA 1 H
TIMD RA Ø H

TIMC MA Ø H
TIMC MA 1 H
TIMC MA 2 H
TIMC MA 3 H
TIMC MA 4 H
TIMC MA 5 H
74128 E5
74128 E12
74128 E13
R17 18 TIMD AØØ A L
R15 18 TIMD AØØ B L
R14 18 TIMD AØ1 A L
R18 18 TIMD AØ1 B L
R16 18 TIMD AØ2 A L
R13 18 TIMD AØ2 B L
R12 18 TIMD AØ3 A L
R11 18 TIMD AØ3 B L
R22 18 TIMD AØ4 A L
R24 18 TIMD AØ4 B L
R19 18 TIMD AØ5 A L
R23 18 TIMD AØ5 B L

MOSRAM ADDRESS DRIVERS

TIMB TRAS(1) H
TIMB CAS H
74S37 E11
R8 18 TIMD CAS Ø L
R7 18 TIMD CAS 1 L

COLUMN ADDRESS STROBE DRIVERS

TIMC REF L
TIMB MUX H
R10 18 TIMD CS Ø L
R9 18 TIMD CS 1 L

CHIP SELECT DRIVERS

TIMA DC OK H
TIMC REF L
74S00 E7
TIMC LA ØØ H
TIMA RWBT H
TIMC LA ØØ L
74S140 E14
TIMB MUX H
TIMA RDOUT H
R27 18 TIMD WB Ø L
R28 18 TIMD WB 1 L

WRITE BYTE CONTROL DRIVERS

REVISIONS		
CHK	CHANGE NO	REV

TITLE MSV11-C MOS MEMORY, LSI (TIMD)
SIZE D | CODE CS | NUMBER M7955-Ø-1 | REV. D
SCALE — | SHEET 4 OF 8 | DIST

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TIMD AΦ5 BL
TIMD AΦ4 BL
TIMD AΦ3 BL
TIMD AΦ2 BL
TIMD AΦ1 BL
TIMD AΦΦ BL

TIMD DI 15 H
TIMD CSΦ L
TIMD CASΦ L
TIMD WB 1 L
TIMD RASD L

TIMD RASC L
TIMD AΦ5 AL
TIMD AΦ4 AL
TIMD AΦ3 AL
TIMD AΦ2 AL
TIMD AΦ1 AL
TIMD AΦΦ AL

TIMD CS1 L
TIMD CAS1 L
TIMD RASB L

TIMD RASA L

4Φ96 E115 — TIMD DI 14 H
4Φ96 E114 — TIMD DI 13 H
4Φ96 E113 — TIMD DI 12 H
4Φ96 E112

4Φ96 E215
4Φ96 E214
4Φ96 E213
4Φ96 E212

4Φ96 E315
4Φ96 E314
4Φ96 E313
4Φ96 E312

4Φ96 E415 — MTXΦ 15 H
4Φ96 E414 — MTXΦ 14 H
4Φ96 E413 — MTXΦ 13 H
4Φ96 E412 — MTXΦ 12 H

4Φ96 EXX
AΦ5 AΦ4 AΦ3 AΦ2 AΦ1 AΦΦ DIN
DOUT
CS CAS WR RAS

GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

(ARRAY) DATA BITS(15-12) MTXΦ

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
MSVII-C MOS MEMORY, LSI	D	CS	M7955-Ø-1	D
SCALE —	SHEET 5 OF 8	DIST		

DCS M7955-Ø-1 REV D

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TIMD A$5BL
TIMD A$4BL
TIMD A$3BL
TIMD A$2BL
TIMD A$1BL
TIMD A$$BL

TIMD DI 11 H

TIMD CS$L
TIMD CAS $L
TIMD WB 1L
TIMD RAS DL

TIMD RAS CL
TIMD A$5AL
TIMD A$4AL
TIMD A$3AL
TIMD A$2AL
TIMD A$1AL
TIMD A$$AL

TIMD CS 1L
TIMD CAS 1L
TIMD RAS BL

TIMD RAS AL

4$96 E111 — TIMD DI $8H
4$96 E11$ — TIMD DI $9H
4$96 E1$9 — TIMD DI $8H
4$96 E1$8
4$96 E211
4$96 E21$
4$96 E2$9
4$96 E2$8
4$96 E311
4$96 E31$
4$96 E3$9
4$96 E3$8
4$96 E411 — MTX1 11H
4$96 E41$ — MTX1 1$H
4$96 E4$9 — MTX$ $9H
4$96 E4$8 — MTX1 $8H

4$96 EXX
A$5 A$4 A$3 A$2 A$1 A$$ DIN
DOUT
CS CAS WR RAS

END PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

(ARRAY) DATA BITS (11-8) MTX1

REVISIONS		
CHK	CHANGE NO	REV

TITLE: MSVII-C MOS MEMORY, LSI			SIZE D	CODE CS	NUMBER M7955-$-1	REV. D
SCALE	SHEET 6 OF 8		DIST			

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TIMD AΦ5 BL
TIMD AΦ4 BL
TIMD AΦ3 BL
TIMD AΦ2 BL
TIMD AΦ1 BL
TIMD AΦΦ BL

TIMD DIΦ7H
TIMD CSΦ L
TMD CASΦL
TMD WBΦL
TIMD RAS DL

TMD RAS C L
TIMD AΦ5 AL
TIMD AΦ4 AL
TIMD AΦ3 AL
TIMD AΦ2 AL
TIMD AΦ1 AL
TIMD AΦΦ AL

TIMDCS 1L
TIMD CAS 1 L
TIMD RAS BL

TIMD RAS P L

4Φ9C E1Φ7 — TIMDDIΦ6H
4Φ9C E1Φ6 — TIMDDIΦ5H
4Φ9C E1Φ5 — TIMDDIΦ4H
4Φ9C E1Φ4

4Φ9C E2Φ7
4Φ9C E2Φ6
4Φ9C E2Φ5
4Φ9C E2Φ4

4Φ9C E3Φ7
4Φ9C E3Φ6
4Φ9C E3Φ5
4Φ9C E3Φ4

4Φ9C E4Φ7 — MTX2 Φ7 H
4Φ9C E4Φ6 — MTX2 Φ6 H
4Φ9C E4Φ5 — MTX2 Φ5 H
4Φ9C E4Φ4 — MTX2 Φ4 H

4Φ9C EXX
AΦ5 AΦ4 AΦ3 AΦ2 AΦ1 AΦΦ DIN CS CAS WE RAS → DOUT

GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

(ARRAY) DATA BITS (7- 4) MTX2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
MSVII-C MOS MEMORY, LSI	D	CS	M7955-Ø-1	.D
SCALE ~	SHEET 7 OF F	DIST		

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TIMD AØ5 BL
TIMD AØ4 BL
TIMD AØ3 BL
TIMD AØ2 BL
TIMD AØ1 BL
TIMD AØØ BL

TIMD DIØ3H

TIMD CSØL
TIMD CASØL
TIMD WBØL
TIMD EASDL

TMD EASCL
TIMD AØ5AL
TIMD AØ4AL
TIMD AØ3AL
TIMD AØ2AL
TIMD AØ1AL
TIMD AØØAL

TIMD CS1 L
TIMD CAS 1L
TIMD RAS BL

TMD EASAL

4Ø96 EXX: AØ5, AØ4, AØ3, AØ2, AØ1, AØØ, DIN, CS CAS WE RAS, DOUT

GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

4Ø96 E1Ø3 — TIMD DIØ3H
4Ø96 E1Ø2 — TIMDDIØ1H
4Ø96 E1Ø1 — TIMDDIØØH
4Ø96 E1ØØ
4Ø96 E2Ø3
4Ø96 E2Ø2
4Ø96 E2Ø1
4Ø96 E2ØØ
4Ø96 E3Ø3
4Ø96 E3Ø2
4Ø96 E3Ø1
4Ø96 E3ØØ
4Ø96 E4Ø3 — MTX3 Ø3 H
4Ø96 E4Ø2 — MTX3 Ø2H
4Ø96 E4Ø1 — MTX3 Ø1 H
4Ø96 E4ØØ — MTX3 ØØ H

(ARRAY) DATA BITS (Ø3-ØØ) MTX3

REVISIONS		
CHK	CHANGE NO.	REV

TITLE: MSV11-C MOS MEMORY, LSI	SIZE: D	CODE: CS	NUMBER: M7955-Ø-1	REV: D
SCALE: ~	SHEET 2 OF 2	DIST		

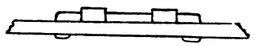
M7955-Ø-1 D CS

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MODULE VARIATIONS AA&CA

1.

2. W2 THRU W5 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING:



3. R-PACKS SHOULD BE INSTALLED SO THAT LEADS DO NOT INTERFERE WITH OTHER COMPONENTS.

4. ⊗ WIRE WRAP PIN.

5.

MEMORY TYPE	JUMPER CONFIG.	VARIATION
NON-PARITY	5-7	AA, CA

6.

MEMORY SIZE	JUMPER CONFIG.		VARIATION
4 K	17-15	12-14	AA
16 K	16-15	13-14	CA

7. OPTIONAL JUMPER 1-2 WILL ALLOW USER TO EXTEND USABLE MEMORY SPACE FROM 28K TO 30K NORMAL JUMPER IS 1-3.

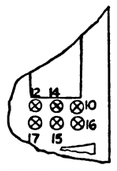
8.

JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	CUT	IN
W3	OUT	IN
W4	IN	OUT
W5	IN	OUT

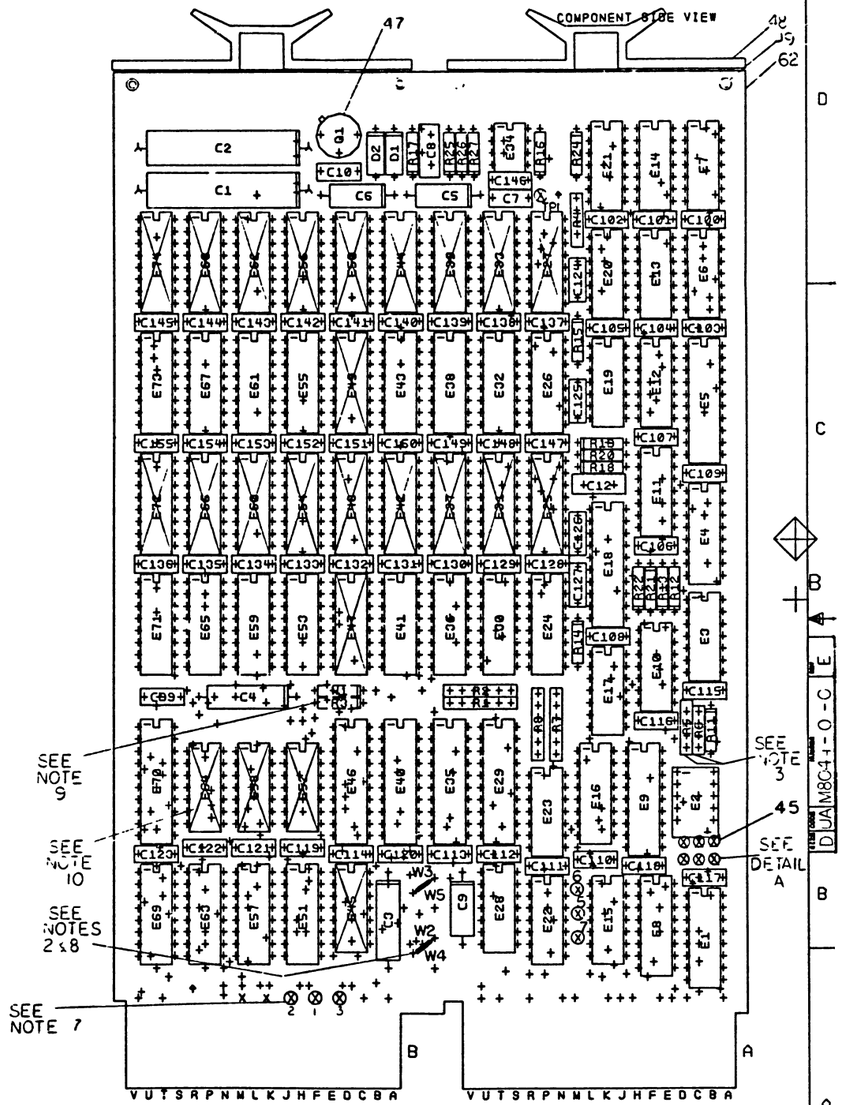
9.

MEMORY SIZE	W1	R3	VARIATION
4K	IN	OUT	AA
16K	OUT	IN	CA

10. THE FOLLOWING IC'S ARE NOT INSTALLED IN AA & CA VARIATIONS: E25, 27, 31, 33, 37, 39, 42, 44, 45, 47, 48, 49, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 72 & 74.



DETAIL A



NOTES:

CHG	CHANGE NO	REV
E2	M8044-0001	C
REVISED & REDRAWN		
R. GIVEN		
E2	M8044-M002	D
R. GIVEN		
M8044-M003		E
R. GIVEN		

ETCH REV. D-P
P.C. DESIGN DATA BASE REV. DL & DM

SIGNATURES	DATE
DRN.	
CHK.	
ENG.	
PROJ. ENG.	
PROD.	

digital

TITLE: 32K 16BIT MOS MEMORY

SCALE 2/1 | SIZE D | CODE UA | NUMBER M8044-0-0 | REV E | SHT. OF

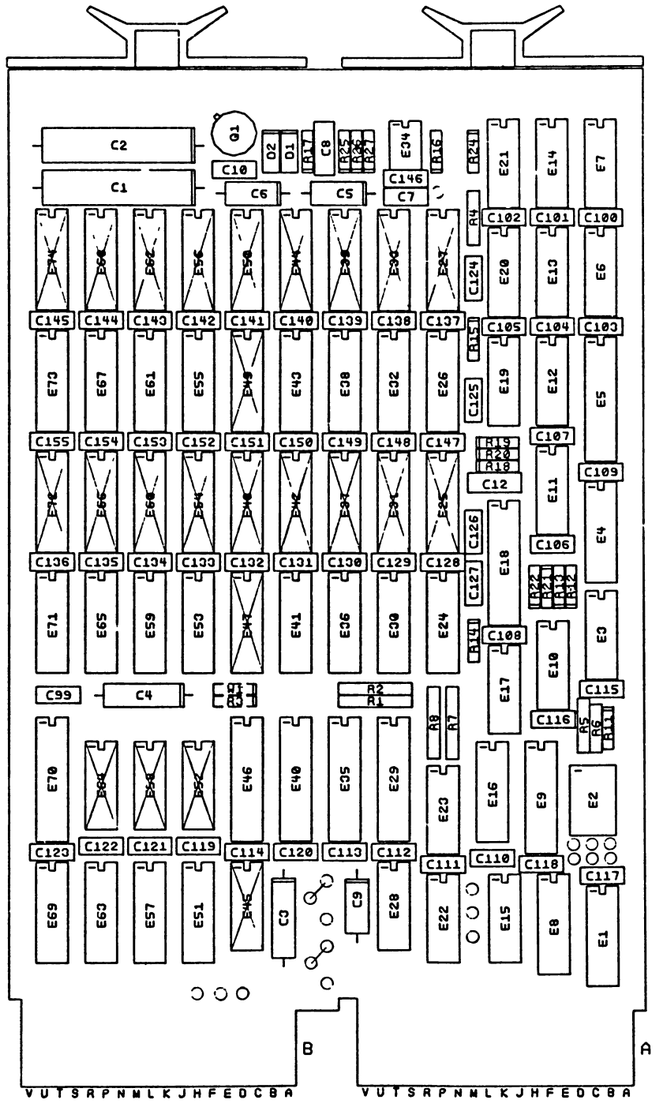
NEXT HIGHER ASSY. B-DD-M8045-0

DUAM8044-0-0 E

MS# 261966

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MODULE VARIATIONS AA & CA



NOTES:

CHK	CHANGE NO	REV

SIGNATURES	DATE
DRN.	
CHK'D.	3-12-
ENG.	
PROJ. ENG.	
PROD.	
SCALE 2/1	
SHT. 2 OF 6	
NEXT HIGHER ASSY.	

digital

TITLE
32K 16 BIT MOS MEMORY

SIZE	CODE	NUMBER	REV
D	UA	M8044-0-0	E

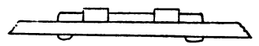
1 MS#

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MODULE VARIATIONS BA, DA & EA

1.

2. W2 THRU W5 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING:



3. R PACKS SHOULD BE INSTALLED SO THAT LEADS DO NOT INTERFERE WITH OTHER COMPONENTS.

4. ⊗ WIRE WRAP PIN.

5.

MEMORY TYPE	JUMPER CONFIG	VARIATION
NON-PARITY	5-7	BA, DA

6.

MEMORY SIZE	JUMPER CONFIG		VARIATION
8 K	14-15	12-13	BA
32 K	15-16	10-14	DA
24 K	16-15	10-14	EA

7. OPTIONAL JUMPER 1-2 WILL ALLOW USER TO EXTEND USABLE MEMORY SPACE FROM 28K TO 30K. NORMAL JUMPER IS 1-3.

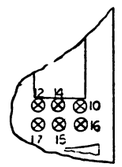
8.

JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	CUT	IN
W3	OUT	IN
W4	IN	CUT
W5	IN	OUT

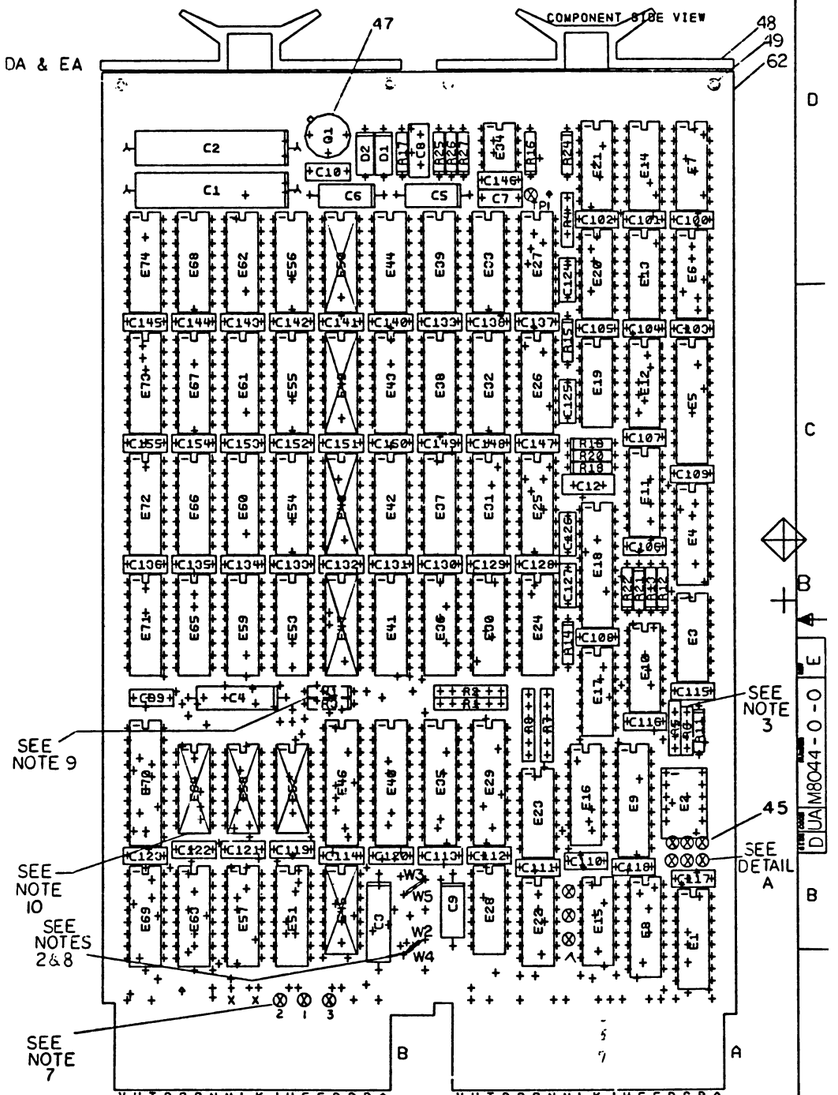
9.

MEMORY SIZE	W1	R3	VARIATION
8K	IN	OUT	BA
32K	OUT	IN	DA
24K	OUT	IN	EA

10. THE FOLLOWING IC'S ARE NOT INSTALLED IN BA & DA VARIATIONS: E45, 47, 48, 49, 50, 52, 58 & 64.



DETAIL A



NOTES:

CHG	CHANGE NO	REV

ETCH REV. D-P
P.C. DESIGN DATA BASE REV. D1 (DM

SIGNATURES	DATE
DRN.	
CHK'D.	
ENG.	
PROJ. ENG.	
PROD.	

SCALE 2/1
SHT. 3 OF 8
NEXT HIGHER ASSY. B-DD-M8044-0

digital

TITLE
32K 16BIT MOS MEMORY

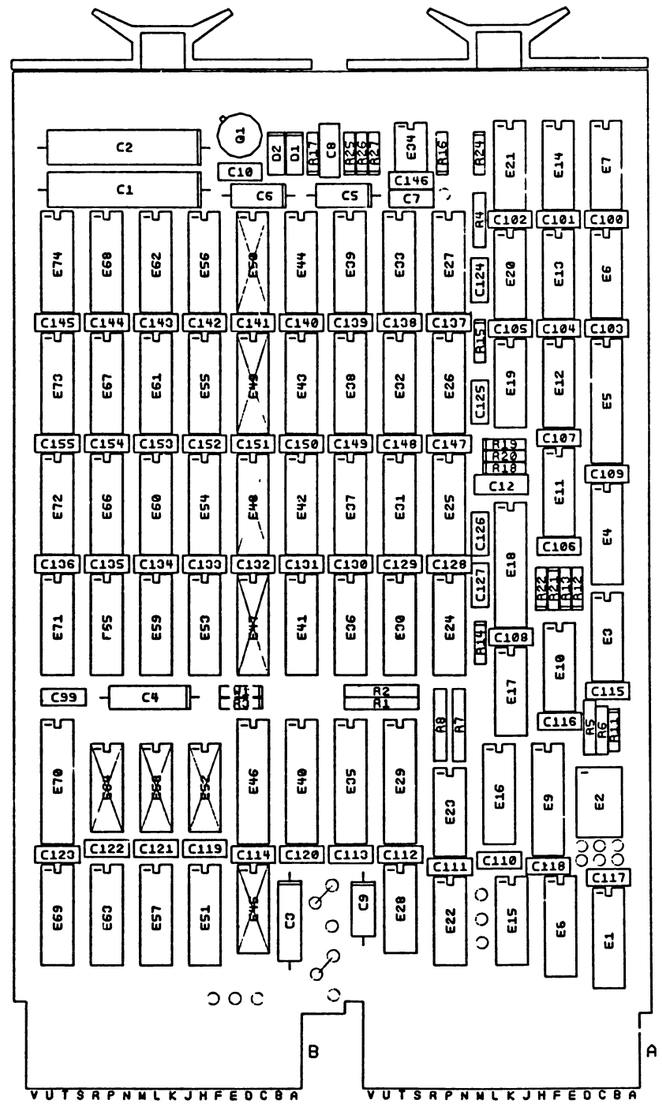
SIZE	CODE	NUMBER	REV
D	IUA	M8044-0-0	E

DUA M8044-0-0 E

MS# 2619-56

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MODULE VARIATIONS BA[illegible] DA & EA



NOTES:

REV	CHANGE NO	CHK

SIGNATURES	DATE
DRN.	
CHK'D.	3-12-7[illegible]
ENG.	
PROJ.ENG.	
PROD.	

SCALE 2/1
SHT. 4 OF 8
NEXT HIGHER ASSY. [illegible]-M8044-0-0

digital

TITLE
32K 16 BIT MOS MEMORY

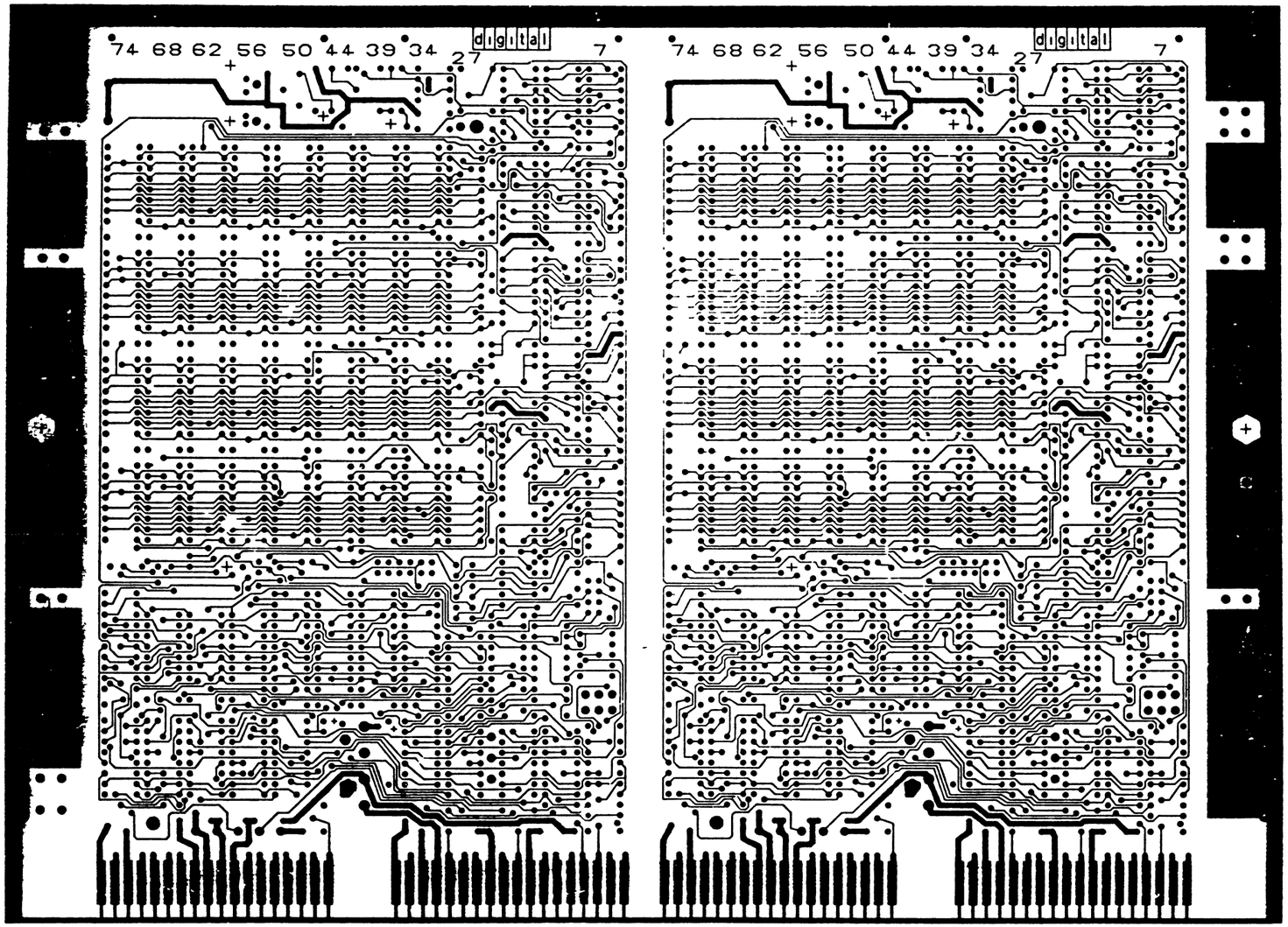
SIZE	CODE	NUMBER	REV
D	UA	M8044-0-0	E

1 MS# [illegible]

M8045 5013128D-P1 L1

M8045 5013128D-P1 L1

LAYER 1



REVISIONS		
CHK	CHANGE NO	REV

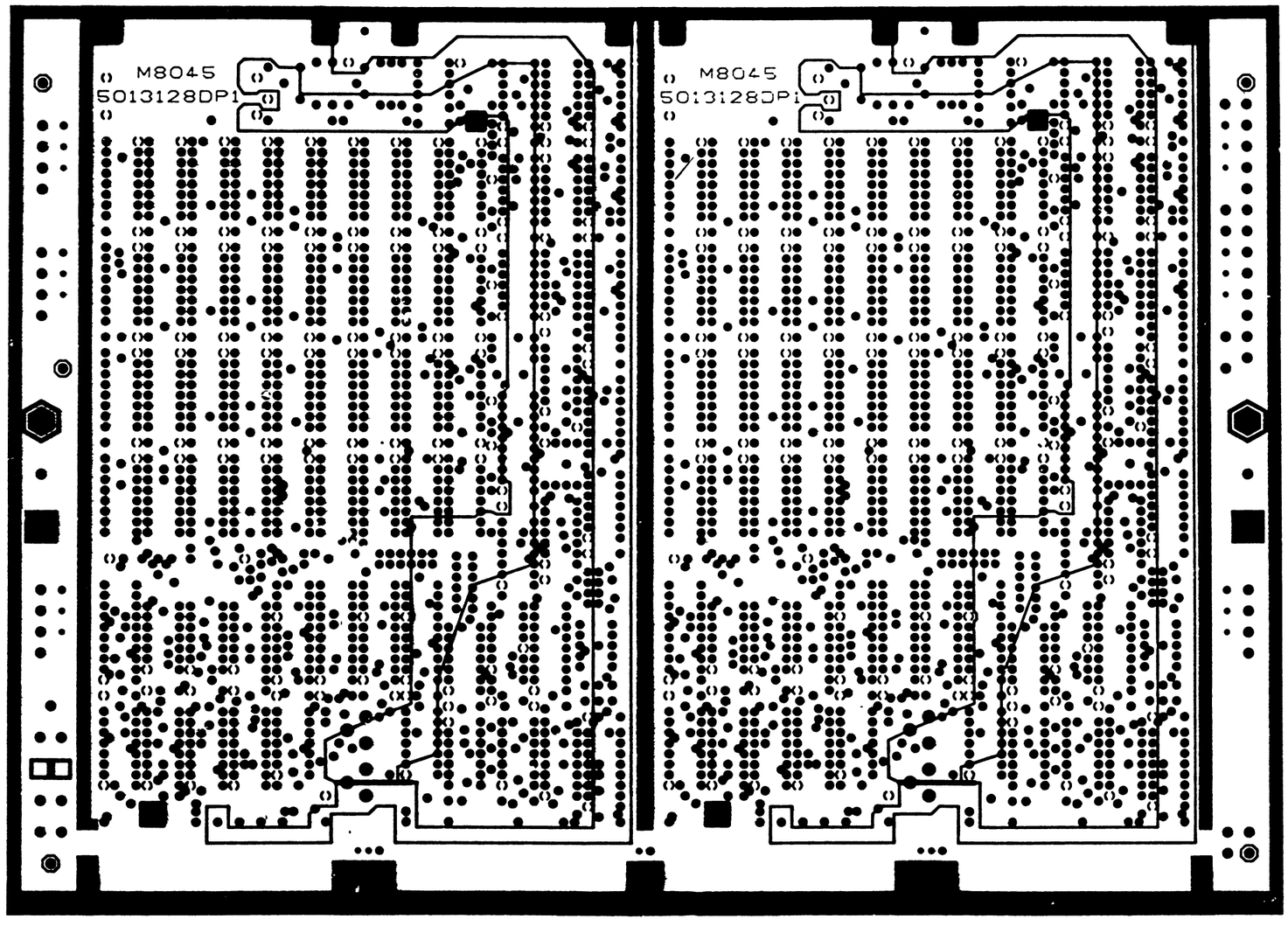
TITLE	SIZE	CODE	NUMBER	REV
32K 16BIT MOS MEMORY	D	UA	M8044-0-0	E
SCALE 2/1 SHEET 5 OF 8	DIST			

DUA M8044-0-0 E

M8045 5013128D-P1 L2

M8045 5013128D-P1 L2

LAYER 2



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
32K 16BIT MOS MEMORY	D	UA	M8044-0-0	E
SCALE 2/1 SHEET 6 OF 8	DIST			

D UA M8044-0-0 E

©1978

L3

L3

LAYER 3

M8045
5013128DP1

M8045
5013128DP1

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
32K 16BIT MOS MEMORY	D	UA	M8044-0-0	E
SCALE 2/1 SHEET 7 OF 8	DIST			

DUA M8044-0-0 E

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L4

L4

LAYER 4

M8045
5013128DP1
32K 18 BIT MOS MEM
SIDE 2

M8045
5013128DP1
32K 18 BIT MOS MEM
SIDE 2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
32K 16BIT MOS MEMORY	D	UA	M8044-0-0	E
SCALE 2/1 SHEET 8 OF 8	DIST			

D UA M8044-0-0 E

8 7 6 5 4 3 2 1

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NOTES:

1. ● = WIRE WRAP PIN

2.

TYPE MEMORY	JUMPER CONFIGURATION
NON PARITY	5 TO 7
PARITY	5 TO 6

3.

TYPE	JUMPER CONFIGURATION
4K	17 TO 15 & 17 TO 14
8K	17 TO 15 & 12 TO 14
16K	16 TO 15 & 16 TO 14
24K	16 TO 15 & 10 TO 14
32K	16 TO 15 & 10 TO 14

4.

STARTING ADDRESS DEC (K)	STARTING ADDRESS OCTAL	SWITCH SETTING (X = OFF) S1-1	S1-2	S1-3	S1-4	S1-5
0	000000					
4	020000					X
8	040000				X	
12	060000				X	X
16	100000			X		
20	120000			X		X
24	140000			X	X	
28	160000			X	X	X
32	200000		X			
36	220000		X			X
40	240000		X		X	
44	260000		X		X	X
48	300000		X	X		
52	320000		X	X		X
56	340000		X	X	X	
60	360000		X	X	X	X
64	400000	X				
68	420000	X				X
72	440000	X			X	
76	460000	X			X	X
80	500000	X		X		
84	520000	X		X		X
88	540000	X		X	X	
92	560000	X		X	X	X
96	600000	X	X			
100	620000	X	X			X
104	640000	X	X		X	
108	660000	X	X		X	X
112	700000	X	X	X		
116	720000	X	X	X		X
120	740000	X	X	X	X	
124	760000	X	X	X	X	X

5. NORMAL JUMPER 1 TO 3.
OPTIONAL JUMPER 1 TO 2
WILL ALLOW USER TO EXTEND USABLE
MEMORY SPACE FROM 28K TO 30K.

6.

JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	OUT	IN
W3	OUT	IN
W4	IN	OUT
W5	IN	OUT

7.

MEMORY SIZE	W1	R3
4K	IN	OUT
8K	IN	OUT
16K	OUT	IN
32K	OUT	IN
24K	OUT	IN

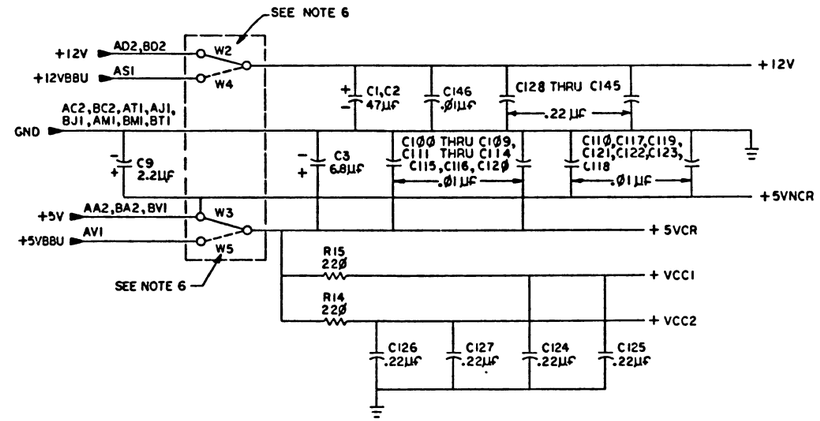
8.

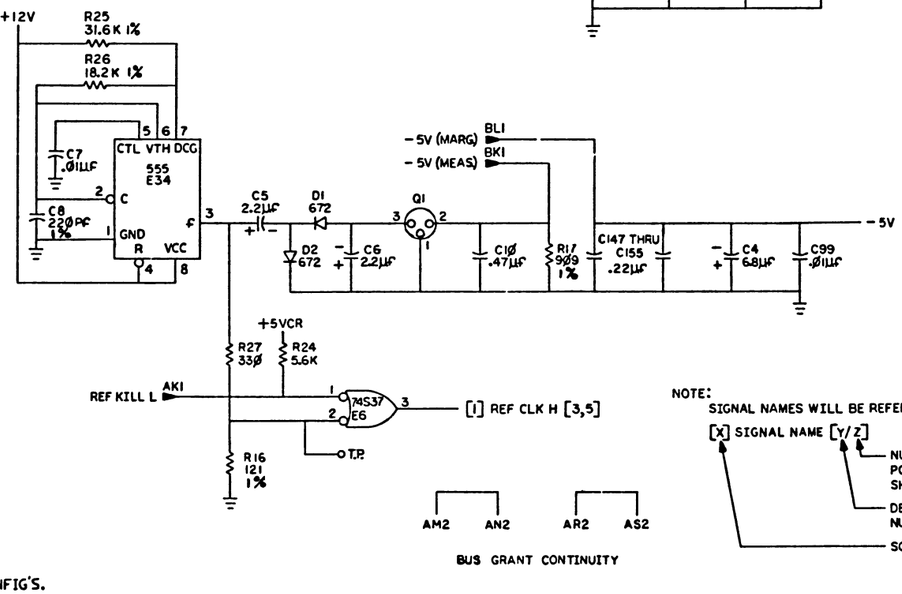
OPTION DESIGNATION	PART ARY VARIATION	SYSTEM DESCRIPTION
MSVII-DA	M8044-AA	4K X 16 BITS
MSVII-DB	M8044-BA	8K X 16 BITS
MSVII-DC	M8044-CA	16K X 16 BITS
MSVII-DD	M8044-DA	32K X 16 BITS
MSVII-DE	M8044-EA	24K X 16 BITS

9.

IC TYPE	+5V	GND	+12V	-5V
555		1	8	
MOS	9	16	8	1
74S373	20	10		
74LS393	14	7		
74S280	1	7		
74S374	14	7		
74S10	14	7		
74S11	14	7		
8641	16	8		
8640	8	1		
74S240	20	10		
74S37	14	7		
74S22	14	7		
1KX4 PROM	18	9		
74S02	14	7		
74LS75	5	12		
74S32	14	7		
74LS10	14	7		
74LS240	20	10		

10. THESE I.C.'S USED ONLY IN 8K, 24K & 32K CONFIG'S.





NOTE:
SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:

[X] SIGNAL NAME [Y/Z]

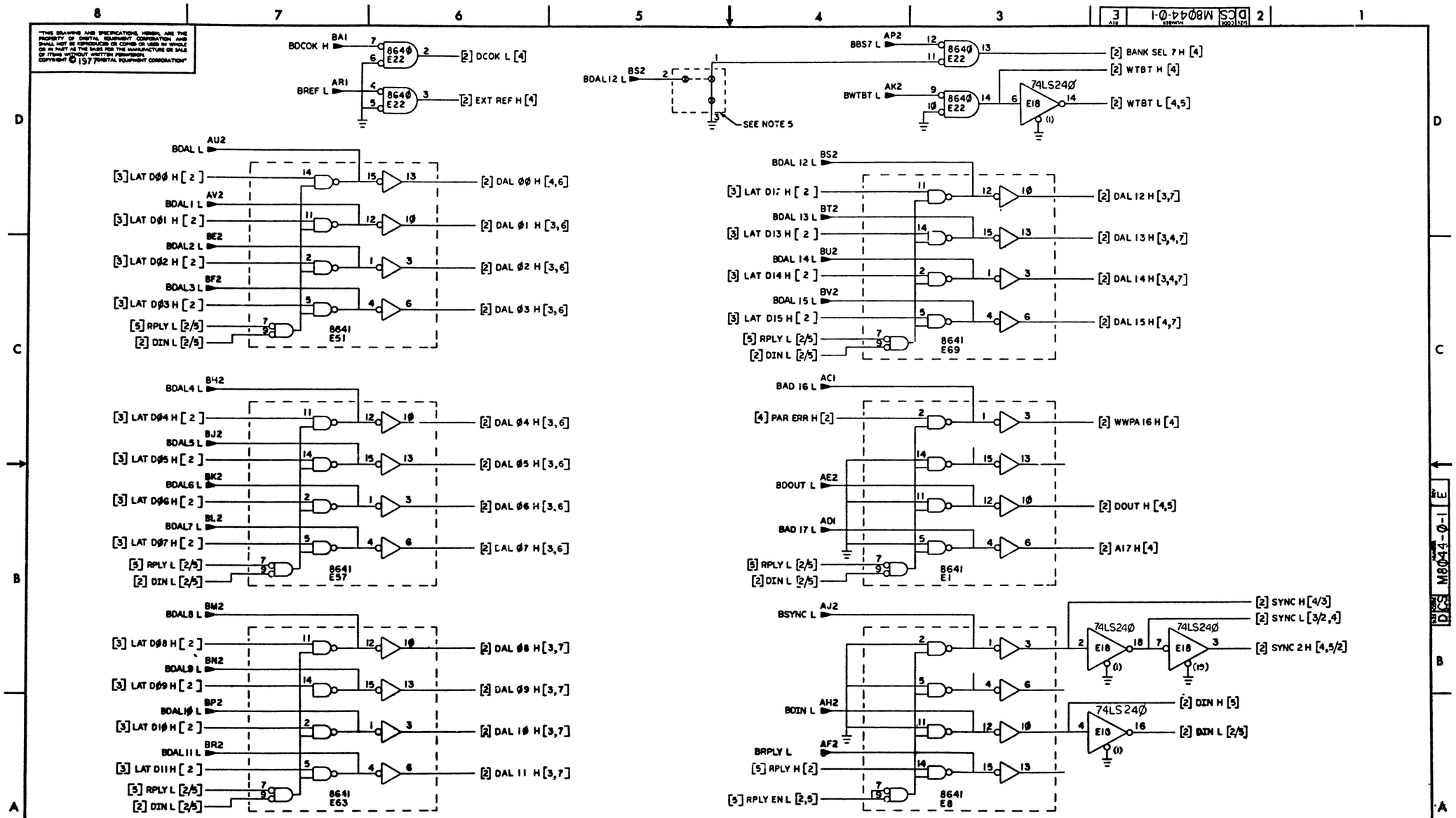
- NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.
- DESTINATION SHEET NUMBER.
- SOURCE SHEET NUMBER.

REVISIONS			
CHK	CHANGE NO.	REV.	
	M8044-COCO1	B	Stevenson 10-Jul-78
	R GIVEN		A.G. Given Apr 6-78
	M8044 ML002	C	R.GIVEN 27-Oct-78

M8004-ML003	D	8.5 Approved 7/25/80
M8044-SH005	E	Approved 13 Jan 81
R. GIVEN		R. Given 9 Jul 81

DRN Stan Garrity	10-25-77	FIRST USED ON: MSVII-D
CHK'D R. GIVEN	2-21-78	digital
ENG. R GIVEN	2-21-78	TITLE: 32K 16BIT MOS MEM
PROJ. ENG. R. Given	2-21-78	
PROG. R. Given	2-21-78	
NEXT HIGHER ASSY.	B-DD-M8044-0	SIZE D CODE CS NUMBER M8044-0-1 REV. E
SCALE		SHEET 1 OF 7 DIST.

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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
32K 16BIT MOS MEM	D	CS	M8044-0-1	E
SCALE	SHEET 2 OF 7	DIST.		

M8044-0-1 E

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[5] ROW ADD OUT CONT H [3]

OC 74S373-Ø E35

[2] DAL Ø1 H [3,6]
[2] DAL Ø2 H [3,6]
[2] DAL Ø3 H [3,6]
[2] DAL Ø4 H [3,6]
[2] DAL Ø5 H [3,6]
[2] DAL Ø6 H [3,6]
[2] DAL 14 H [3,4,7]
[2] SYNC L [3/2,4]

R2 22 [3] MUX A1 H [6/2,7/2]
R1 22 [3] MUX A2 H [6/2,7/2]
R2 22 [3] MUX A3 H [6/2,7/2]
R1 22 [3] MUX A4 H [6/2,7/2]
R2 22 [3] MUX A5 H [6/2,7/2]
R1 22 [3] MUX A6 H [6/2,7/2]

[5] COL ADD OUT CONT L [3]

OC 74S373-Ø E46

[2] DAL Ø7 H [3,6]
[2] DAL Ø8 H [3,7]
[2] DAL Ø9 H [3,7]
[2] DAL 1Ø H [3,7]
[2] DAL 11 H [3,7]
[2] DAL 12 H [3,7]
[2] DAL 13 H [3,4,7]
[2] SYNC L [3/2,4]

R3 22 W1 [3] MUX A7 H [6/2,7/2]
SEE NOTE 7

[5] REF ADD OUT CONT L [3/2]

74LS393 E23 (ICL 2CL)
[1] REF CLK H [3,5]

OC 74S373 E29

[5] REF ADD OUT CONT L [3/2]

+5VCR
R4 5K
R4 5K
74S1Ø E2Ø
[3] PAR ERR IND H [4]

OC 74S373 E4Ø

[6] DO ØØ H [3]
[6] DO Ø1 H [3]
[6] DO Ø2 H [3]
[6] DO Ø3 H [3]
[6] DO Ø4 H [3]
[6] DO Ø5 H [3]
[6] DO Ø6 H [3]
[6] DO Ø7 H [3]
[4] DATA LAT L [3/2,4]

[3] LAT DØØ H [2]
[3] LAT DØ1 H [2]
[3] LAT DØ2 H [2]
[3] LAT DØ3 H [2]
[3] LAT DØ4 H [2]
[3] LAT DØ5 H [2]
[3] LAT DØ6 H [2]
[3] LAT DØ7 H [2]

OC 74S373 E7Ø

[7] DO Ø8 H [3]
[7] DO Ø9 H [3]
[7] DO 1Ø H [3]
[7] DO 11 H [3]
[7] DO 12 H [3]
[7] DO 13 H [3]
[7] DO 14 H [3]
[7] DO 15 H [3]
[4] DATA LAT L [3/2,4]

[3] LAT DØ8 H [2]
[3] LAT DØ9 H [2]
[3] LAT D1Ø H [2]
[3] LAT D11 H [2]
[3] LAT D12 H [2]
[3] LAT D13 H [2]
[3] LAT D14 H [2]
[3] LAT D15 H [2]

REVISIONS
CHK | CHANGE NO. | REV

TITLE 32K 16BIT MOS MEM
SIZE D | CODE CS | NUMBER M8Ø44-Ø-1 | REV. E
SCALE — | SHEET 3 OF 7 | DIST.

DEC FORM NO. SMD 130

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[5] PLUP2 H [4/3]
[2] WTBT H [4]
74S02 E7
74S74 E14
[4] DATI REQ L [5/2]
[2] SYNC H [4/3]
[4] DATI CYC END L [4]
[2] DCOK L [4]
74S32 E10
[2] WTBT L [4,5]
74S02 E7
[2] DOUT H [4,5]
74S37 E6
[4] DATO REQ L [5]
[2] SYNC H [4/3]
[4] DATO CYC END L [4]
[2] SYNC H [4/3]
8640 E13
[5] DL4 L [4]
[5] DL6 H [4,5]
[5] INT REF L [4,5/5]
74S11 E11
[5] PLUP2 H [4/3]
74S74 E12
[4] DATA LAT L [3/2,4]
[2] SYNC2 H [4,5/2]
74S74 E12
74S02 E7
[4] DATO CYC END L [4]
8640 E13
[4] DATI CYC END L [4]
[5] PLUP2 H [4/3]

+5VNCR
R5 5K
R6 5K
R11 5.6K
SW1 E2
SEE NOTE 4
1KX4 PROM E9
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CEA
CEB
+5VNCR
R12 1K
+5VNCR
R13 1K
SEE NOTE 3
[2] A17 H [4]
[2] WWPA16 H [4]
[2] DAL15 H [4,7]
[2] DAL14 H [3,4,7]
[2] DAL13 H [3,4,7]
[2] EXT REF H [4]
[2] BANK SEL7 H [4]

74LS75 E16
[2] DAL 00 H [4,6]
D0
D1
D2
D3
R0(1)
R0(0)
R1(1)
R1(0)
R2(1)
R2(0)
R3(1)
R3(0)
ENB1
ENB2
[4] LAT A00 H [5]
[4] LAT A00 L [5]
[4] LAT R0 SEL L [5]
[4] LAT R0 SEL H [5]
[3] PAR ERR IND H [4]
[4] PAR ERR H [2]
[4] PLUP 1 H [5]
[2] SYNC L [3/2,4]
[4] DATA LAT L [3/2,4]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
32K 16 BIT MOS MEM	D	CS	M8044-0-1	E
SCALE	SHEET 4 OF 7	DIST.		

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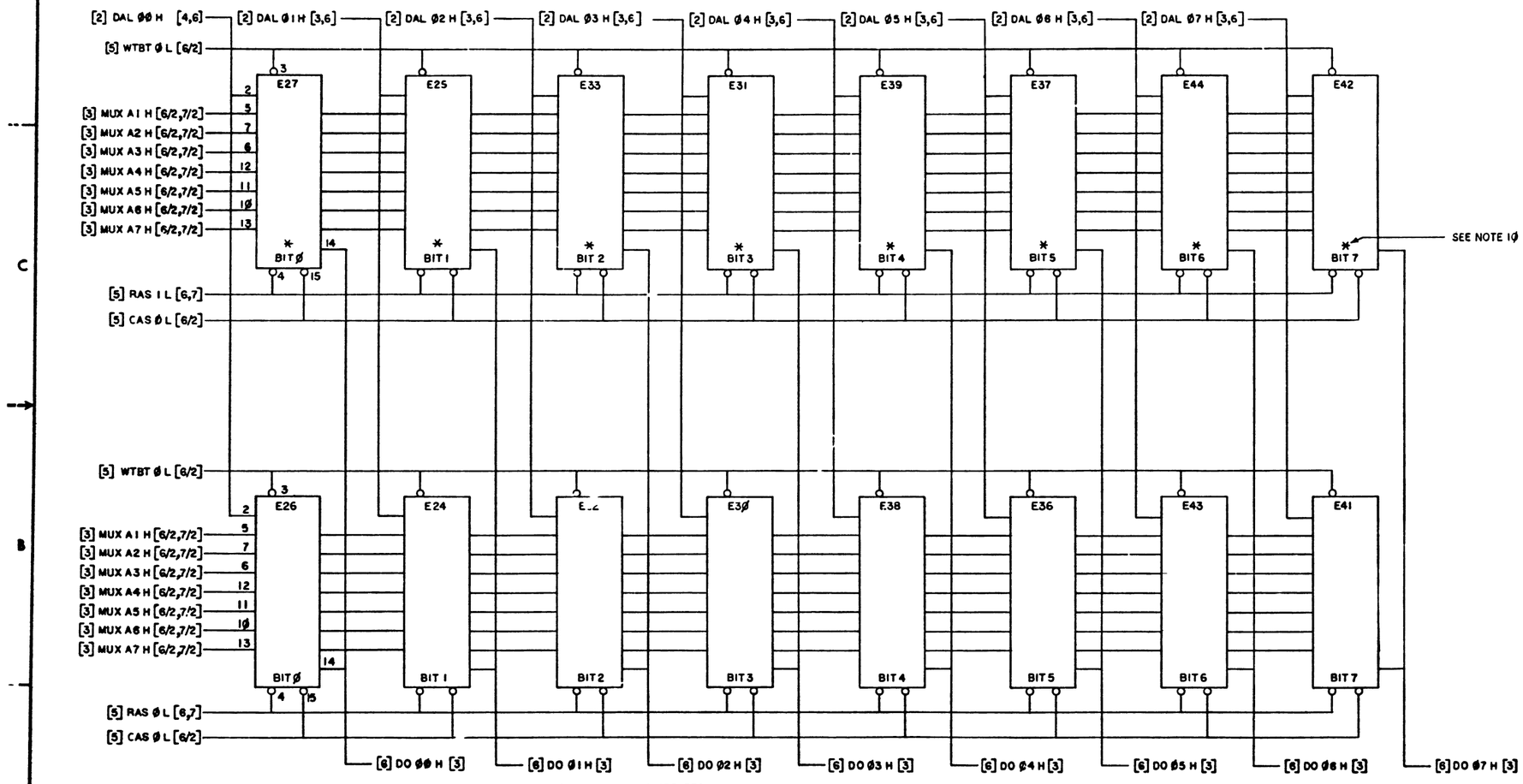
74LS24Ø E5 [5] REF REQ L [5]
74LS24Ø E5 [5] PLUP 2 H [4/3]
74S74-Ø1 E21 [1] REF CLK H [3,5]
8640 E13
74S74-Ø1 E21
74LS24Ø E18 [5] INT REF L [4,5/5]
8640 E13 [5] INT REF H [5/2]
[5] ROW ADD INH L [5]
74LS1Ø E28 [5] DL9 H [5/2] [5] DL6 L [5/2] [5] INT REF H [5/2]
74LS24Ø E5 [5] DL2 H [5] [5] DL2 L [5]
74LS24Ø E5 [5] DL3 H [5] [5] DLT 3 H [5]
74S22 E19 R18 19.6 1%
+5VCR R19 619 1%
R2Ø 289 1%
C12 220 PF 1%
74S1Ø E2Ø [5] REF REQ L [5] [4] DATI REQ L [5/2] [4] DATO REQ L [5]
74S11 E11 [5] LOCK OUT L [5/2]
74S22 E19 [5] DL6 L [5/2]
74LS24Ø E18 +5VCR R21 33Ø
E4 200 NS DEL. LINE 20NS TAP [5] DL2 H [5] [5] DL3 H [5] [5] DL5 H [5] [5] DL6 H [4,5] [5] DL7 H [5] [5] DL9 H [5/2] [5] DL Ø H [5/3]
74LS24Ø E5 [5] LOCK OUT L [5/2]
R22 215 [5] DL1Ø H [5]
74LS24Ø E5 [5] DL4 L [4]
[5] DL4 H [5]
74LS24Ø E18 [5] DL5 H [5] [5] DL5 L [5]
74LS24Ø E18 [5] DLT 5 H [5]
74LS24Ø E5 [5] DL6 H [4,5] [5] DL6 L [5/2]
74LS1Ø E28 [5] INT REF L [4,5/5] [5] DL Ø H [5/3] [5] DL7 H [5] [5] DL9 H [5/2] SEE NOTE 2
74S74 E15 [5] RPLY EN L [2,5] [2] SYNC 2 H [4,5/2] [5] RPLY L [2/5]
74S37 E6 [5] RPLY H [2]
74S74 E15 [4] PLUP 1 H [5] [5] DATO RPLY CLK H [5] [2] SYNC 2 H [4,5/2]
74S37 E3 [5] INT REF L [4,5/5] R7 22 [5] CAS Ø L [6/2]
74S37 E3 [5] DLT 3 H [5] R8 22 [5] CAS 1 L [7/2]
74S32 E1Ø [4] LAT AØØ L [5] [2] WTBT L [4,5]
74S32 E1Ø [4] LAT AØØ H [5]
74S11 E11 [5] DL Ø H [5/2] [4] DATI REQ L [5/2] [5] INT REF L [4,5/5]
74S37 E3 R8 22 [5] WTBT Ø L [7/2]
74S37 E3 R8 22 [5] WTBT 1 L [7/2]
[5] DATO RPLY CLK H [5]
74S37 E17 [4] LAT RØ SEL L [5] [5] INT REF L [4,5/5]
74S37 E17 [4] LAT RØ SEL H [5]
74S32 E1Ø [5] DL Ø H [5/3] [5] DLT 3 H [5]
74S37 E17 R7 22 [5] RAS Ø L [6,7]
74S37 E17 R7 22 [5] RAS 1 L [6,7]
74S1Ø E2Ø [5] DL2 L [5] [5] DL5 L [5] [5] ROW ADD INH L [5] [5] ROW ADD OUT CONT H [3]
74LS1Ø E28 [5] DLØ H [5/3] [5] INT REF L [4,5/5] [5] COL ADD OUT CONT L [3]
74S37 E6 [5] LOCK OUT L [5/2] [5] INT REF H [5/2] [5] REF ADD OUT CONT L [3/2]
74S02 E7 [2] DIN H [5] [2] DOUT H [4,5] [5] RPLY EN L [2,5]

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
32K 16 BIT MOS MEM	D	CS	M8Ø44-Ø-1	E
SCALE — SHEET 5 OF 7	DIST			

ASSY CODE DCS M8Ø44-Ø-1 REV E

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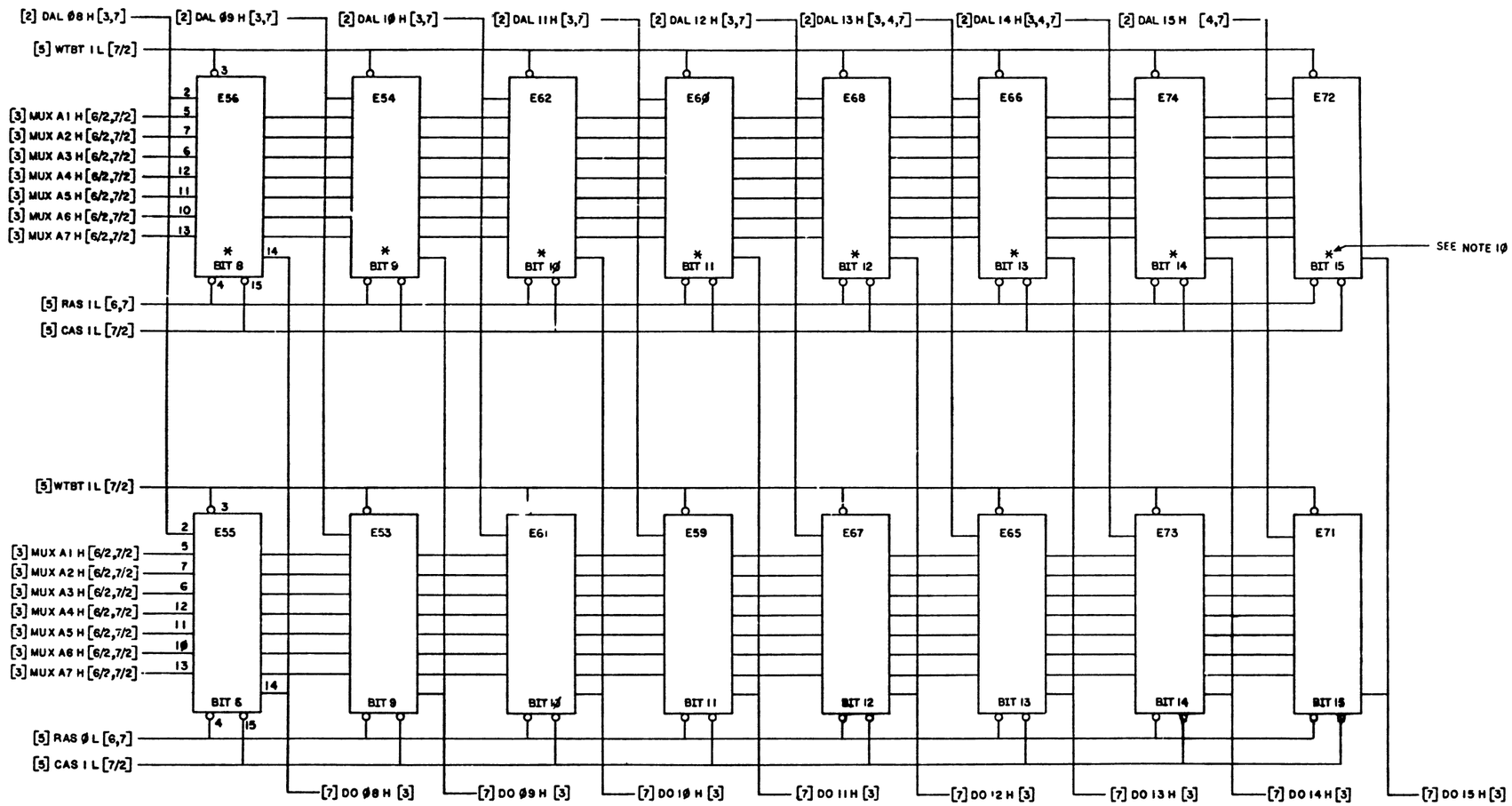


VCC1 — E26,E27,E32,E33,E38,E39,E43,E44, E55,E56,E61,E62,E67,E68,E73,E74
VCC2 — E24,E25,E30,E31,E36,E37,E41,E42, E53,E54,E59,E60,E65,E66,E71,E72
+5VNCR — E1, E8, E9, E15,E16,E45,E51,E52,E57,E58,E63,E64,E69,E70
+5VCR — E3 THRU E7, E10 THRU E14,E17 THRU E23,E28,E29,E35,E40,E46

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
32K 16BIT MOS MEM	D	CS	M8044-Ø-1	E
SCALE	SHEET 6 OF 7	DIST.		

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VCC1 — E26,E27,E32,E33,E38,E39,E43,E44, E55,E56,E61,E62,E67,E68,E73,E74
VCC2 — E24,E25,E3Ø,E31,E36,E37,E41,E42, E53,E54,E59,E6Ø,E65,E66,E71,E72
+5VNCR — E1, E8, E9, E15,E16,E45,E51,E52,E57,E58,E63,E64,E69,E7Ø
+5VCR — E3 THRU E7, E1Ø THRU E14, E17 THRU E23, E28,E29,E35,E4Ø,E46

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
32K 16 BIT MOS MEM	D	CS	M8Ø44-Ø-1	E
SCALE — SHEET 7 OF 7	DIST.			

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DUAMB047-0-0

JUMPER SHIP CONFIGURATION

CONFIGURATION	WIRE WRAP PINS FROM	WIRE WRAP PINS TO	LEVEL
RAM BANK 8	J30	J31	L1
	J32	J33	L1
	J31	J32	L2
CH8 ADDRESS 176500	J23	J18	L1
	J24	J19	L1
CH1 ADDRESS 177560	J20	J19	L2
	J20	J15	L1
	J25	J14	L1
	J27	J13	L1
ROM (TU58 BOOT)	J37	J36	L1
	J21	J22	L1
	J34	J37	L2
	J33	J30	L2
	J20	J19	L2
BAUD RATES	J45 (CH8)	J50 (38.4K)	L1
	J46 (CH1)	J48 (9600)	L1
VECTORS (CH8,300CH1,60)	J53	J57	L1
	J54	J52	L1
	J56	J51	L1
	J54	J55	L2
BREAK DETECTION (HALT)	J6	J7	L1
CRYSTAL CLOCK	J68	J67	L1
SLU PARAMETERS (8 DATA BITS, NO PARITY, ONE STOP BIT)	J59	J61	L1
	J62	J64	L1
	J60	J63	L1
	J61	J62	L2
	J59	J66	L2
	J63	J65	L2

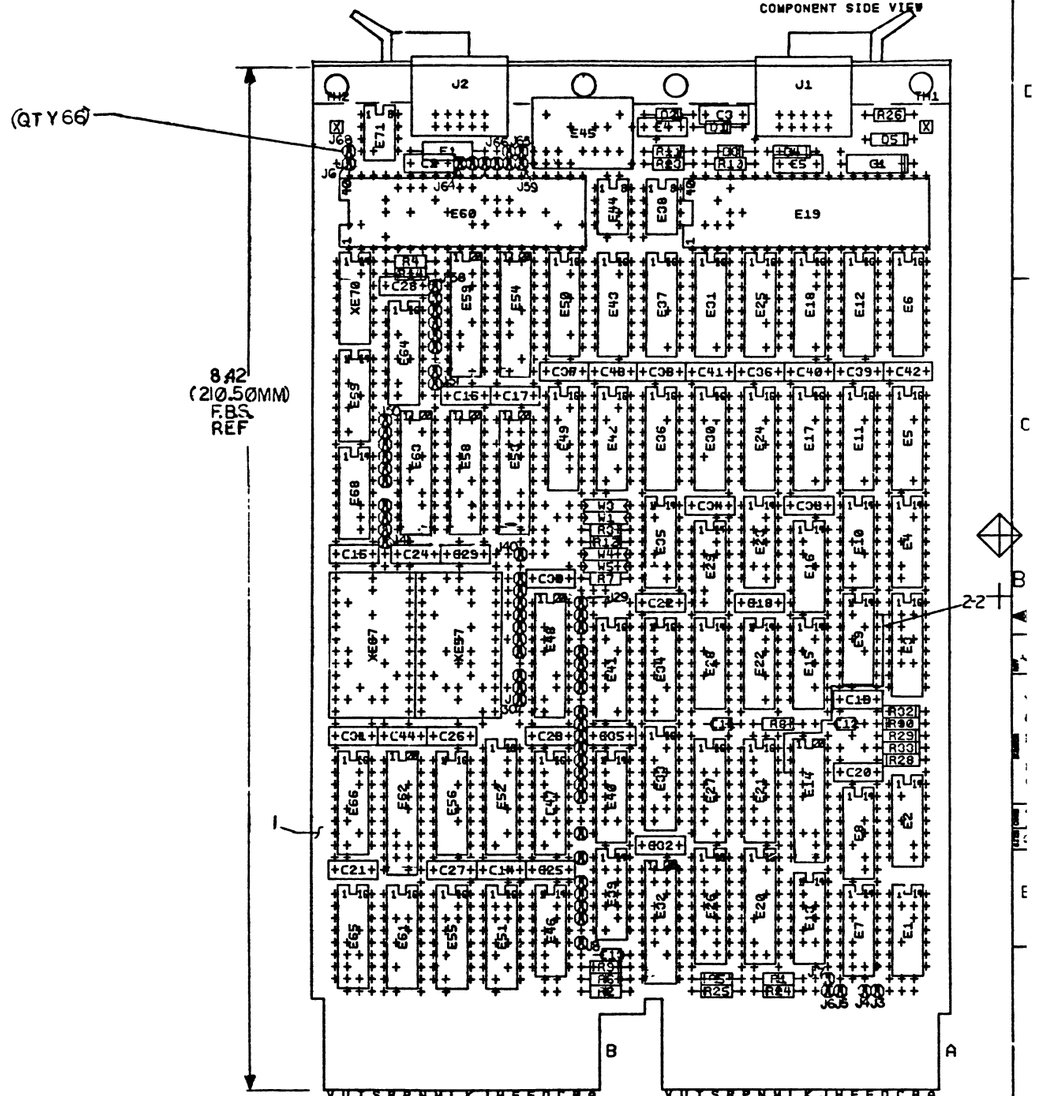
SEE NOTE #2

REWORK INSTRUCTIONS

ECO #2

ETCH CUT SIDE 1, AS SHOWN:
2-1 AT E9-2

WIRE ADD SIDE 1, AS SHOWN:
2-2 FROM E9-13 TO E14-3



NOTES:
1. IDEA EDIT REV. IS 328
2. WIRE WRAP JUMPERS ARE INSTALLED AFTER THE MODULE HAS SUCCESSFULLY PASSED G.A. TEST.

CHG/CHANGE NO	REV
8.	
	C
	B

ETCH REV. D
P.C. DESIGN DATA BASE REV. A

SIGNATURES	DATE
DRN.	9/5/79
CHK'D	2-0-77
ENG.	10 MAY 79
PROJ.ENG.	10 MAY 79
PROD.	9/20/79

digital

TITLE: LSI-11 MEM & I/O

SCALE 2-1 | SHT. 1 OF 3 | NEXT HIGHER ASSY. B-DQ-M9047-0

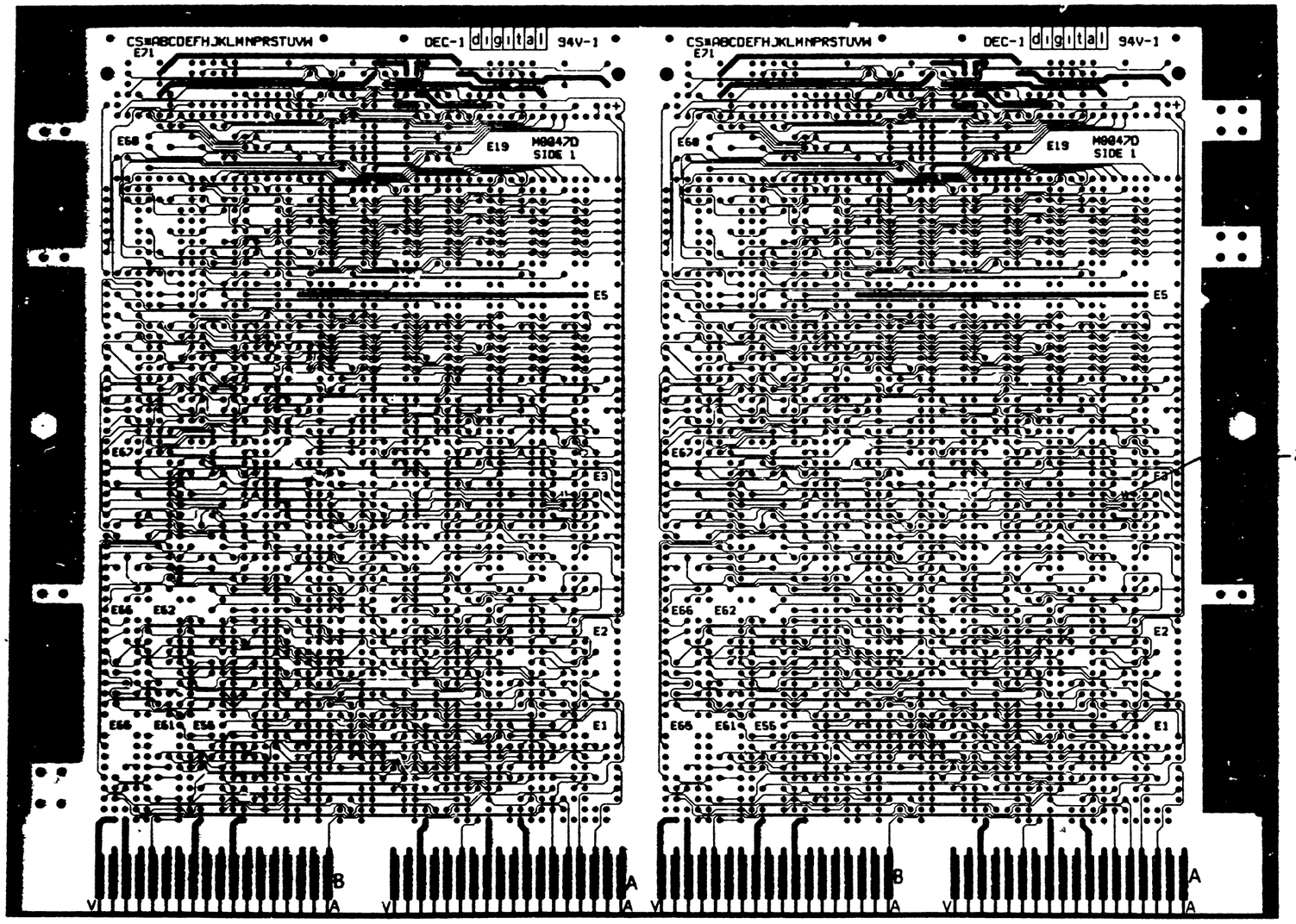
SIZE	CODE	NUMBER	REV
D	UA	M9047-00	C

MS#1902770

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50-13564-D M8047 L1 LAYER 1

50-13564-D M8047 L1



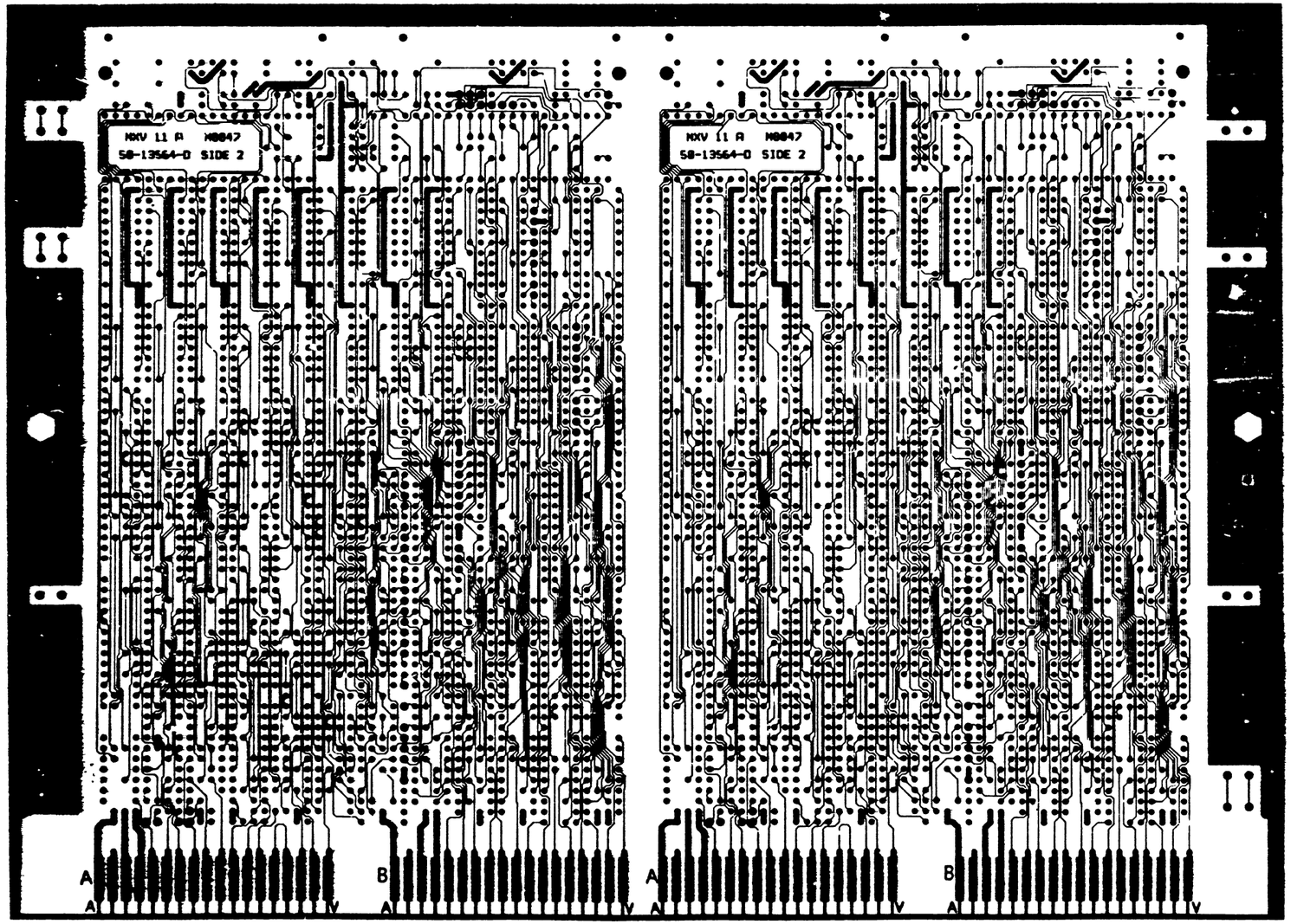
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI11 MEM & I/O	D	UA	M8047-0-0	C
SCALE 2/1 SHEET 2 OF 3	DIST			

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L4

LAYER 4



REVISIONS		
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TITLE	SIZE	CODE	NUMBER	REV
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SCALE 2/1 SHEET 3 OF 3	DIST.			

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[5] D 15 H — BDAL 15 L — [1] DA 15 H [+] [1] DA 13 H — 74LS375 E66 — [1] A 13 H [2/3] [1] A 13 L [2] — [5] D 05 H — BDAL 05 L — [1] DA 05 H [4,6/2]

[5] D 14 H — BDAL 14 L — [1] DA 14 H [+] [1] DA 12 H — [1] A 12 H [2/3,8] [1] A 12 L [2] — [5] D 04 H — BDAL 04 L — [1] DA 04 H [4,6/8]

[5] D 13 H — BDAL 13 L — [1] DA 13 H [+] [1] DA 10 H — [1] A 10 H [2/3,8/2] [1] A 10 L [2] — [5] D 03 H — BDAL 03 L — [1] DA 03 H [4,6/2,7]

[6] VEC H — 74LS32 E39 — [3] RPLY L — [5] D 12 H — BDAL 12 L — [1] DA 12 H [+] [1] DA 09 H — [1] A 09 H [2/2] [1] A 09 L [2/3] — [5] D 02 H — BDAL 02 L — [1] DA 02 H [4,6/2]

8641 E65 — 8641 E51

[1] DIN H — 74LS04 E46 — ENB 1,2 ENB 3,4 — [1] SYNC L — [3] RPLY L

[7] SLU H — 74LS00 E46 — [7] SEL 2 L

[5] D 11 H — BDAL 11 L — [1] DA 11 H [+] [1] DA 07 H — 74LS375 E56 — [1] A 07 H [2,8/2] [1] A 07 L [2/2] — [5] D 07 H — BDAL 07 L — [1] DA 07 H [4,6/2]

[5] D 10 H — BDAL 10 L — [1] DA 10 H [+] [1] DA 05 H — [1] A 05 H [2/2,8/2] [1] A 05 L [2/2] — [5] D 06 H — BDAL 06 L — [1] DA 06 H [4,6/4]

[5] D 09 H — BDAL 09 L — [1] DA 09 H [+] [1] DA 04 H — [1] A 04 H [2/2,8/2] [1] A 04 L [2] — [5] D 01 H — BDAL 01 L — [1] DA 01 H [4,6/2,7]

[5] D 08 H — BDAL 08 H — [1] DA 08 H [+] [1] DA 03 H — [1] A 03 H [2/2,8/2] [1] A 03 L [2] — [5] D 00 H — BDAL 00 L — [1] DA 00 H [4,6/2,7/3]

8641 E61 — 8641 E55

[1] DIN H — 74LS00 E46 — [7] SLU RPLY L — [1] SYNC L — [3] RPLY L — [1] DIN H — 74LS00 E46 — [7] SEL 6 L

74LS373 E62 — [1] DA 15 H — [1] DA 14 H — [1] DA 11 H — [1] DA 08 H — [1] DA 06 H — [1] DA 02 H — [1] DA 01 H — [1] A 15 H [2/2] [1] A 14 H [2/3] [1] A 11 H [2/4,8] [1] A 08 H [2/3,8/2] [1] A 06 H [2/3,8/2] [1] A 02 H [2,7,8/2] [1] A 01 H [2,7,8/2] — [1] SYNC L

74LS375 E47 — BBS7 L — AP2 — 8640 E13 — [1] BS7 H [2/3] [1] BS7 L [2]

BAD 17 L — AD1 — 8640 E1 — [1] A 17 H [2/2] [1] A 17 L

BAD 16 L — AC1 — 8640 E1 — [1] A 16 H [2/2] [1] A 16 L

BWTBT L — AK2 — 8640 E13 — [1] WT H [2] [1] WT L [3]

[1] SYNC L

BDIN L — AH2 — 8640 E1 — 74S240 E14 — [1] DIN H [3] [1] DIN L [2,7]

BD OUT L — AE2 — 8640 E1 — 74S240 E14 — [1] DOUT H [2] [1] DOUT L [7]

BSYNC L — AJ2 — 8640 E13 — 74S240 E14 — [1] SYNC H [2] [1] SYNC L [2,7] — [5] R14-1

REVISIONS		
CHK	CHANGE NO.	REV.
MP	M8047-MR001	B
	M8047-MR002	C
	M8047-AB003	D
	M8047-AB004	E

DRN.	R. FITCH	22AUG78
CHK'D	R.W.Cantu	6 Feb 79
ENG.	Robert Fitch	22AUG78
PROJ. ENG.	Robert Fitch	29 JAN 79
PROD.C.	Randy RH	5/23/79
NEXT HIGHER ASSY.	B-DD-M8047-0	
SCALE	NONE	
SHEET	1 OF 3	

FIRST USED ON: MXVII-A

digital

TITLE: LSI-11 MEM AND I/O

SIZE: D — CODE — NUMBER: MSM8047-0-1 — REV.

DIST.

PCMAX47-0-1 REV F

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[1]A Ø1 H
[3]COL ADD L
[1]A Ø2 H
[1]A Ø3 H
[1]A Ø4 H
[1]A Ø5 H
[1]A Ø6 H
[1]A 14 H
[1]A Ø7 H
[3]ROW ADD L
[1]A Ø8 H
[1]A Ø9 H
[1]A 10 H
[1]A 11 H
[1]A 12 H
[1]A 13 H

81 LS97 E53 / 81 LS97 E58

[2]MUX A1 L [4/2]
[2]MUX A2 L [4/2]
[2]MUX A3 L [4/2]
[2]MUX A4 L [4/2]
[2]MUX A5 L [4/2]
[2]MUX A6 L [4/2]
[2]MUX A7 L [4/2]

[5]9.6K
[3]REF ADD L
[5]2.4K
[5]19.2K
[5]4.8K
[5]38.4K
[5]12K
[5]600HZ

81 LS97 EG3

J33 J34 +3V

1K x 4 PROM E52 (A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 CEA CEB)

[1]A 17 H
[1]A 16 H
[1]A 15 H
[1]A 14 H
[1]A 13 H
[1]BS7 H
[1]SYNC L

[2]16K L
+5V
R7 2.7K
W5
W4
[2] RAM SEL -[3]
[2] 4K L

W3 W1
[2] MUX A7 L [4/2]

[1]BS7 L
[1]A12 L
[1]A11 H
[1]A10 L
[1]A09 L
74 S260 E49 → J22

[1]A17 H
[1]A16 H
[1]A15 H
[1]A14 H
74 S260 E48 → J21

J11 [1]A13 H
J10 [1]A13 L

[1]SYNC H
74 LS00 E22 → J20

74 LS32 E37
[1]WT H
[2]ROM L [3]

JUMPER CHART				
MODULE TYPE	W1	W3	W4	W5
M8047-AA	IN	OUT	IN	OUT
M8047-CA	OUT	IN	OUT	IN

[1]BS7 H
[1]A12 H
[1]A11 H
[1]A10 H
[1]A09 L
[1]A08 H
[1]A07 L
[1]A06 H
J23
J24
[1]A05
J25
J27
J28

74 S133 E34 → [2] SLU Ø L [7/1]
176500 X
176510 X
176520 X
176530 X

74 LS00 E22 → [2] SLU H

74 S133 E41 → [2] SLU 1 L [7/2]
176500 TO 176570 X
177500 TO 177570 X

[5]CLOCK H
[6]FE 1 H
[6]RDATA 1
[3]RPLY H

6881 E7 → AF1, AE1, AF2

J3 BRI
J4 BEVNT L
J5 BAI
J6 BDCOK H
J7 API
BHALT L
BRPLY L

[1]A Ø9 H
[1]A Ø5 H
[1]A Ø4 H
[1]A Ø3 H
[1]A Ø9 L
[1]A Ø5 L
[1]A Ø4 L
[1]A Ø3 L
J15 J14 J13 J12 J16 J17 J18 J19

+5V → AA2, BA2, BV1
+12V → AD2, BD2
GND → AC2, AJ1, AM1, AT1, BC2, BJ1, BM1, BT1
AR2
AS2

REVISIONS		
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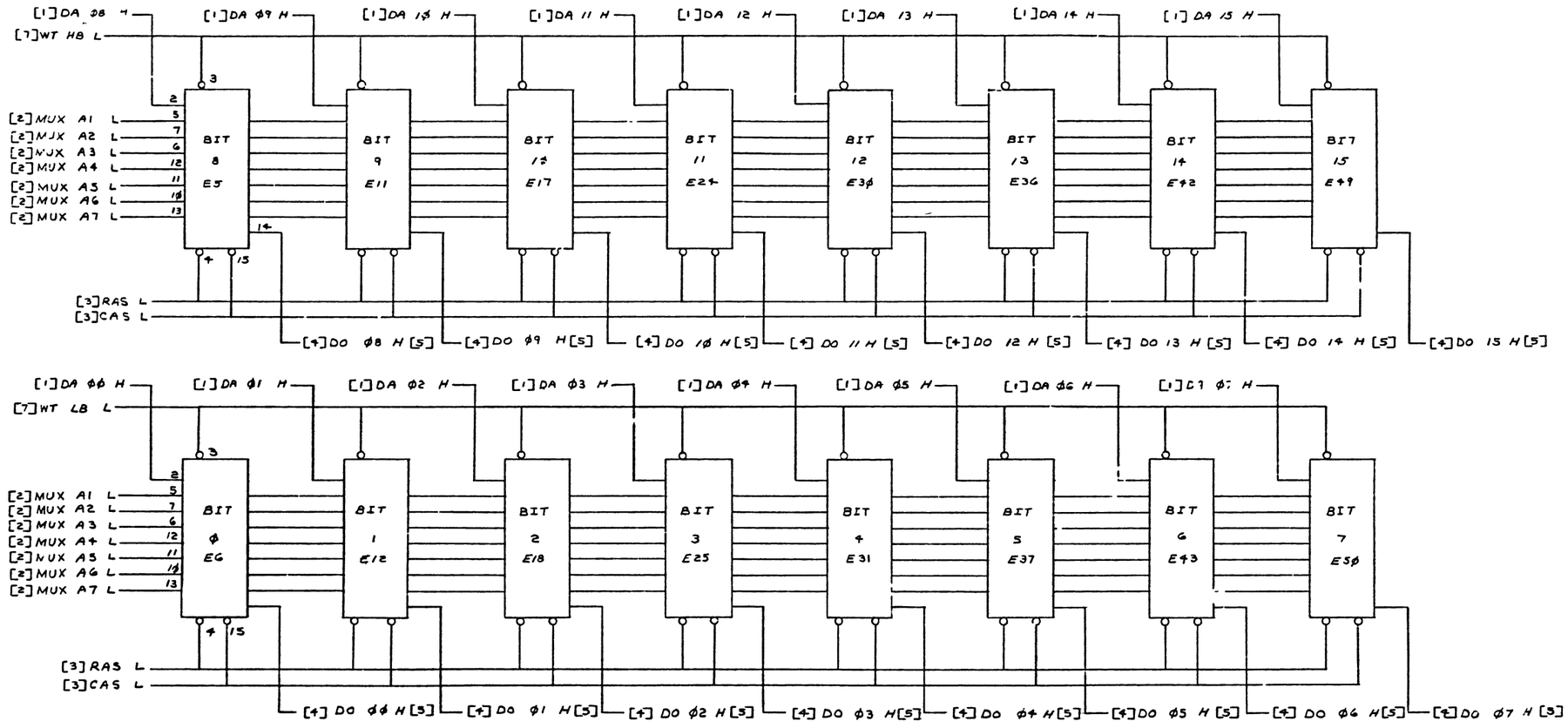
NOTE:
RPLY ON T∅ FOR DOUT
RPLY ON T1 FOR DIN
UN LATCH DATA ON T4
AND NOT REF

[3] T0 H
[3] T3 H
74 LS08 E33
[3] RAS L [1/2]
[3] REF (∅) H
74 LS∅∅ E29
[3] CAS L [1/2]
[3] T5 H
[3] T1 H
[3] T2 H
[3] T4 H [5]
[3] T6 H
[3] T7 H
[3] T8 H
[3] T9 H
+5V
R29 261
200NS DELAY LINE 20 NS TAP E3
[3] T1∅ H
.332 196
R3∅ 19.6
74 S24∅ E14
[5] R14-1
8881 E2
R28 511
R33 215
C13 22∅ PF
74 LS27 E9
74 LS74 E15 DATI
[3] DATI (1) H
[3] DATI (1) L
[3] DATI (∅) L
[3] DATI (∅) H
[1] WT L
[2] RAM SEL L
74 LS∅4 E9
74 LS74 E15 DATO
[3] DATO (1) L
[3] DATO (∅) L
[3] DATO (∅) H
[1] DOUT H
[3] T∅ L
[3] T6 H
[3] REF (∅) H
7410 E1∅
[3] DATO (1) H
8640 E13
[3] T7 H
[3] T∅ L
[3] REF (∅) L
74 LS27 E16
[2] INIT H
74 LS27 E9
+5V
R8 7.5K
300 NS
[2] ROM L
[7] SLU RPLY L
8881 E2
C11 22∅ PF
74 LS27 E16
[1] DIN H
[1] DOUT H
74 LS02 E35
74 LS02 E35
[3] RPLY H [2,1]
74 S24∅ E14
[3] RPLY L [1/3]
[5] R14-1
[3] RFR (1) H
[3] RFR (1) L
[3] RFR (∅) L
[3] RFR (∅) H
74 LS74 E15 RFR
74 LS∅4 E4
[5] 76.8 K
[3] T9 H
[3] T6 L
[3] REF H
7410 E1∅
[3] REF (1) H
[3] REF (∅) L
[3] REF (∅) H [5]
[3] REF CLR L
74 LS74 E23 REF
74 LS∅4 E4
[3] REF (1) L
[3] REF H
74 LS∅4 E4
[3] T∅ H
[3] T∅ L
74 LS∅4 E4
[3] T6 H
[3] T6 L
74 LS∅4 E4
[3] T2 H
[3] T2 L
[3] REF H
[3] REF CLR L
74 LS∅∅ E29
[3] REF ADD L [2]
[3] REF (∅) H
[3] T∅ H
7410 E1∅
[3] COL ADD L [2]
[3] T2 L
[3] REF (∅) H
74 LS∅∅ E29
[3] ROW ADD L [2]

REVISIONS
CHK | CHANGE NO | REV

TITLE LSI-11 MEM AND I/O
SIZE CODE CS
NUMBER M8047-0-1
REV. E
SCALE
SHEET 3 OF 8
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SIZE	CODE	NUMBER	REV.
D	CS	M8Ø47-Ø-1	E
SCALE		SHEET 4 OF 8	DIST.

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+5V
OSC1 E49 8 14 7
19.6608M
J68 8
J67 1

74LS373 E69
1A 3 [5] 9830.4 M
1B 4 [5] 4.9152 M
1C 5 [5] 2.4576 M
1D 6 [5] 1.2288 M
2A 11 [5] 614.4 K (38.4K)
2B 10 [5] 307.2 K (19.2K)
2C 9 [5] 153.6 K (9600)
2D 8 [5] 76.8 K (REF) (4800) [3]
1A 13, CLR1 1, CLR2 12, 2A 2

74LS373 E68
1A 3 [5] 38.4 K (A7 (2400) [2]
1B 4 [5] 19.2 K (A6) (1200) [2]
1C 5 [5] 9.6 K (A5) [2]
1D 6 [5] 4.8K (A4) (300) [2]
2A 11 [5] 2.4K (A3) (150) [2]
2B 10 [5] 1.2K (A2) [2]
2C 9 [5] 600 HZ (A1) [2]
2D 8 [5] 300 HZ
1A 13, CLR1 1, CLR2 12, 2A 2
[5] R14-1 [1,3/2]
R14 100

74LS373 E48
1D1 2D2 3D3 4D4 5D5 6D6 7D7 8D8 11 ENB 1 CO
[+] DO 15 H [1] D 15 H [1]
[+] DO 14 H [1] D 14 H [1]
[+] DO 13 H [1] D 13 H [1]
[+] DO 12 H [1] D 12 H [1]
[+] DO 11 H [1] D 11 H [1]
[+] DO 10 H [1] D 10 H [1]
[+] DO 09 H [1] D 09 H [1]
[+] DO 08 H [1] D 08 H [1]

74LS373 E54
1D1 2D2 3D3 4D4 5D5 6D6 7D7 8D8 11 ENB 1 CO
[+] DO 07 H [1] D 07 H [1]
[+] DO 06 H [1] D 06 H [1]
[+] DO 05 H [1] D 05 H [1]
[+] DO 04 H [1] D 04 H [1]
[+] DO 03 H [1] D 03 H [1]
[+] DO 02 H [1] D 02 H [1]
[+] DO 01 H [1] D 01 H [1]
[+] DO 00 H [1] D 00 H [1]
[5] RAM SEL L

[3] T 4 H
[3] REF (0) H
74LS08 E20 13, 12, 11
[5] RAM SEL L [1]

[5] 614.4 K J56 8
[5] 307.2 K J49 8
[5] 153.6 K J48 8
[5] 76.8 K J47 8
[5] 38.4 K J44 8
[5] 19.2 K J42 8
[5] 4.8 K J43 8
[5] 2.4 K J41 8
J45 8 [5] CLK 0 [6/3]
J46 8 [5] CLK 1 [6/3]

[5] 307.2 K
74LS08 E28 4, 5, 6
74LS00 E29 1, 2, 3
74LS00 E29 1, 2, 3
Ø026 E71 2, 3, 7
Ø026 E71 1, 4, 8, 5
+12V
C2 .47 UF
C4 .47 UF
C3 .47 UF
D1 DG64
D2 DG64
D3 DG64
D5 +3.1
D4 -5.1V
C5 .47 UF
C1 3.9 UF
R23 680
-12V
-5V

74LS390 E70
[6] INIT H
SET 9 7, 6
CLR 3, 2
R3(1) 11
R2(1) 8
R1(1) 9
R0(1) 12
CLR0 1, CLK0 14
[5] CLOCK H [2]

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TITLE LSI-11 MEM AND I/O
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UART E69 (SLU 0) I/O

UART E13 (SLU 1) CONSOLE

DC003 E29

DC003 E26

J1

J2

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256X4 PROM E64

[6] PE Ø H 2
[6] PE 1 H 3
[6] FE Ø H 5
[6] FE 1 H 6
[6] OE Ø H 7
[6] OE 1 H 4
[2] SLU Ø L 1
15

11 D 12 H
10 D 13 H
9 D 14 H
12 D 15 H
13 19

[7] SEL 2 L

74LS257 E21

[6] XR Ø H 2 1A
[6] XR 1 H 3 1B
[6] XIE Ø H 5 2A
[6] XIE 1 H 6 2B
11 3A
16 3B
[7] BRK 1 (1) H 13 4B
[7] BRK Ø (1) H 14 4A
SEL OUT CRL
1 15

1Y 4 D Ø7 H
2Y 7 D Ø6 H
3Y 9 D Ø1 H
4Y 12 D ØØ H

[2] SLU Ø L
[7] SEL 4 L

74LS257 E27

[6] DR Ø H 2 1A
[6] DR 1 H 3 1B
[6] RIE Ø H 5 2A
[6] RIE 1 H 6 2B
11 3A
10 3B
14 4A
13 4B
SEL OUT CRL
1 15

1Y 4
2Y 7
3Y 9
4Y 12

[2] SLU Ø L
[7] SEL Ø L

J56 81LS97 E59 3 1 D Ø7 H
J55 81LS97 E59 6 7 D Ø5 H
J54 81LS97 E59 8 9 D Ø4 H
[6] VEC L

J53 81LS97 E59 12 11 D Ø3 H
[6] VEC 1 H 12
[6] VEC Ø H 13
74LS32 E37 11
81LS97 E59 14 13 D Ø2 H
81LS97 E59 16 15 D Ø1 H
81LS97 E59 18 17 D ØØ H
19

+5V R3 68Ø +3V

J58 +3V
J57
J52 [6] VEC 1 H
J51 [6] VEC Ø H

+3V 10
[1] DA ØØ H 12 74LS74 E68 9 [7] BRK1 (1) H 8 [7] BRK1 (1) L [6]
[7] XCSR 1 L 11 9 [7] BRK1 (Ø) L 8 [7] BRK1 (Ø) H
13 [6] INIT L

+3V 4
[1] DA ØØ H 2 74LS74 E68 5 [7] BRKØ (1) H 6 [7] BRKØ (1) L [6]
[7] XCSR Ø L 3 5 [7] BRKØ (Ø) L 6 [7] BRKØ (Ø) H
1 [6] INIT L

R9 2.7K +5V
C13 22Ø pf
+5V RG 33Ø
[7] SLU H [1] 19 18 8 [7] SLU RPLY L [1,3]
ENB RXCX SYNC BRPLY
[1] SYNC L 6
DCØØ4 E32
[1] DA Ø2 H 2 DAL2 SEL4 17 [7] SEL Ø L
[1] DA Ø1 H 3 DAL1 SEL1 16 [7] SEL 2 L [1]
[1] DA ØØ H 4 DALØ SEL2 15 [7] SEL 4 L
SEL Ø 14 [7] SEL 6 L [1]
BWTBT AK2 5 WTBT
[1] DOUT L 9 DOUT WT LB 13 [7] WT LB L [4]
[1] DIN L 7 DIN WT HB 12 [7] WT HB L [4]
[6] VEC H 1 VECTOR INWD 11 [7] INWD L

[7] WTLB L 4
[3] RPLY H 5 EN
[7] SLU H 6
74LS138 E33
[1] A Ø1 H 1 SELA
[1] A Ø2 H 2 SELB
[2] SLU 1 L 3 SELC

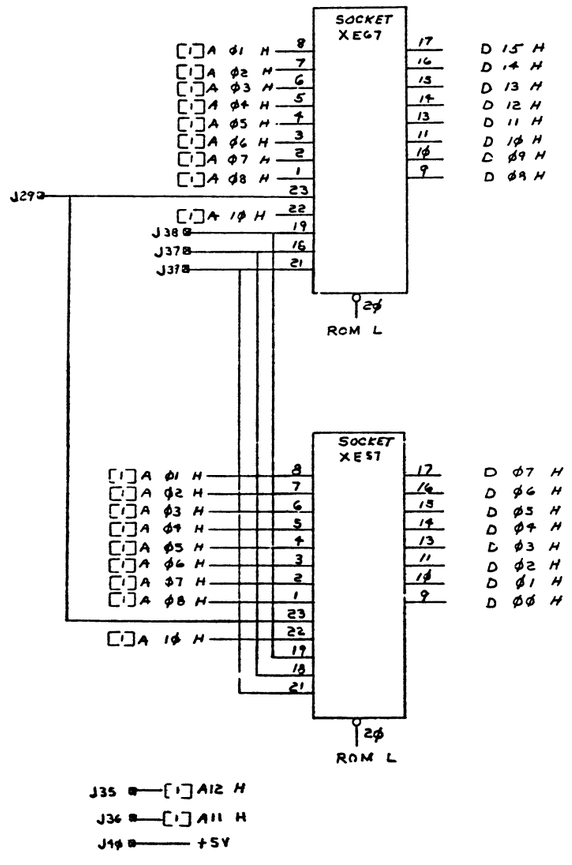
D Ø 15 [7] RCSR 1 L [6]
D1 14
D2 13 [7] XCSR 1 L [6]
D3 12 [7] XDBR 1 L [6]
D4 11 [7] RCSR Ø L [6]
D5 16
D6 9 [7] XCSR Ø L [6]
D7 7 [7] XDBR Ø L [6]

[7] INWD L 8
[7] SEL 2 L 9
74LS32 E33 10
[2] SLU Ø L 1
74LSØØ E22 2 3 [7] RDBR 1 L [6]
12
[2] SLU 1 L 13
74LSØØ E22 11 [7] RDBR Ø L [6]

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TITLE LSI-11 MEM AND I/O
SIZE D CODE CS NUMBER M8Ø47-Ø-1 REV. E
SCALE SHEET 7 OF 8 DWG.

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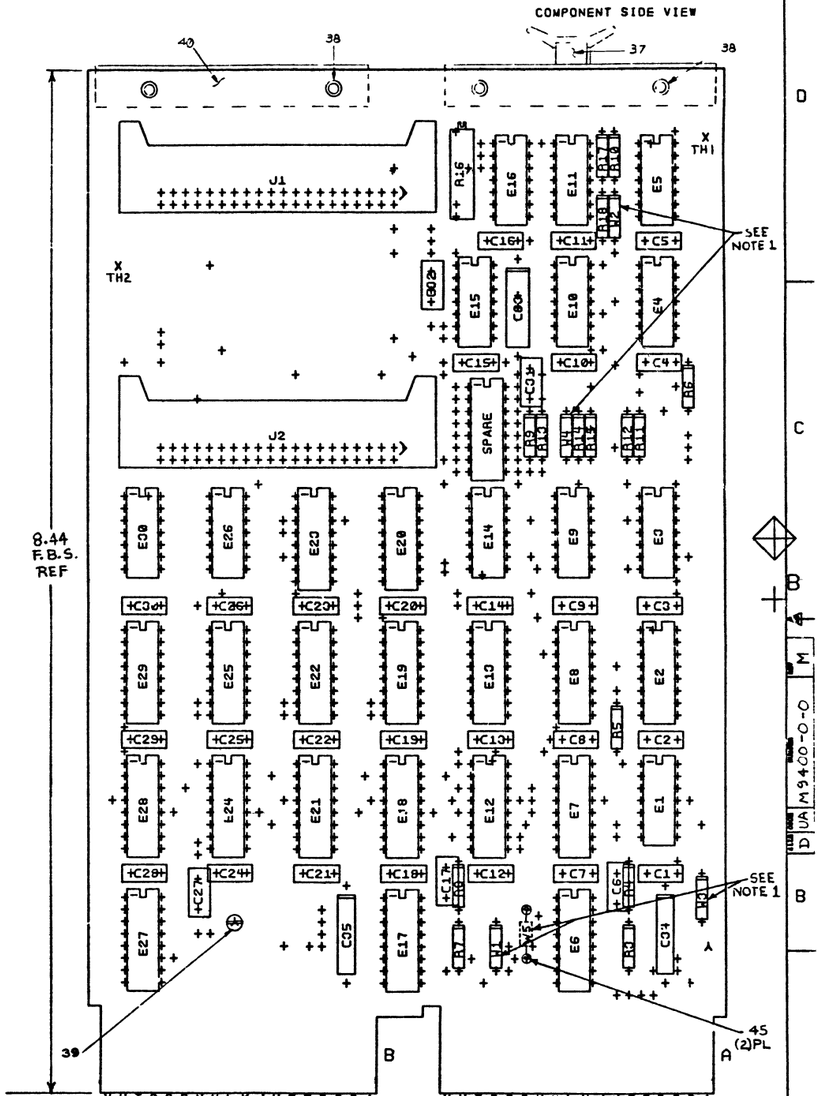
REVISIONS		
CHK	CHANGE NO.	REV

TITLE	LSI-11 MEM AND I/O	
SIZE	CODE	NUMBER
D	CS	M8Ø47-Ø-1
SCALE	SHEET 8 OF 8	DIST.

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W3- SHOULD ALWAYS BE IN UNLESS DOING BUS MARGININING
W4- IS OPTIONAL FOR RPLY OR NO RPLY
W5- A JUMPER WHICH WILL BE CALLED W5 IN ETCH REV D SHOULD BE IN WHEN RUNNING PROGRAMS SUCH AS DECXII WHICH MIGHT RESET INTERRUPT ENABLE BITS. THIS MIGHT RESULT IN NO RPLY TO IAK. IF W5 WERE NOT INSTALLED, DEPO* MDIIDXQLAI-1 MUST BE INSTALLED WHEN RUNNING DECXII. CAUTION: W5 SHOULD NOT BE INSTALLED WHEN RUNNING OPERATING SYSTEMS. WIRE WRAP POSTS FOR W5 DO NOT EXIST ON ETCH REV C AND BELOW. JUMPER AF2 TO AM2 ON BACKPLANE, REMOVE JUMPER AFTER RUNNING DECXII.
2. M9400-YN VARIATION IS THE SAME AS -YC VARIATION EXCEPT FOR REF DESIGNATIONS E19, E22, E25, E29.
3. REMOVE THE FOLLOWING UNUSED FINGERS FROM ARTWORK: AF1, AH1, AS1, AU1, BD1, BE1, BF1, BH1, BS1.



NOTES:

REV	CHK	CHANGE NO	DATE	BY
K		M9400-0008 REVISED & REDRAWN	25 MAY 78	J. CURTIS
L		M9400-A8010	2 JUN 78	J. CURTIS
M		M9400A8012	3 JUL 78	J. CURTIS

ETCH REV. E-P1
P.C. DESIGN DATA BASE REV. E

SIGNATURES	DATE
DRN. J. RICHARD	8-12-77
CHK'D.	16DEC77
ENG.	13DEC77
PROJ. ENG.	12DEC77
PROD.	4/2/78

digital

TITLE LSI REF BOOT CABLE CONN

SCALE 2/1 | SIZE D | CODE UA | NUMBER M9400-0-0 | REV M
SHT. 1 OF 1
NEXT HIGHER ASSY. B-DD-M9400-0

MS#

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NOTES:

1. BD INIT L AND INIT H ARE SIGNALS GENERATED BY THIS MODULE THAT ARE USED ON THIS MODULE.
2. A STANDARD ROM STARTING LOCATION FOR THE FOLLOWING BOOTSTRAPS HAS BEEN ESTABLISHED. ALL FUTURE REV 11-X'S THAT INCLUDE ANY OF THESE BOOTSTRAPS SHOULD USE THE SAME STARTING LOCATIONS. IF A NEW BOOTSTRAP IS ESTABLISHED, PLEASE ECO THIS NOTE TO INCLUDE THE DEVICE AND STARTING LOCATION.

* PERTAINS TO REV 11-AC AND J ONLY.
** PERTAINS TO REV 11-HK AND L ONLY.
*** PERTAINS TO REV 11-N ONLY.

BOOTSTRAP	STARTING LOCATION
*. RX01	165242
*. ABSOLUTE LOADER	165406
*. RK05	165650
*. CPU DIAGNOSTIC (MEMORY ADDIFYING)	173302
*. CPU DIAGNOSTIC (NON-MEMORY MODIFYING)	173000
* MEMORY DIAGNOSTIC	173626
*. ODT	
**. REMOTE-11	173000
**. REMOTE-11 SECONDARY DOWNLINE LOAD	173006
**. RX01	173700
***. RX02	173000

3. ADJUST R16 SO THAT THE DMA REFRESH FPEQUENCY MEASURED AT E15 PIN8 IS AS FOLLOWS:
 MAX. FREQUENCY SETTING; 33.6 KHZ (29.76 µs)
 NOM. FREQUENCY SETTING; 33.3 KHZ (30.03 µs)
 MIN. FREQUENCY SETTING; 33.0 KHZ (30.30 µs)
 THIS FREQUENCY IS PRE-SET AT THE FACTORY AND SHOULD NOT BE ALTERED.

4. FOR -YN VARIATION SUBSTITUTE THE FOLLOWING I. C.'S :
 E19, P/N 23871A9-00
 E22, P/N 23872A9-00
 E25, P/N 23873A9-00
 E29, P/N 23874A9-00

IC 5264	8	16
IC 8136	8	16
IC 74174	8	16
IC 8554	8	16
IC 8641	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV.	CHANGE NO.	CHK	REVISIONS
K	M9400-0000B86A	D. Douglas	D. A Bennett 27-JUN-78 DICK BENNET
L	M9400-AB010	J. CURTIS	J. Curtis 25-JAN-79
M	M9400-AB012	J. CURTIS	J. Curtis 28-MAR-79

FIRST USED ON OPTION MODEL

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO

PARTS LIST

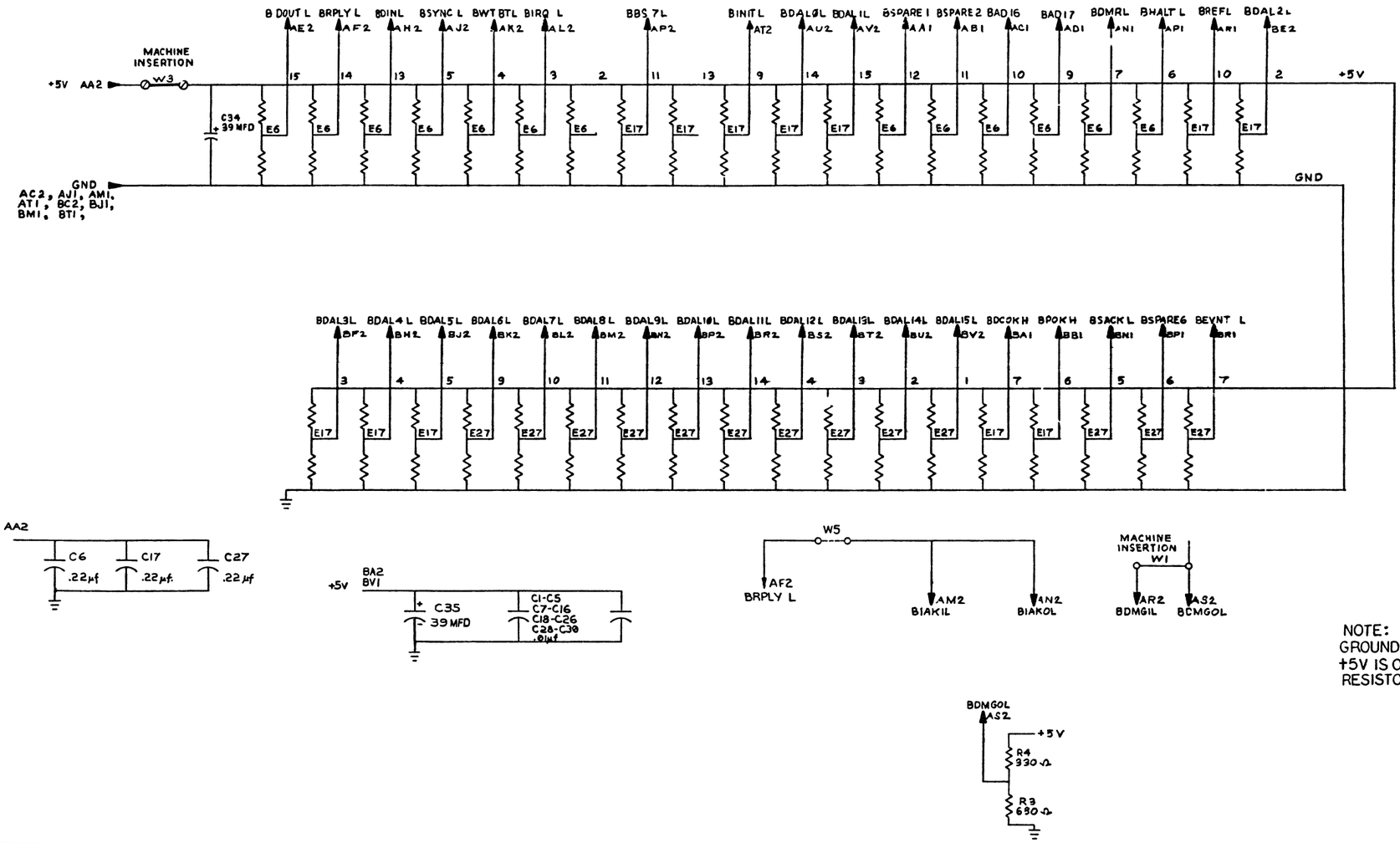
ETCH BOARD REV. E P1

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. D. Douglas	DATE 5/13/78	digital
CHK'D. J. Curtis	DATE 5-30-78	
ENG. R. Grandi	DATE 12-APR-78	TITLE LSI REF. BOOT CONN.
PROJ. ENG. D. Bennett	DATE 12-APR-78	
PROD. Paul Powell	DATE 6-27-78	
NEXT HIGHER ASSY		SIZE D CODE CS NUMBER M9400-0-1 REV. M
SCALE 1/1		
SHEET 1 OF 5		DIST.

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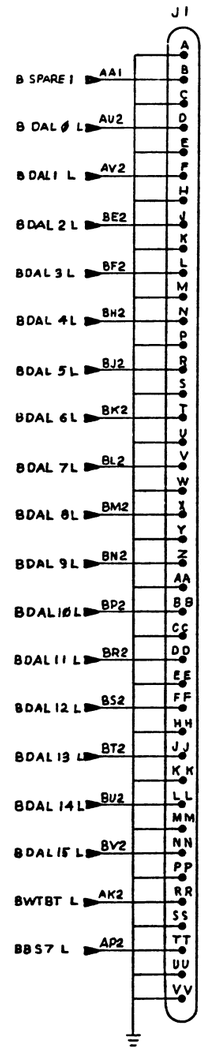
NOTE:
GROUND IS ON PIN 8
+5V IS ON PIN 16 OF EACH RESISTOR PACK.

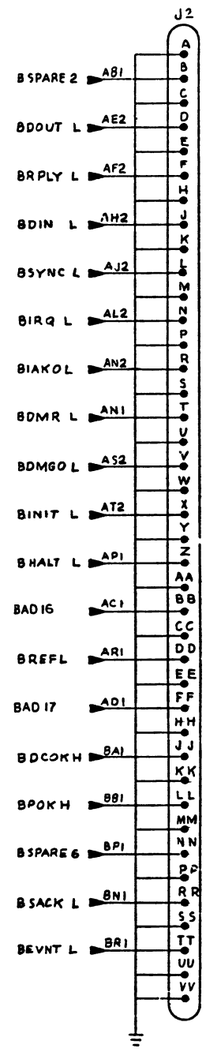
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI REF BOOT CABLE CONN	D	CS	M9400-0-1	M
SCALE — / —	SHEET 2 OF 5	DIST		

DEC FORM NO. DRG 1.38

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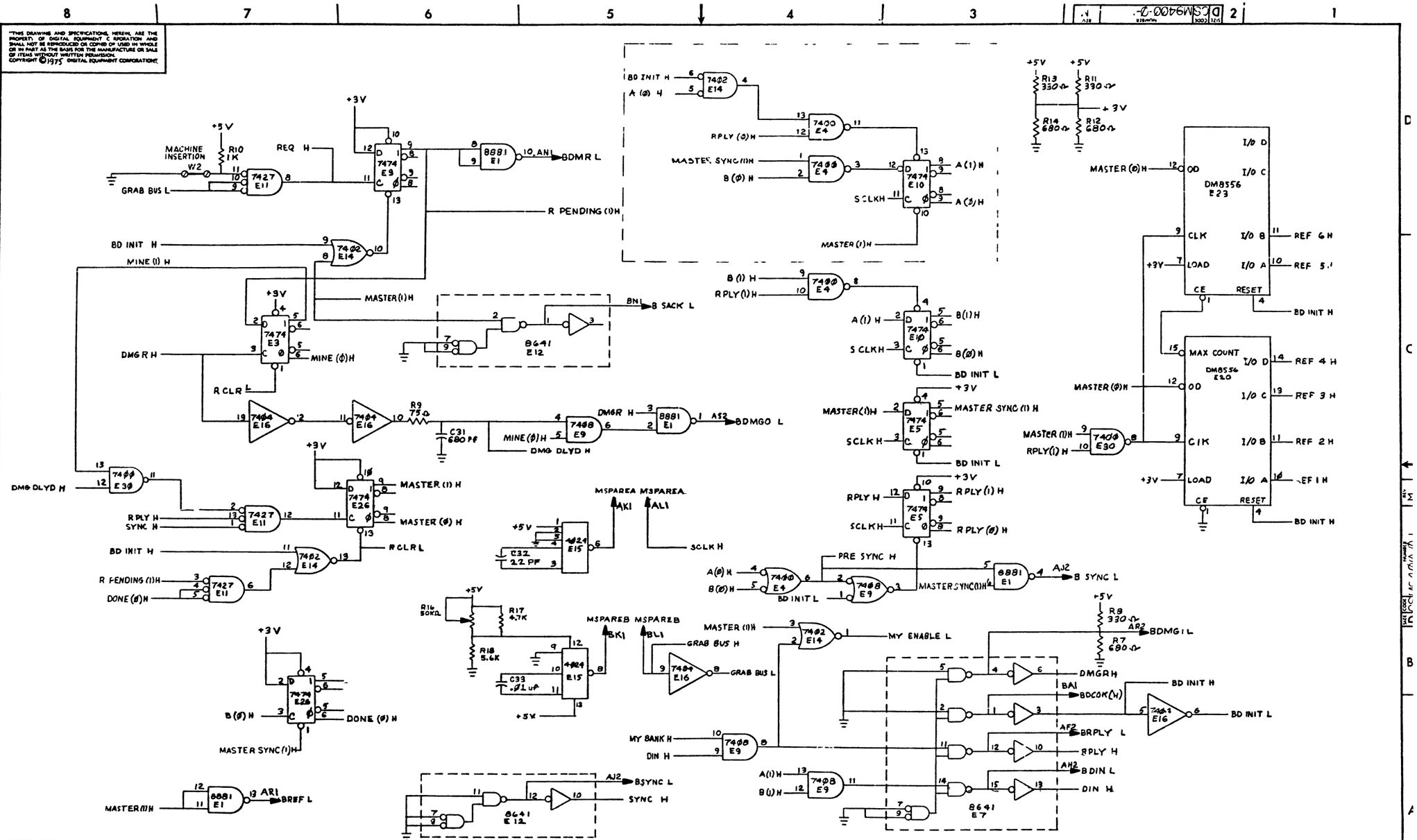


REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI REF BOOTCABLE CONN	D	CS	M9400-Ø-1	A
SCALE —	SHEET 3 OF 5	DIST		

DEC FORM NO. 5103 1/30

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EVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI REF BOOT CABLE CONN	D		CS M-9400-0-1	M
SCALE —	SHEET 4 OF 5		D.ST.	

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SEE NOTE #4

BA 1 H
BA 2 H
BA 3 H
BA 4 H
BA 5 H
BA 6 H
BA 7 H
BA 8 H
BA 10 H

512X4 PROM M5624 E19 03
512X4 PROM 02 M5624 E22
512X4 PROM M5624 E29
512X4 PROM M5624 E25

REF 1 H
REF 2 H
REF 3 H
REF 4 H
REF 5 H
REF 6 H

8641 E18
8641 E21
8641 E24
8641 E28

AU2 BDAL 0 L — DAL 0 H
AV2 BDAL 1 L — DAL 1 H
BE2 BDAL 2 L — DAL 2 H
BF2 BDAL 3 L — DAL 3 H
BH2 BDAL 4 L — DAL 4 H
BJ2 BDAL 5 L — DAL 5 H
BK2 BDAL 6 L — DAL 6 H
BL2 BDAL 7 L — DAL 7 H
BM2 BDAL 8 L — DAL 8 H
BN2 BDAL 9 L — DAL 9 H
BR2 BDAL 11 L — DAL 11 H
BP2 BDAL 10 L — DAL 10 H
BS2 BDAL 12 L — DAL 12 H
BT2 BDAL 13 L — DAL 13 H
BU2 BDAL 14 L — DAL 14 H
BV2 BDAL 15 L — DAL 15 H

MY BANK L
MY ENABLE L
MASTER (1) H

+5V
R5 1K
R6 1K
R13 1K
W4 MACHINE INSERT

DAL 11 H — 7438 E30
BS7 H
DAL 12 H
DAL 10 H
DAL 9 H
REF H
STROBE
SYNC H
8136 R2 OUTPUT

MY BANK H — 7404 E16 — MY BANK L

AD2 BBS7 L — BS7 H
AR1 BREF L — REF H
E12 8641

74174 E13
DAL 1 H — BA 1 H
DAL 2 H — BA 2 H
DAL 3 H — BA 3 H
DAL 4 H — BA 4 H
DAL 5 H — BA 5 H
DAL 6 H — BA 6 H

74174 E8
DAL 7 H — BA 7 H
DAL 8 H — BA 8 H
DAL 10 H — BA 10 H

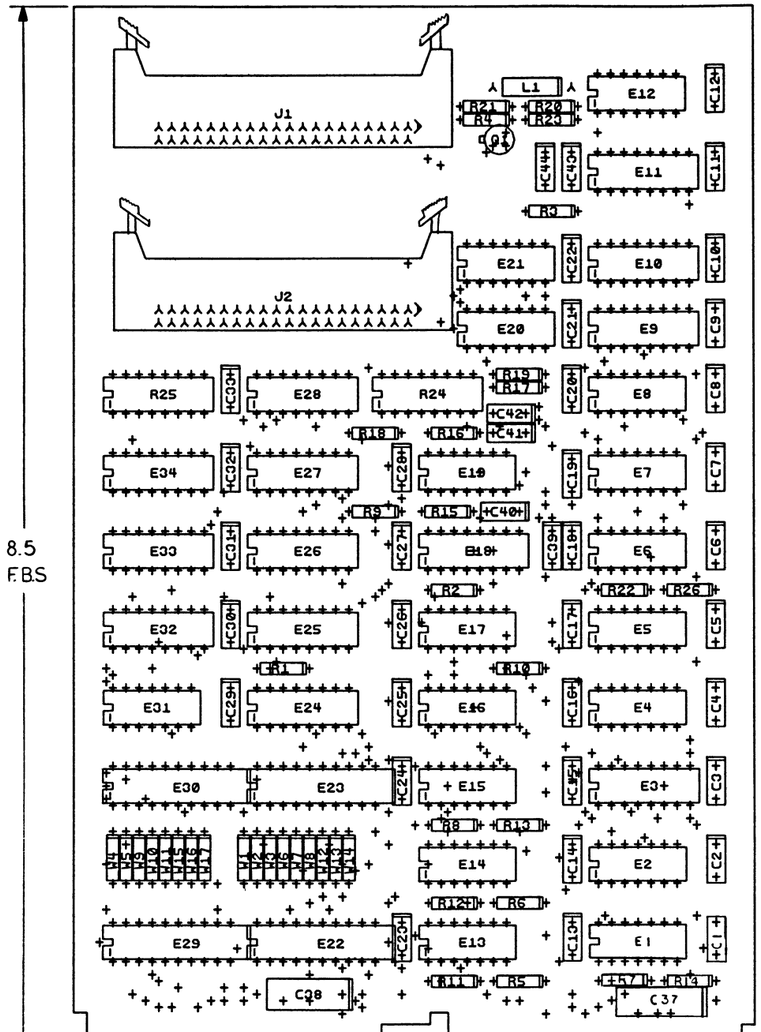
BD INIT L
SYNC H

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV
LSI REF BOOT CABLE CONN	D	CS	M9400-0-1	F
SCALE —	SHEET 5 OF 5	DIST		

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COMPONENT SIDE VIEW



NOTES:

CHK	CHANGE NO	REV
	M7269 0000	C

SIGNATURES	DATE
DRN.	
CHK'D.	
ENG.	
PROJ.ENG.	
PROD.	
SCALE 2/1	
SHT. OF 3	
NEXT HIGHER ASSY. B-DD-M7269-0	

digital

TITLE
RK VII CONTROL

SIZE	CODE	NUMBER	REV
D	UA	M7269-0-0	C

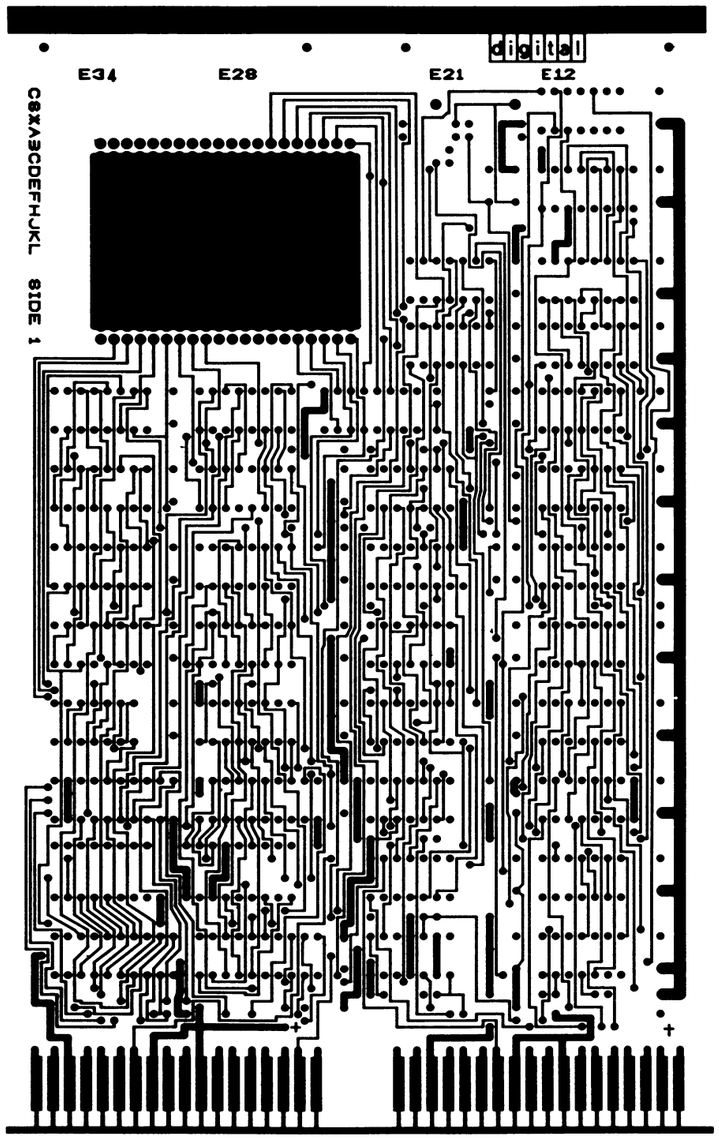
ETCH REV. C
P.C. DESIGN DATA BASE REV. C

D UA M7269-0-0 C

MS#40628

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M7269-10628 REV-C



VIEWED FROM SIDE 1

REVISIONS		
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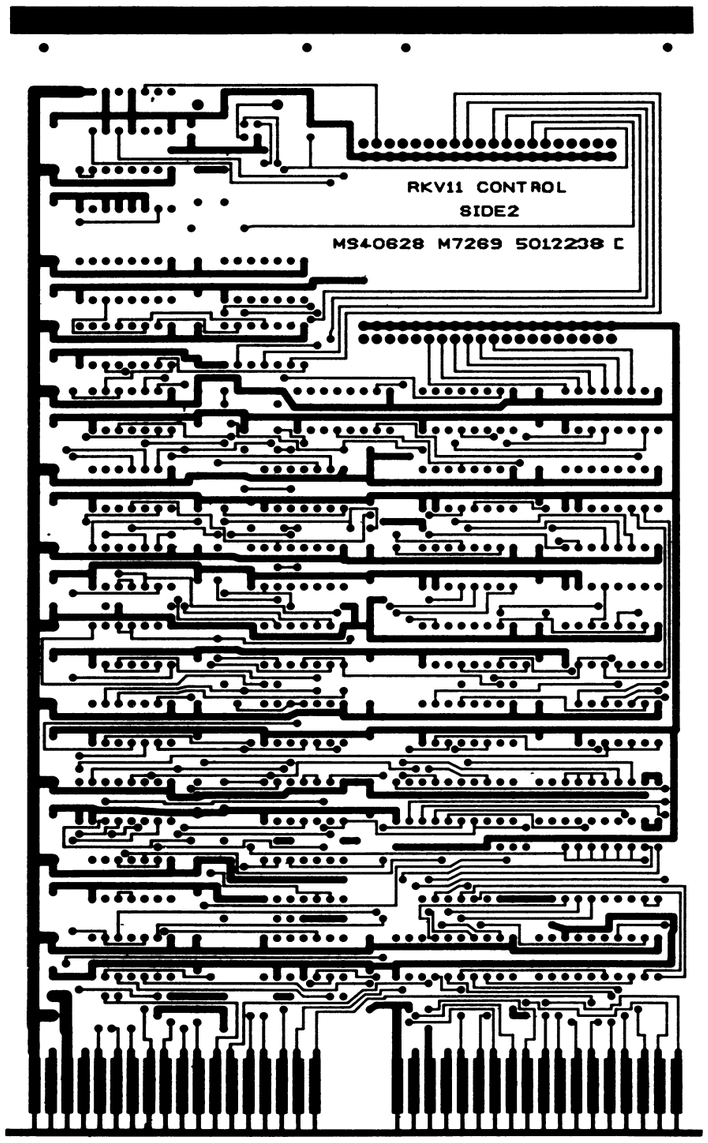
TITLE: RKVII CONTROL			SIZE: D	CODE: UA
SCALE: 2:1	SHEET: 2 OF 3		DIST	

NUMBER: M7269 -0-0 REV: C

DEC FORM NO DRD 137

DUA M7269 -2-0 C

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VIEWED FROM SIDE 2

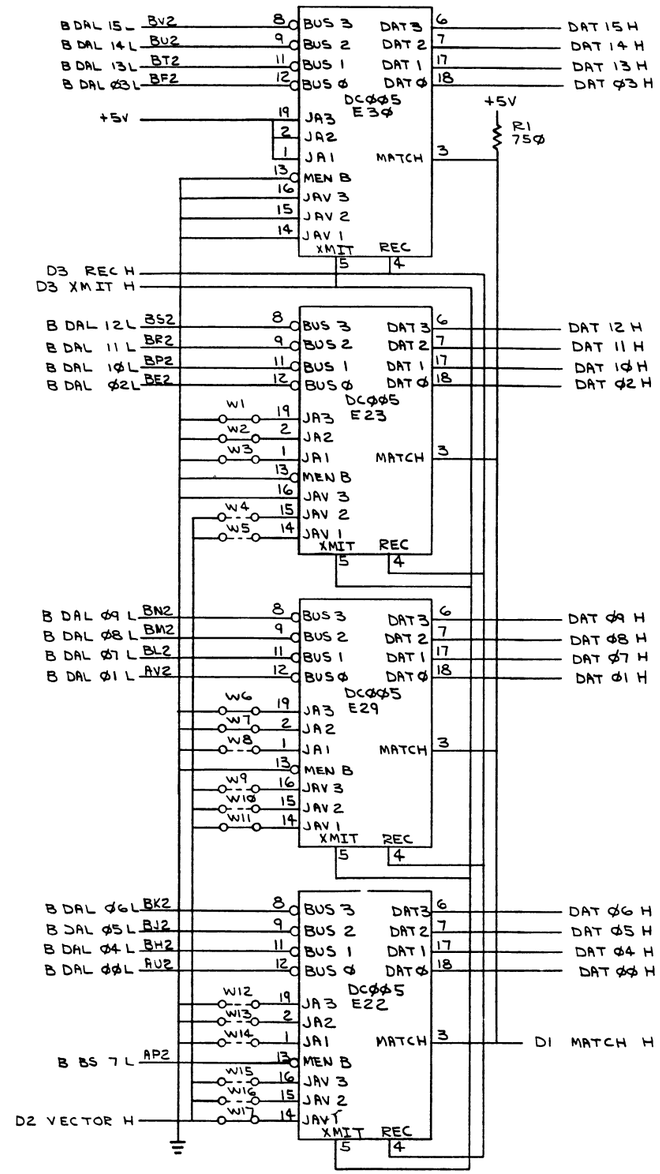
REVISIONS		
CHK	CHANGE NO	REV

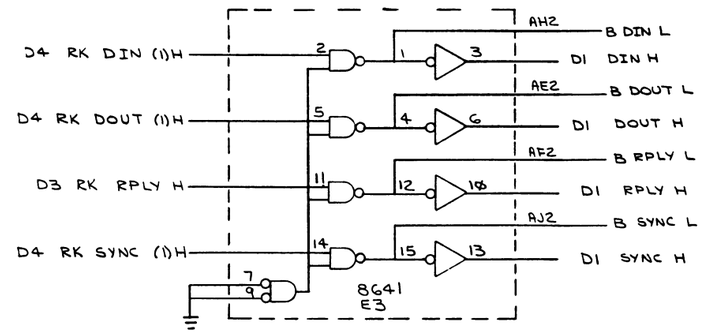
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RKVII CONTROL	D	UA	M7269 -0-0	C
SCALE 2:1 SHEET 3 OF 3	DIST			

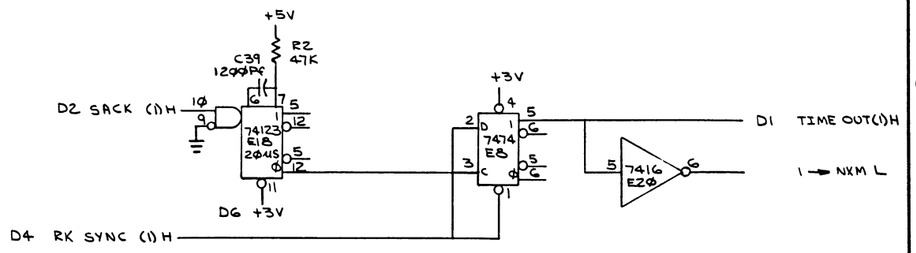
DEC FORM NO DRD 137

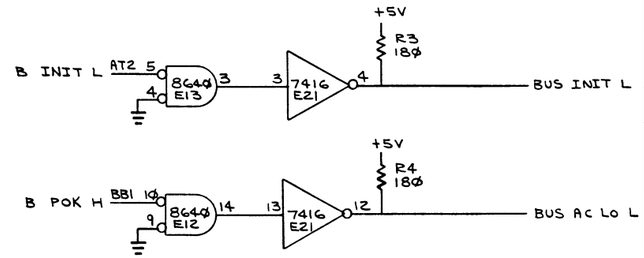
DUA M7269 -0-0 C

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AJ1, AM1, AT1, BJ1, BM1, BT1, AC2, BC2 — ⏚

+5V — AA2, BA2

NOTE: SUBSTUTION LIST FOR 74LSØØ - 74ÇÇ
74LS74 - 7474
74LSI74 - 74174

REVISIONS			
CHK	CHANGE NO.	REV.	
	M7269-00001	C	

DRN.		7-14-76
CHK'D		9/22/76
ENG.		9/23/76
PROJ. ENG.		10CT76
PROD.D Manager		10CT76
NEXT HIGHER ASSY.		
D-UA-M7269-0-D		
SCALE		
SHEET 1 OF 6		

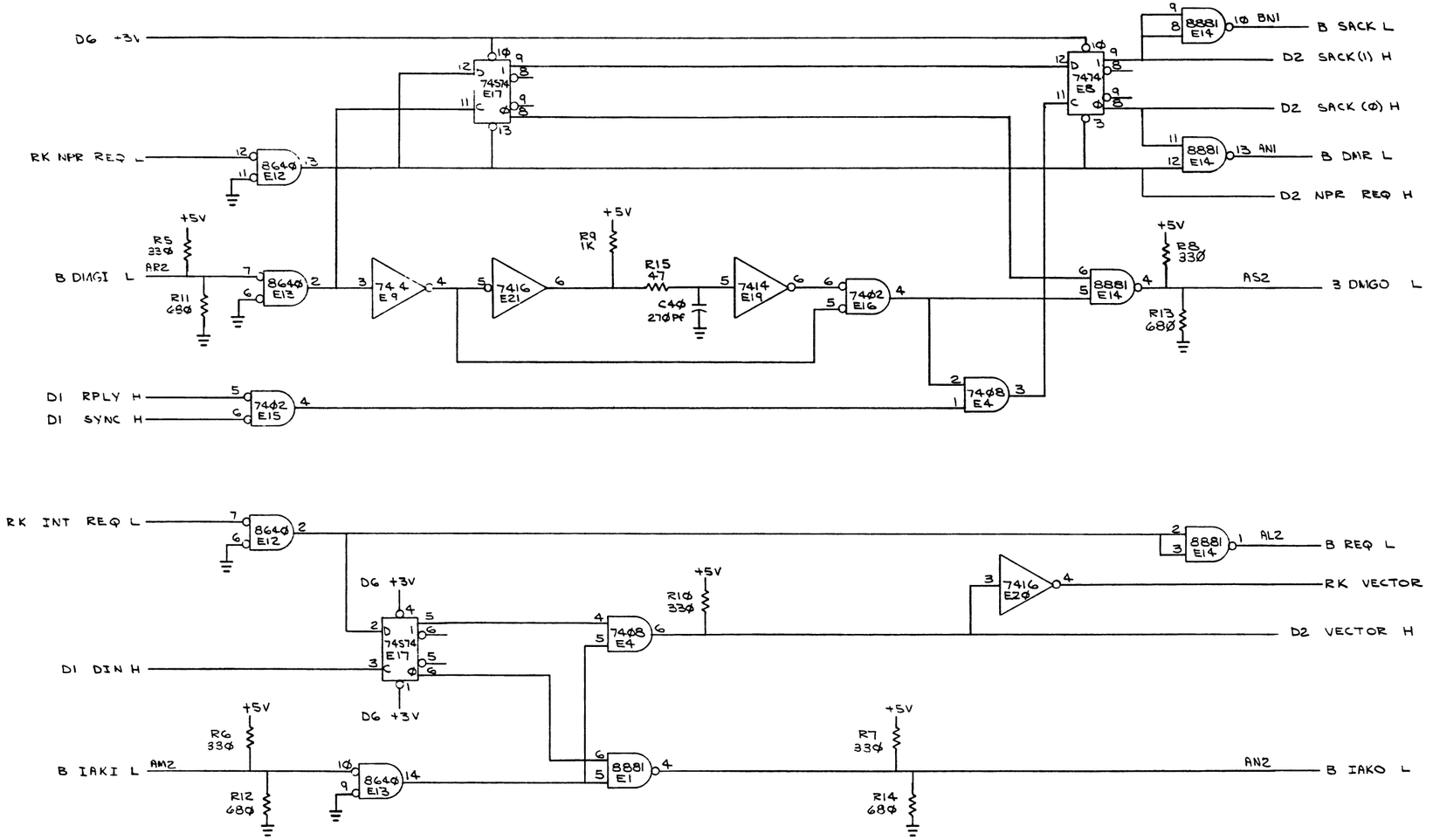
FIRST USED ON: RKVII-D — digital

TITLE: RKVII-D CONTROL (D1)

SIZE	CODE	NUMBER	REV.
D	CS	M7269-Ø-1	C

DIST.

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RKV11-D CONTROL (D2)	D	CS	M7269-0-1	C
SCALE — / — SHEET 2 OF 6	DIST			

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D4 NPR XMIT DATA (1) H

74174 E24
D5 R5(1)
DAT Ø3 H — D4 R4(1)
DAT Ø2 H — D3 R3(1)
DAT Ø1 H — D2 R2(1)
D1 MATCH H — DØ RØ(1)
DAT ØØ H — D1 R1(1)
CLR CLK
DG +3V
D1 SYNC H

7416 E31 → RKA Ø3 L
7416 E31 → RKA Ø2 L
7416 E31 → RKA Ø1 L

7408 E4 → D3 SYNC. SEL H

B WT BT L — AK2 — 8640 E13
D4 READ H

7400 E2 → 8881 E1 → STB HI BYT L
7400 E2 → 8881 E1 → STB LO BYT L
8881 E1 → B NTBT L (AK2)

D4 NPR XMIT ADD (1) H
D4 NPR XMIT DATA (1) L

7400 E5 → SEL ADD L
7402 E15 → DAT → RK L
D3 REC H
D3 XMIT H
D3 RK RPLY H

D1 DIN H — 7400 E5
D3 SYNC. SEL H — 7400 E5
D1 DOUT H — 7400 E5
D2 VECTOR H

7402 E16 → 7416 E21 → R18 1.8K +5V, R16 47, C41 1200 PF → 7414 E19 → 7408 E4

R19 1K +5V, R17 47, C42 270 PF → 7416 E21 → 7414 E19 → 7402 E16

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
RKV11-D CONTROL (D3)	D	CS	M7269-Ø-1	C
SCALE — SHEET 3 OF 6	DIST.			

REV C | CODE DCS | NUMBER M7269-Ø-1

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RK READ L

8640 E12

D4 READ H

74174 E9

7416 E2Φ

Φ → NPR L

DATA STR 2 L

D4 RK SYNC (1) H

D4 RK DIN (1) H

D4 RK DOUT (1) H

D4 NPR XMIT ADD (1) H

D2 NPR REQ H

DG +3V

7416 E11

23,97410D E1Φ

+3V

7474 E7

D4 STOP (1) H

D4 STOP (Φ) H

D2 SACK (Φ) H

D1 TIME OUT (1) H

7402 E15

D4 NPR XMIT DATA (1) H

D4 NPR XMIT DATA (1) L

D2 SACK (1) H

+5V

Q1 A05

L1 22 uh

R23 1K

R21 1K

C43 6.8PF

C44 39 PF

7414 E19

220 330

R26 1K

R22 1K

+5V

D2 SACK (Φ) H

D4 STOP (Φ) H

D4 STOP (1) H

7438 E6

D1 RPLY H

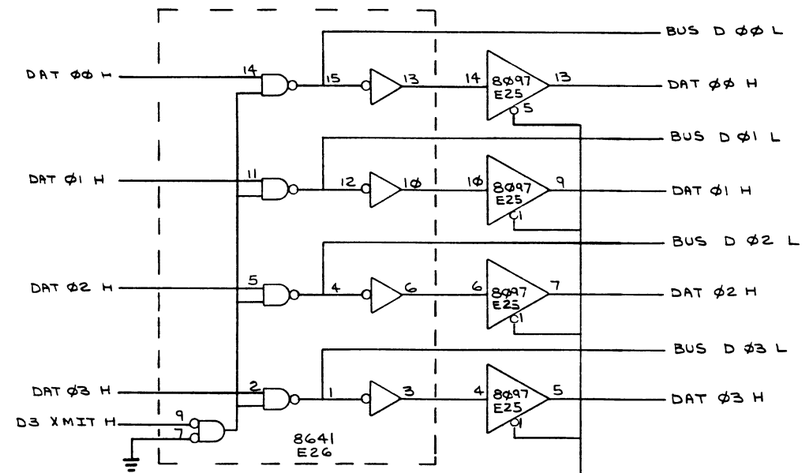
7414 E19

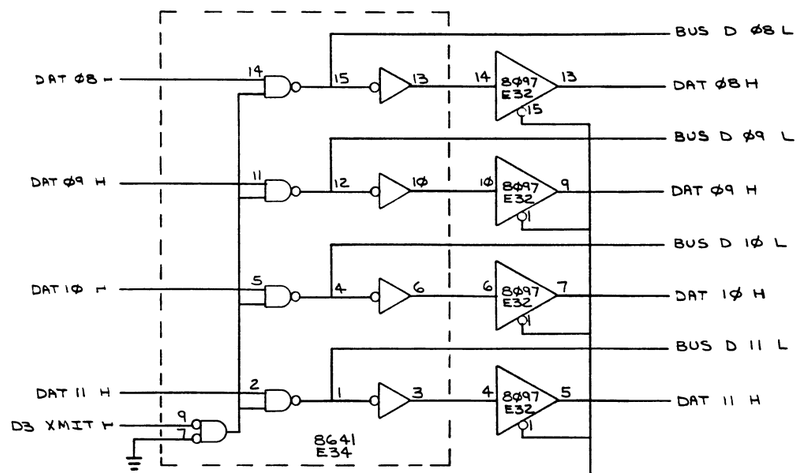
REVISIONS		
CHK	CHANGE NO	REV.

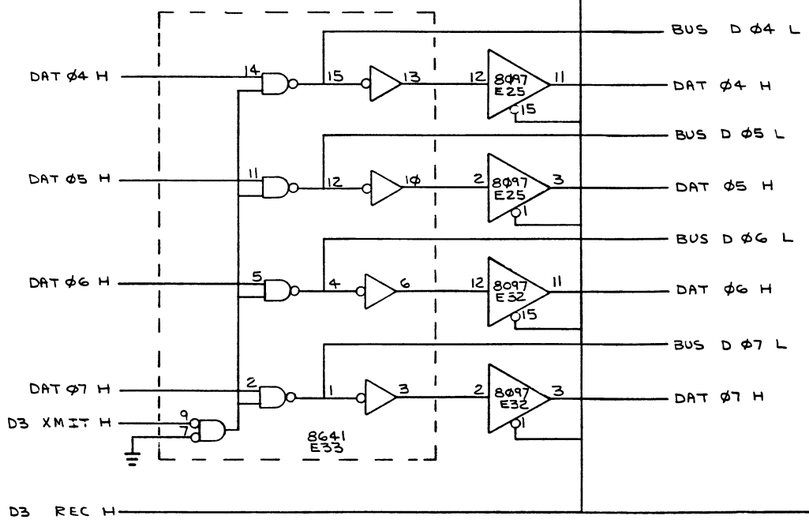
TITLE	SIZE	CODE	NUMBER	REV.
RKVII-D CONTROL (D4)	D	CS	M7269-Ø-1	C
SCALE	SHEET 4 OF 6	DIST.		

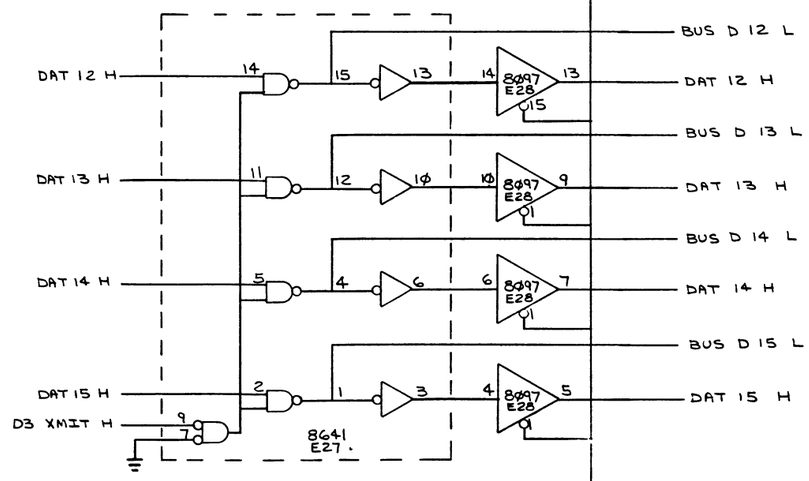
DCS M7269-Ø-1 REV C

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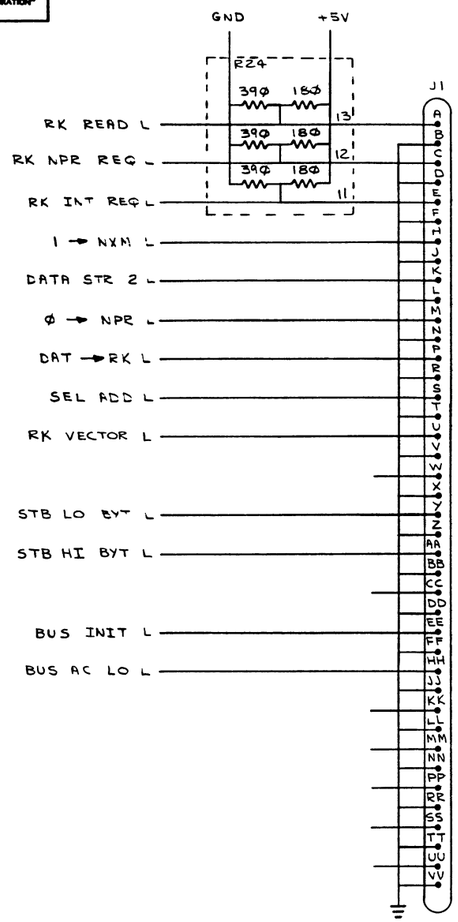


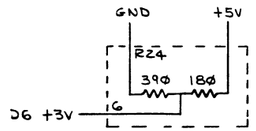
REVISIONS		
CHK	CHANGE NO	REV.

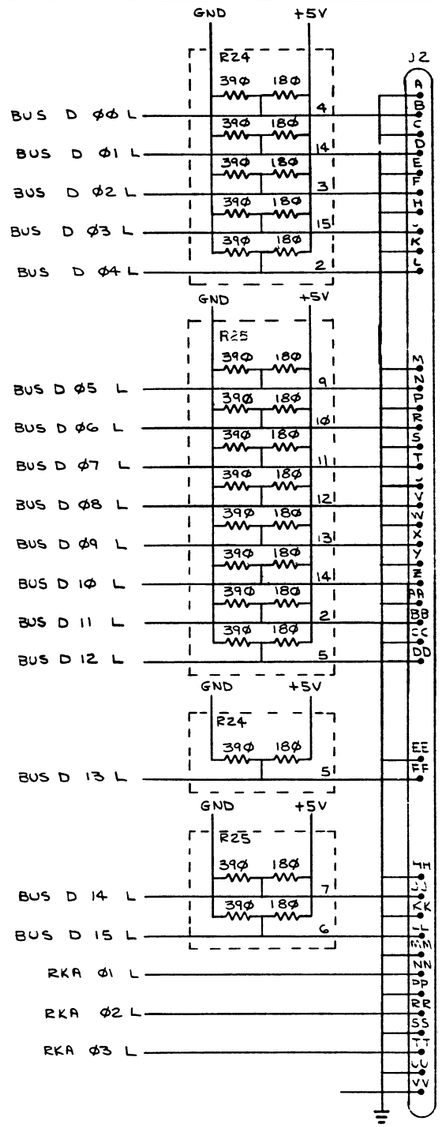
TITLE	SIZE	CODE	NUMBER	REV.
RKV11-D CONTROL (D5)	D	CS	M7269-Ø-1	C
SCALE —	SHEET 5 OF 6			

M7269-Ø-1 REV C

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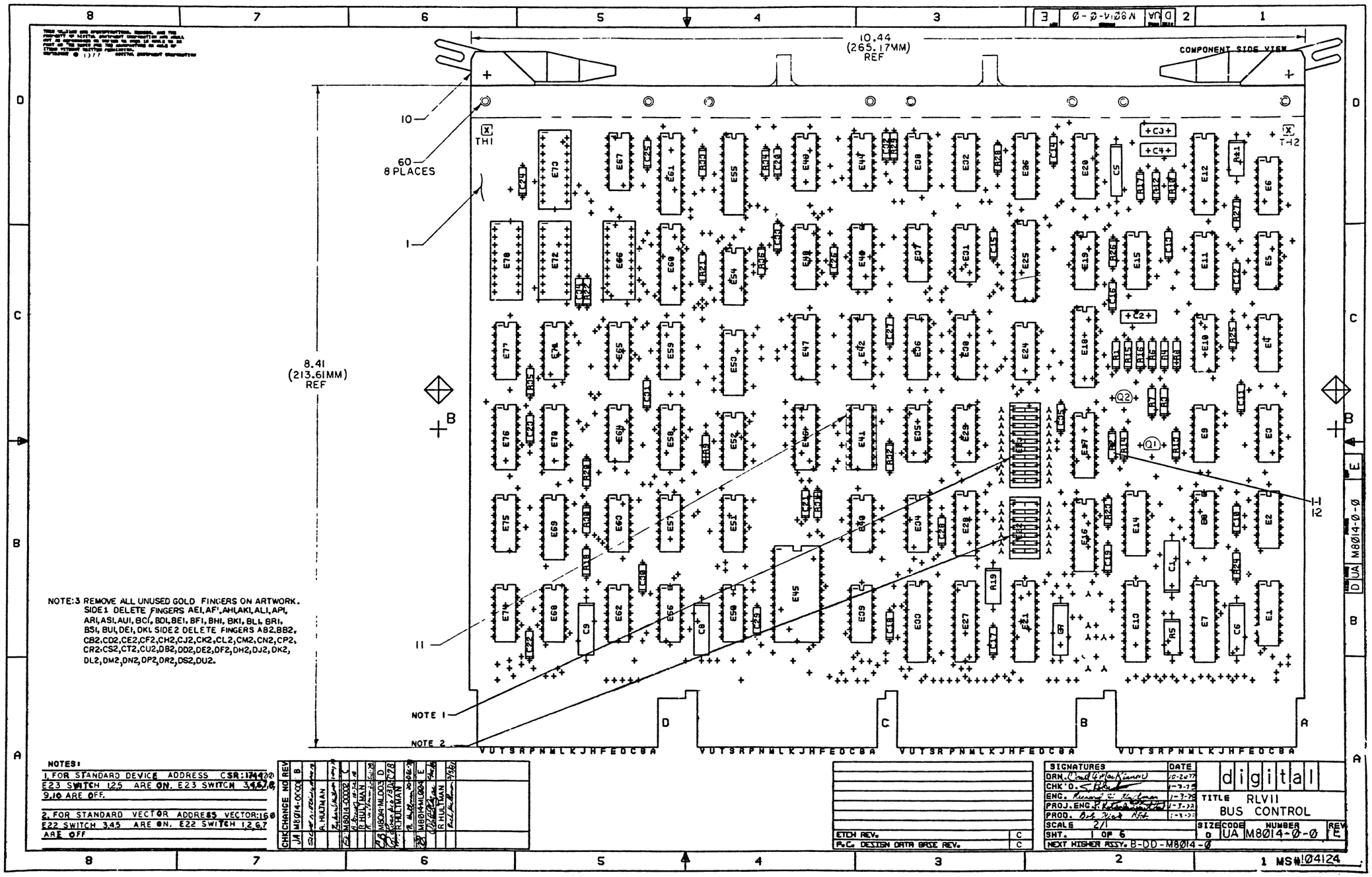




REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
RKVII-D CONTROL (D6)	D	DCS	M7269-Ø-1	C
SCALE — / — SHEET 6 OF 6	DIST.			

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NOTE:3 REMOVE ALL UNUSED GOLD FINGERS ON ARTWORK.
SIDE1 DELETE FINGERS AE1,AF1,AH1,AK1,AL1,AP1,
AR1,AS1,AU1,BC1,BD1,BE1,BF1,BH1,BK1,BL1,BR1,
BS1,BU1,DE1,DK1. SIDE2 DELETE FINGERS AB2,BB2,
CB2,CD2,CE2,CF2,CH2,CJ2,CK2,CL2,CM2,CN2,CP2,
CR2,CS2,CT2,CU2,DB2,DD2,DE2,DF2,DH2,DJ2,DK2,
DL2,DM2,DN2,DP2,DR2,DS2,DU2.

NOTES:
1. FOR STANDARD DEVICE ADDRESS CSR:174400
E23 SWITCH 1,2,5 ARE ON. E23 SWITCH 3,4,6,7,8,9,10 ARE OFF.

2. FOR STANDARD VECTOR ADDRESS VECTOR:160
E22 SWITCH 3,4,5 ARE ON. E22 SWITCH 1,2,6,7 ARE OFF

CHK	CHANGE NO	REV
JA	M8014-0000	B
	M8014-0002	C
	M8014-0003	D
	M8014-0004	E

ETCH REV.	C
P.C. DESIGN DATA BASE REV.	C

SIGNATURES	DATE
DRN.	10-20-77
CHK'D.	1-3-78
ENG.	1-3-78
PROJ. ENG.	1-3-78
PROD.	1-3-78

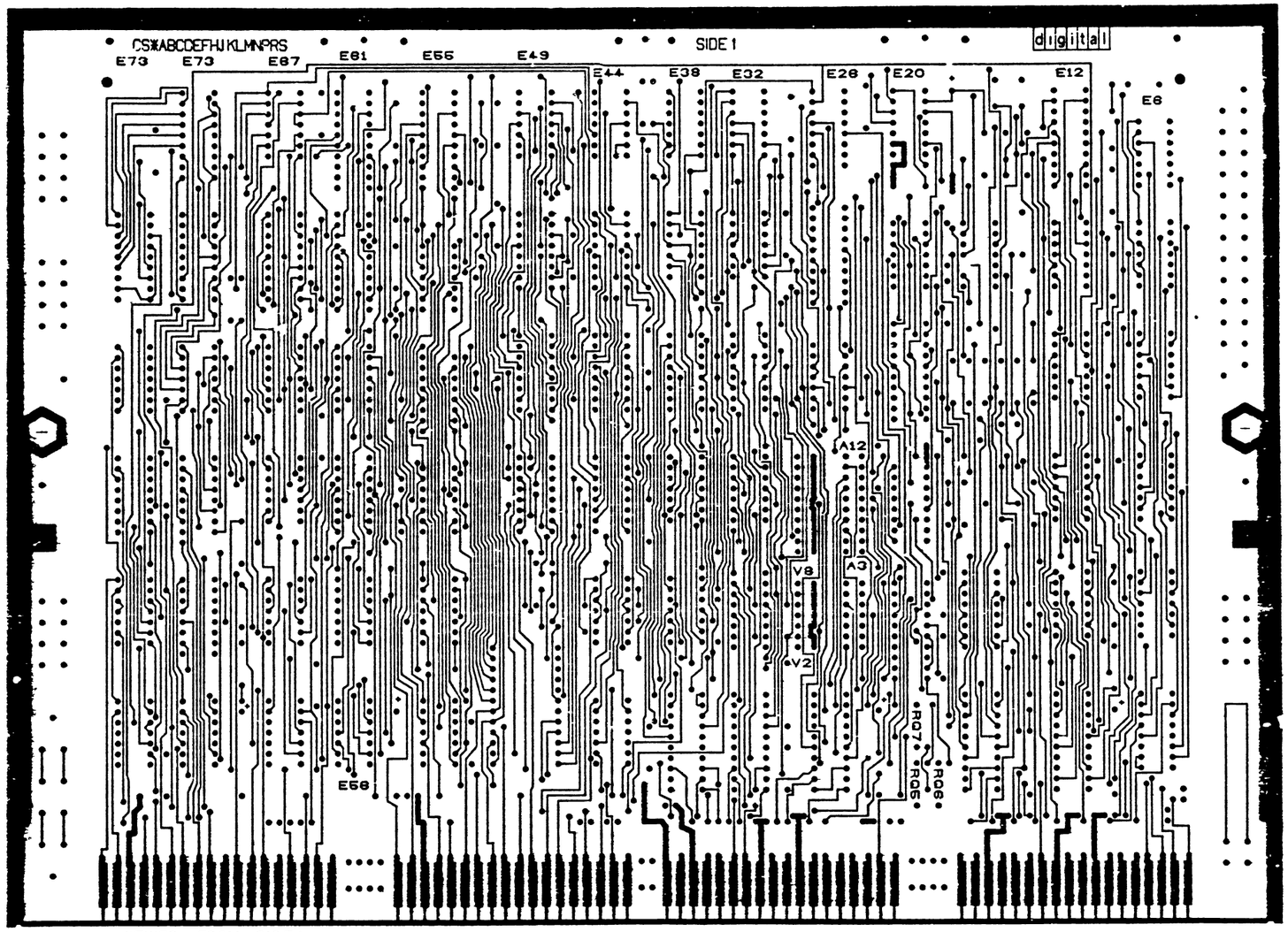
digital

TITLE RLVII
BUS CONTROL

SCALE 2/1
SHT. 1 OF 6
SIZE D | CODE UA | NUMBER M8014-0-0 | REV E
NEXT HIGHER ASSY. B-DD-M8014-0

MS#104124

LAYER 1



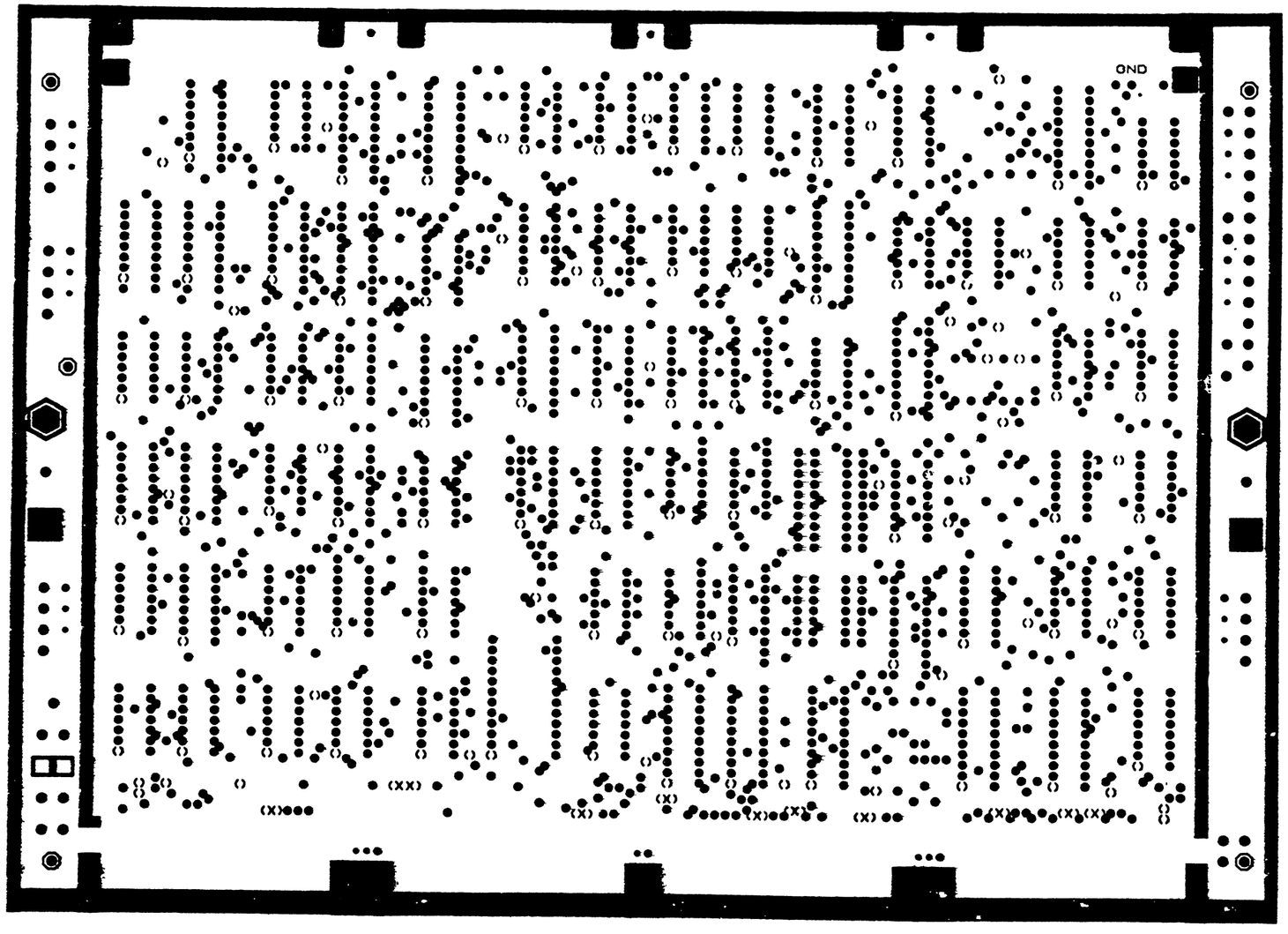
VIEWED FROM SIDE 1

REVISIONS			
CHK	CHANGE NO		

TITLE	SIZE	CODE	NUMBER	REV
RLVII BUS CONTROL	D	UA	M8014-0-0 -	E
SCALE	SHEET 2 OF 6			

DUAM8014-0 E

LAYER 2

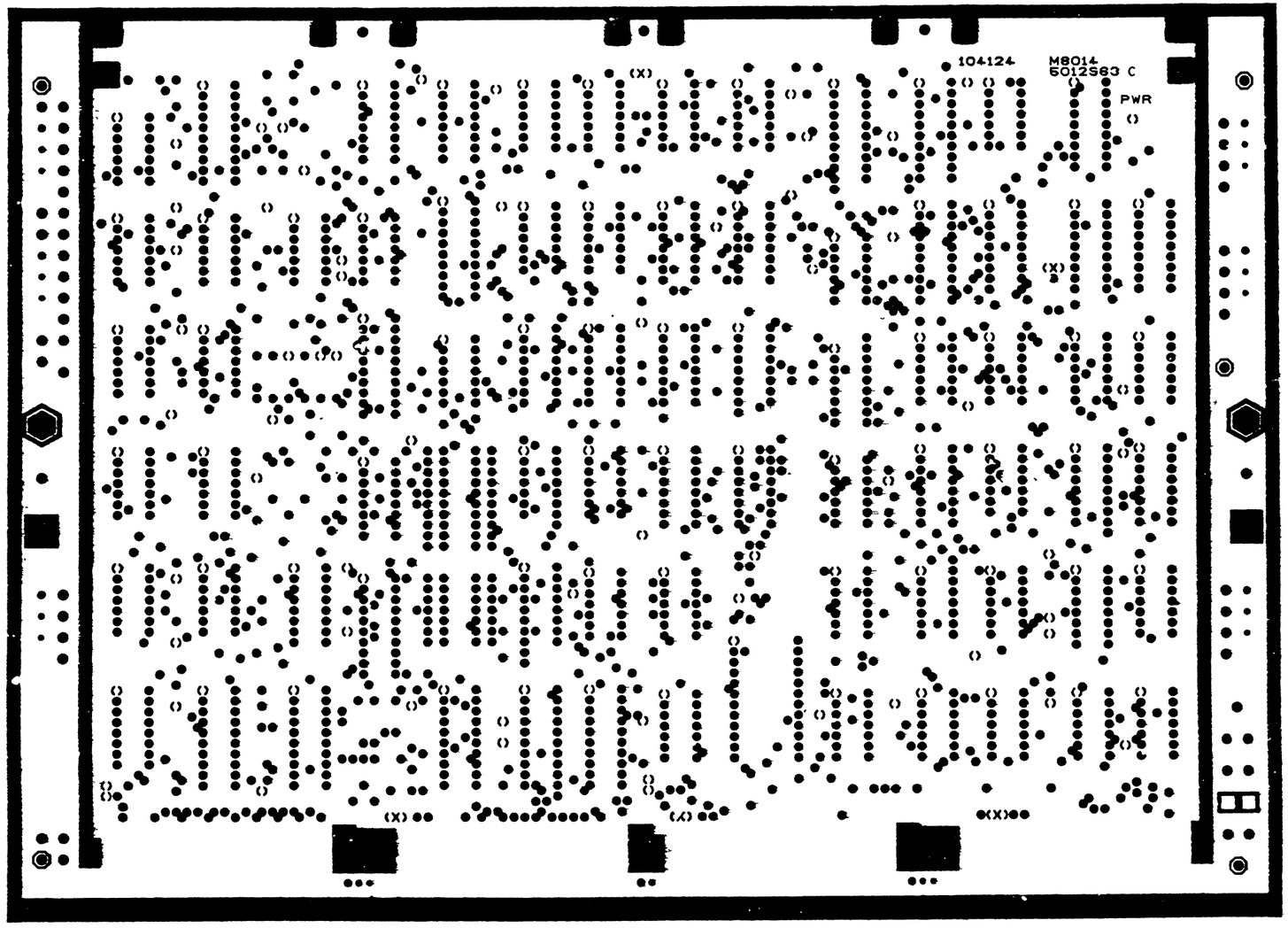


VIEWED FROM SIDE 1

REVISIONS		
CHR	CHANGE NO	BY

TITLE	RLVII BUS CONTROL
SCALE	2:1
SHEET	3 OF 6
SIZE	D
CODE	UA
DWG NO	M8014-0-0-
REV	E

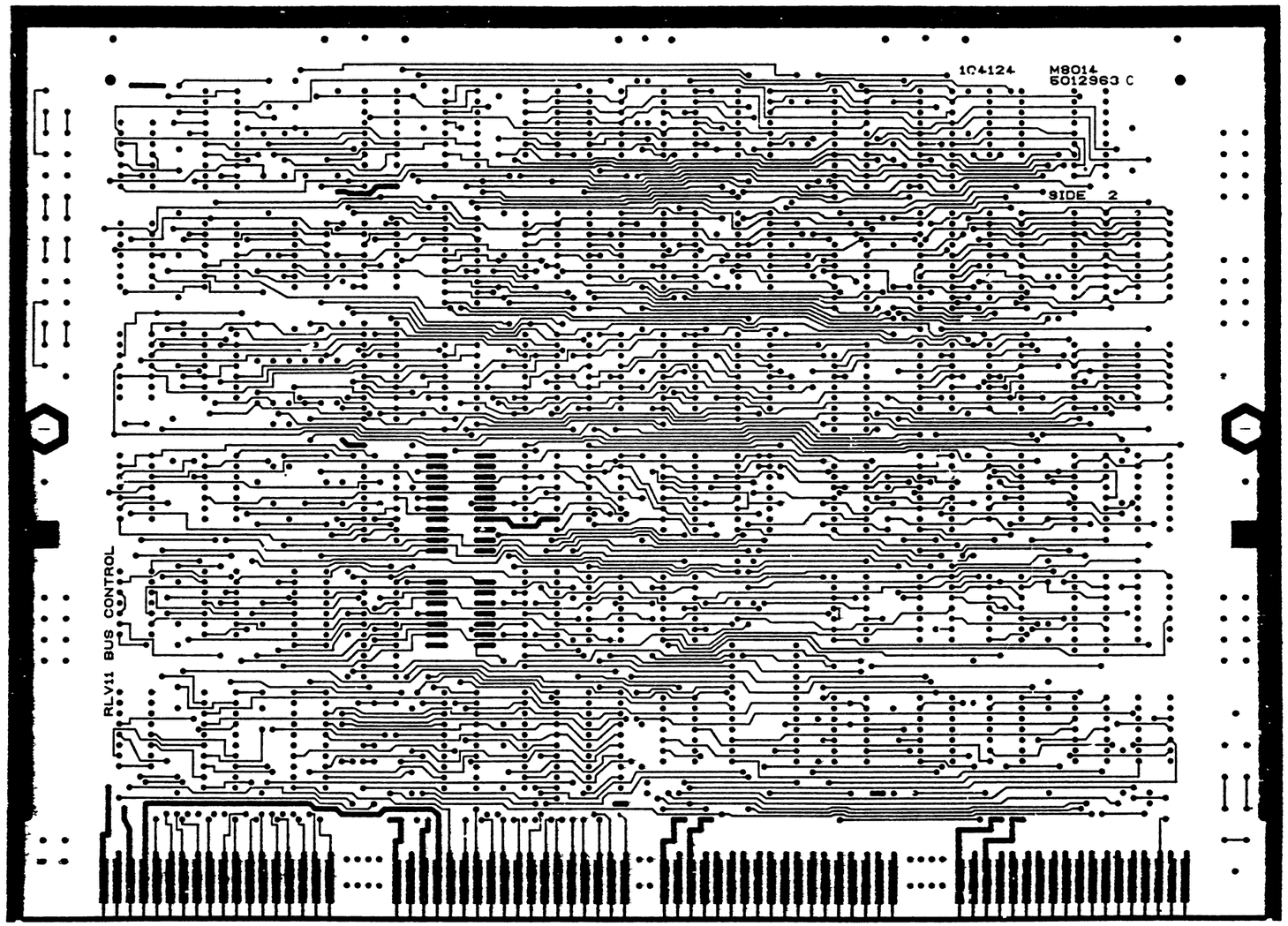
D UA M8014-0-0 E



VIEWED FROM SIDE2

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV
REVII BUS CONTROL	D	UA	M8214-A-B -	E
SCALE 2:1 SHEET 1 OF 6	DIST			



VIEWED FROM SIDE 2

REVISIONS		
CHK	CHANGE NO	BY

TITLE	SIZE	CODE	NUMBER	REV
RLV11 BUS CONTROL	D	UA	M8014-0-0	E
SCALE 2:1 SHEET 5 OF 6				

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REWORK INSTRUCTIONS:

E.CO #1:

COMPONENT DELETE SIDE 1:

1-1 DELETE R2, 3.3K (P/N. 1300439-00)

COMPONENT ADDS SIDE 1:

1-2 ADD R2, 1.1K (P/N 1301475-00)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLVII BUS CONTROL	D	UA	M8Ø14-0-0	E-
SCALE 2/1 SHEET 6 OF 6	DIST			

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BC5 DIS BUS XF (1) L
BCI GS RPLY H
BCI M RPLY H
BCI R SYNC H
BCI R RDOUT H
BCI R DIN H
B RPLY L
B SYNC L
B DOUT L
BDIN L
8641 E1
BC2 MATCH H
BC2 TS DAL 2 H
BC2 TS DAL 1 H
BC2 SC RDY (1) L
BC3 VEC TO BUS H
BUS PROTOCOL
BC5 DIS BUS XF (1) L
BCI G DIN H
BC5 LIMIT (1) H
BCI SEL CSR L
BCI SEL BA L
BCI SEL DA L
BCI GD OUT L
BCI SEL MP L
BCI WRT CSR L
BCI WRT CSR PLS H
BCI RD CSR L
BCI RD BA L
BCI WRT DA L
BCI WRT CSR PLS L
BCI WRT DA PLS L
BCI RD DA L
BCI RD FIFO L
BCI GS RPLY H
BCI G DOUT PLS L
BCI DAL REC H
BCI B P OK H
BCI P OK H
BCI MASTER L
DC2 NPR EN H
BC3 COMP ERR L
BC5 LIMIT (1) H
BC2 WC OFLW (0) H
BCI MASTER RPLY L
BCI B POK L
DMA CONTROL
BDMGI L
B DMGO L
B DMR L
BC3 INIT L
DEV SEL
MASTER H
BCI SYNCO H
BCI M DIN H
BCI EN ADD H
BCI M RPLY H
BCI EN DATA L
BCI MASTER RPLY L
BC5(B) HIGH
BC5(A) HIGH
BCI R SYNC H
BCI M RPLY H
BC3 IERDY H
BC2 DSK WRT H
BCI DSK WRT L
BC3 8.2 MHZ H
BC3 INIT H
BCI NXM (1) H
BC5(D) HIGH
BCI SYNCO H
WAITING
BCI NXM (1) H
BCI NXM (1) L
BC3 CLR ERR L
NXM DETECTION
BC5(C) HIGH
BCI DAL XMIT EN H
10µS MIN
BCI MRPLY H
BC3 INIT H
B SACK L
BWTBT L
BCI G EN ADD H

NOTE:
1. * MEANS REFERRING TO POINT ON D-CS-M8013-0-1.

REVISIONS			
CHK	CHANGE NO.	REV.	
JA	M8014-00001	B	
	M8014-00002	C	
	M8014 — M1004	D	

DRN.		7-21-77
CHK.		1-16-78
ENG.		1-2-78
PROJ. ENG.		1-6-78
PROD.		1-6-78
NEXT HIGHER ASSY.	D-UA-M8014-0-0	
SCALE		
SHEET	1 OF 5	

FIRST USED ON: RLVII
digital
TITLE: RLVII BUS CONTROL (BCI)
SIZE: D | CODE: CS | NUMBER: M8014-0-1 | REV: D
DIST.

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BUS XCVRS

DC005 E33

DC005 E27

DC005 E21

DC005 E13

WC/BA LO BYTE DC006 E18

WC/BA HI BYTE DC006 E25

8556 E17 XBA

8556 E47

8556 E46

8556 E36

8556 E28

DISK ADDRESS SERIALIZER 74150 E45

DISK ADDRESS REGISTER

E23 ON=1

E22 ON=1

74LS11 E11

74LS74 E35

74LS02 E51

7408 E56

74S04 E34

8881 E8

BCI SEL 8A L
BCI INIT L
BCI SEL MP L
BC5(1) HIGH
BC2 WC OFLW (1) H
BC2 WC OFLW (0) H
BC3 CLR ERR L
BCI RD CSR L
BCI WRT CSR L
BC2 INIT A H
BCI WRT CSR PLS H
BCI EN ADD H
BCI GEN ADD H
BCI RD BA L
BCI G DOUT PLS L
BCI EN ADD H
BCI RD DA L
BCI WRT DA L
BC5(F) HIGH
BC5(1) HIGH
+5V
BC3 VEC TO BUS H
BC2 MATCH H
(DC2) INC DA L
BCI WRT DA PLS L
BC3 INIT L
BCI DAL XMIT EN H
BCI DAL REC H
CP1 BC2 DA 1 H
CM1 BC2 DA 0 H
BCI INIT A H
10 CBI BC2 DA (1) L
10 ADI B DAL 17X
AC1 B DAL 16X

BOAL 13 L BT2
BOAL 12 L BS2
BOAL 11 L BR2
BOAL 14 L BU2
BOAL 10 L BP2
BOAL 9 L BN2
BOAL 8 L BM2
BOAL 15 L BV2
BOAL 7 L BL2
BOAL 6 L BK2
BOAL 5 L BJ2
BOAL 0 L AU2
BOAL 4 L BH2
BOAL 3 L BF2
BOAL 2 L BE2
BOAL 1 L AV2
BBS 7 L AP2

A12 A11 A10 A9 A8 A7 A6 A5 A4 A3
V8 V7 V6 V5 V4 V3 V2
R19 26.1K

BC2 TS DAL 13 H
BC2 TS DAL 12 H
BC2 TS DAL 11 H
BC2 TS DAL 14 H
BC2 TS DAL 10 H
BC2 TS DAL 9 H
BC2 TS DAL 8 H
BC2 TS DAL 15 H
BC2 TS DAL 7 H
BC2 TS DAL 6 H
BC2 TS DAL 5 H
BC2 TS DAL 0 H
BC2 TS DAL 4 H
BC2 TS DAL 3 H
BC2 TS DAL 2 H
BC2 TS DAL 1 H

BC5 BCNTA 3 H
BC5 BCNTA 2 H
BC5 BCNTA 1 H
BC5 BCNTA 0 H

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLV11 BUS CONTROL (BC2)	D	CS	M8014-0-1	D
SCALE —	SHEET 2 OF 5	DIST		

DEC FORM NO. DRD 128

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INTERUPT CONTROL
DC203 E16
BC3 IE RDY H
BIAK I L AM2
B INIT L AT2
BCI R DIN L
+5V
R15 330
R16 680
R23 1K
RQSTA
BIAKI
BINIT
BDIN
RQSTB
ENA DAT
ENB DAT
ENA CLK
ENB CLK
ENA ST
BIRQ
BIAKO
INITO
VECTOR
VEC RQST
ENB ST
AN2 BIAKO L
BC3 INIT L
BC3 VEC TO BUS H
R13 330
R14 680
BC5(B)HIGH
BC3 IERDY H
BC3 C RDY(I) H
BC3 INIT H
74LS174 E10
74LS02 E5
BCI WRT CSR PLS H
74LS174 E26
R20 10K
R21 10K
R22 10K
BC2 TS DAL 1 H
BC2 TS DAL 2 H
BC2 TS DAL 3 H
BC2 TS DAL 6 H
BC2 TS DAL 8 H
BC2 TS DAL 9 H
D3 D2 D1 DØ D4 D5 CLK CLR
R3(I) R2(I) R1(I) RØ(I) R4(I) R5(I)
CVI BC3 FO (I) H
DCI BC3 F1 (I) H
DDI BC3 F2 (I) H
CEI BC3 DRV SEL Ø (I) H
CCI BC3 DRV SEL 1 (I) H
8097 E70
BCI RD CSR L
DC2 SET C RDY L DHI
74LS08 E52
BC5(G) HIGH
BC3 COMP ERR H
74LS74 E63
DFI
BC3 C RDY (I) H
BC3 C RDY (I) L
BCI WRT CSR PLS L
BCI TS DAL 7 H
74LS32 E29
74Ø8 E56
74LS04 E62
12 CRI
BC3 CLR ERR H
BC3 CLR ERR L
BC3 C RDY(I) H
DC5 DRV ERR H CHI
DC3 CRC ERR(I) H DLI
BCI NXM (I) L
74LS51 E40
74LS10 E44
74LS04 E49
BC3 COMP ERR L
BC3 COMP ERR H
BC2 TS DAL 15 H
DC5 DRIVE READY H DT2
BC2 TS DAL Ø H
+5V
R17 180K
C5 6.8UF
DC2 INC DA L DBI
74LS123 E20
DC2 DLT L CUI
74LS08 E52
DC3 PRESET OPI L DMI
74 LS109 E69
BC5(G) HIGH
BC3 CLR ERR L
BCI NXM (I) H
BC2 TS DAL 13 H
BC2 TS DAL 11 H
BC2 TS DAL 14 H
BC2 TS DAL 7 H
BC2 TS DAL 10 H
BC2 TS DAL 12 H
BC3 INIT H
BC3 SCRDY(I) L
74LS74 E15
BCI R SYNC L
BC5(C) HIGH
DC3 MIS MATCH L CKI
74LS22 E51
74LS04 E9
74LS04 E30

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLVII BUS CONTROL (BC3)	D	CS	M8014-Ø-1	D
SCALE —	SHEET 3 OF 5	DIST.		

DEC FORM NO. DRD 128

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BC1 RD FIFØ L
BC1 EN DATA L
74LSØØ E5Ø

BC5 ED BIN H
BC1 MDIN H
BC5 LD BCNT PLS L
FIFO OUTPUT BUFFER

74LS295 E65: BC2 TS DAL 8 H, BC2 TS DAL 9 H, BC2 TS DAL 1ØH, BC2 TS DAL 11 H
74LS295 E31: BC2 TS DAL 4 H, BC2 TS DAL 5 H, BC2 TS DAL 6 H, BC2 TS DAL 7 H
74LS295 E77: BC2 TS DAL 6 H, BC2 TS DAL 1 H, BC2 TS DAL 2 H, BC2 TS DAL 3 H
74LS295 E38: BC2 TS DAL 12 H, BC2 TS DAL 13 H, BC2 TS DAL 14 H, BC2 TS DAL 15 H
74LS295 E84: BC2 TS DAL 8 H, BC2 TS DAL 9 H, BC2 TS DAL 1ØH, BC2 TS DAL 11 H
74LS295 E54: BC2 TS DAL 4 H, BC2 TS DAL 5 H, BC2 TS DAL 6 H, BC2 TS DAL 7 H
74LS295 E71: BC2 TS DAL Ø H, BC2 TS DAL 1 H, BC2 TS DAL 2 H, BC2 TS DAL 3 H

FIFO INPUT BUFFER
BC5(L) HIGH
BC5(E) HIGH
BC5(L) HIGH
BC5(F) HIGH
BC5(G) HIGH
BC5(M) HIGH
BC5(C) HIGH

BC4 TS FIFO Ø H
BC4 TS FIFO 1 H
BC4 TS FIFO 2 H
BC4 TS FIFO 3 H
BC4 TS FIFO 4 H
BC4 TS FIFO 5 H
BC4 TS FIFO 6 H
BC4 TS FIFO 7 H
BC4 TS FIFO 8 H
BC4 TS FIFO 9 H
BC4 TS FIFO 1ØH
BC4 TS FIFO 11 H
BC4 TS FIFO 12 H
BC4 TS FIFO 13 H
BC4 T3 FIFO 14 H
BC4 TS FIFO 15 H

BC5 ED BIN H
BC1 M DIN H
74LS295 E32: BC2 TS DAL 12 H, BC2 TS DAL 13 H, BC2 TS DAL 14 H, BC2 TS DAL 15 H
BC5(E) HIGH

(RD/WRT ADDR CNTR)
DCØØ6 E6Ø
74LSØ4 E49
BC3 CLR ERR L
BC5 INC RA H
BC5(M) HIGH
BC5 ED RAM L
BC5 WRT RAM L

2111A2 E78
2111A2 E66
2111A2 E73
2111A2 E72

BC5(G) HIGH
DC5 SER DATA IN H
(SAVE)
74LS74 E68
BC3 INIT L

WRT/RD SHIFT REGISTER
74LS299 E55 ODD
74LS299 E61 EVEN
BC5(K) HIGH
BC5(J) HIGH
BC5 SR LD EN H
BC4 BCNTA Ø L
74LSØ4 E34
BC3 INIT L
BC5 WRT RAM L
DC2 DSK WRT H (DJ1)
BC5 BCNTA ØH

BC4 BCNTA Ø L
74LS51 E67
74LS27 E57
BC5 WRT EMPTY Ø H
DC WRT DATA AREA L
BC4 SER DATA OUT H

(FIFO BUFFER)

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE	CODE	NUMBER	REV.
RLV11 BUS CONTROL (BC4)		D	CS	M8014-Ø-1	D
SCALE	SHEET 4 OF 5	DIST			

DEC FORM NO. DRD 132

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AC2 BC2 CC2 DC2 AJ1 BJ1 AM1 BM1 AT1 BT1 CT1 DT1

AD2 BD2 +12V

AA2 BA2 CA2 DA2 BV1 +5V

BC5(G) HIGH

DC2 EN WRT RAM H DS1 — 74LS74 E68 — BC3 CLR ERR L

BC1 DSK WRT L — 74LS74 E35 — BC5(I) HIGH

74LS51 E67 — BC5 WRT RAM L

74LS32 E29

74LS175 E43

BC5 BCNTA 2 H
BC5 BCNTA 1 H
BC5 BCNTA 0 H
BC5 BCNTA 3 H

D0 R0(1) — BC5 SR LD EN H
D1 R1(1) — BC5 SYNK H
D2 R2(1) — BC5 SYNK L
D3 R3(1)
CLK CLR

74LS10 E44

74LS11 E74

232184I E41 — A0 A1 A2 A3 A4 — D1 D2 D3 D4 D5 D6 D7 D8

74161 E46 — D0 D1 D2 D3 — R0(1) R1(1) R2(1) R3(1) — CLR LD CLK CNT EN CRY EN CO CE

DSK WRT H (DJ1) DC2 *

DC1 CLK BC H CF1 — 74S04 E34 — DC1 BC ENAB H — BC5(H) HIGH

BC3 CLR ERR L — (DB1) DC2 INC DA L — (CJ1)

74LS175 E42 — BC1 WRT DATA AERA L (DH1)

D0 R0(1) — BC5 ED RAM H
D0 R0(0) — BC5 ED RAM L
D1 R1(1) — BC5 WRT INC RA H
D1 R1(0)
D2 R2(1) — BC5 ED BIN H
D2 R2(0)
D3 R3(1) — BC5 MAX MIN L
D3 R3(0)
CLK CLR

74LS04 E62 — BC1 WRT EMPTY (0) L

74LS20 E39

74LS00 E39 — BC5 LD BOUT PLS L

74LS00 E75 — BC5 MAX MIN L

BC5(F) HIGH — 74LS74 E37 — BC5 LIMIT (I) H — BC5 LIMIT (I) L

74LS00 E75 — 74LS00 E75 — S DR1 — BC5 RAM STATUS H

BC5 SYNK L
BC3 CLR ERR L
DC2 MAINT H DV1 — 74LS04 E62

BC5(F) HIGH — 74LS74 E37 — BC5 WRT EMPTY (0) L — BC5 WPT EMPTY (0) H

BC3 INIT L

BC1 DSK WRT L
BC2 WCO FLW (1) L — 74LS02 E51 — 74LS02 E51 — DC2 DSKWRT H — DJ1 — 74LS51 E40

74LS00 E75 — BC5 INC RA H

74191 E58 — MAX/MIN RCLK D3 D2 D1 D0 — R3(1) R2(1) R1(1) R0(1) — LD DN/UP CLK ENB

BC5 EN ROM L

74191 E53 — MAX/MIN RCLK D3 D2 D1 D0 — R3(1) R2(1) R1(1) R0(1) — LD DN/UP CLK ENB

FIFO WORD COUNTER

BC3 CLR ERR L
BC5 ED RAM H

R18 1K — +5V — 74LS04 E62 — BC5 EN ROM L

DC2 DSK WRT H (DJ1)
DC2 MAINT H (DV1)
BC3 C RDY (1) H — 74LS27 E57 — BC2 WC OFLW (1) H (DD1)

74LS00 E50 — 74LS08 E52 — BC1 MASTER R-PLY L — BC1 RD FIFO L

BC3 CLR ERR L — 74S74 E59 — BC5 DIS BUS XF (1) H — BC5 DIS BUS XF (1) L — BC5 SYNK H — BC5 EN RAM XF (1) H

7408 E56

+5V — C10 – C35 .047UF — C6 – C9 6.8UF

+5V — R24 1K … R36 1K

BC5(A) HIGH — BC5(B) HIGH — BC5(C) HIGH — BC5(D) HIGH — BC5(E) HIGH — BC5(F) HIGH — BC5(G) HIGH — BC5(H) HIGH — BC5(I) HIGH — BC5(J) HIGH — BC5(K) HIGH — BC5(L) HIGH — BC5(M) HIGH

BC5 LIMIT (I) L — 74S04 E34

REVISIONS

CHK	CHANGE NO	REV

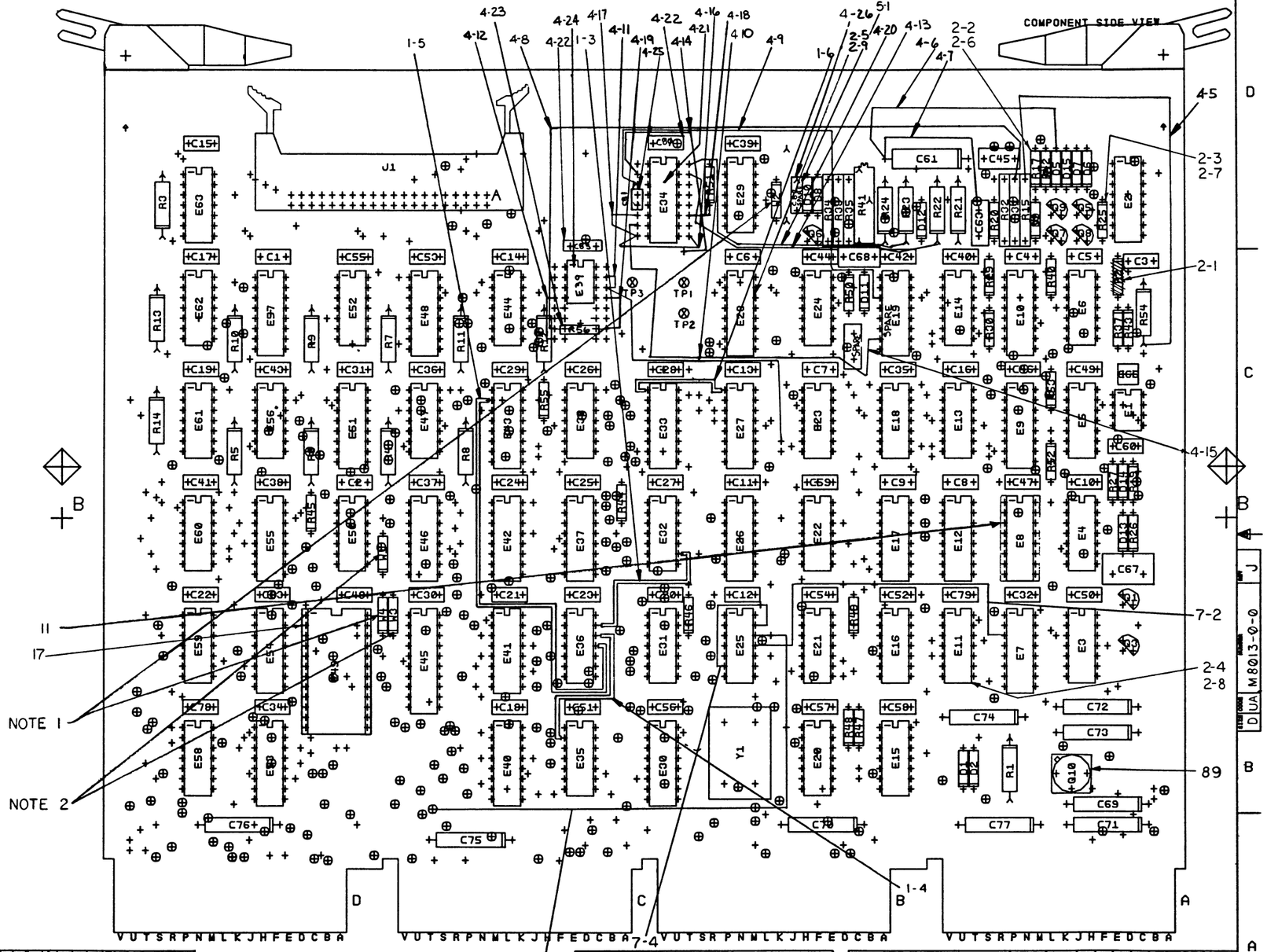
(FIFO COUNTROL)

TITLE	SIZE	CODE	NUMBER	REV.
RLV11 BUS CONTROL (BC5)	D	CS	M8014-0-1	D
SCALE —	SHEET 5 OF 5	DIST		

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M8013-0-0 D UA J

COMPONENT SIDE VIEW



NOTES:
PART SUBSTITUTION LIST:
23-017E2-00 : E49 PREFERRED
23-058B7-00 : E49 SUBSTITUTE
1. WHEN USING 23-017E2-00 FOR E49 REMOVE W2 & W4 (W1 & W3 INSERTED)
2. WHEN USING 23-058B7-00 FOR E49 REMOVE W1 & W3 (W2 & W4 INSERTED)

CHK	CHANGE NO	REV
	M8013-0-0001	C
R.HULTMAN	M8013-ML002	D
R.HULTMAN	M8013-ML003	E
R.HULTMAN	M8013-ML004	F
R.HULTMAN	M8013-ML5	H
R.HULTMAN	M8013-ML6	J
M. CARICH		

SIGNATURES	DATE
DRN. R Nichols	10-10-77
CHK'D. Bill Mahoney	11-1-77
ENG. Richard Hoffman	1-3-78
PROJ.ENG. Kirk Peterson	1-3-78
PROD. Bob Mark R.M.	1-3-78
SCALE 2/1	
SHT. 1 OF 4	
NEXT HIGHER ASSY. B-DD-M8013-0	

ETCH REV. C
P.C. DESIGN DATA BASE REV. CL

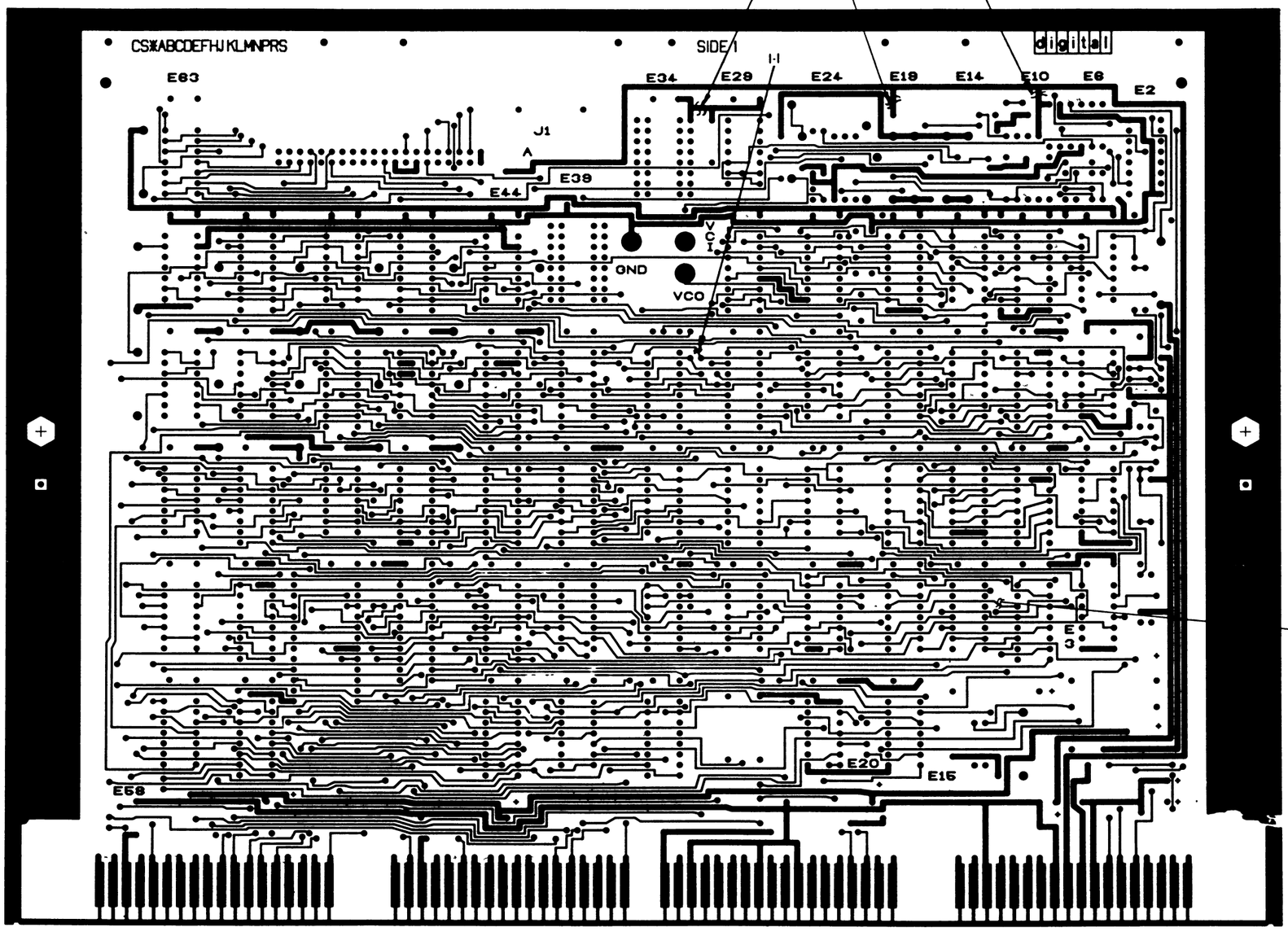
digital

TITLE
RLVII DISK CONTROL

SIZE	CODE	NUMBER	REV
D	UA	M8013-0-0	J

MS# 104123

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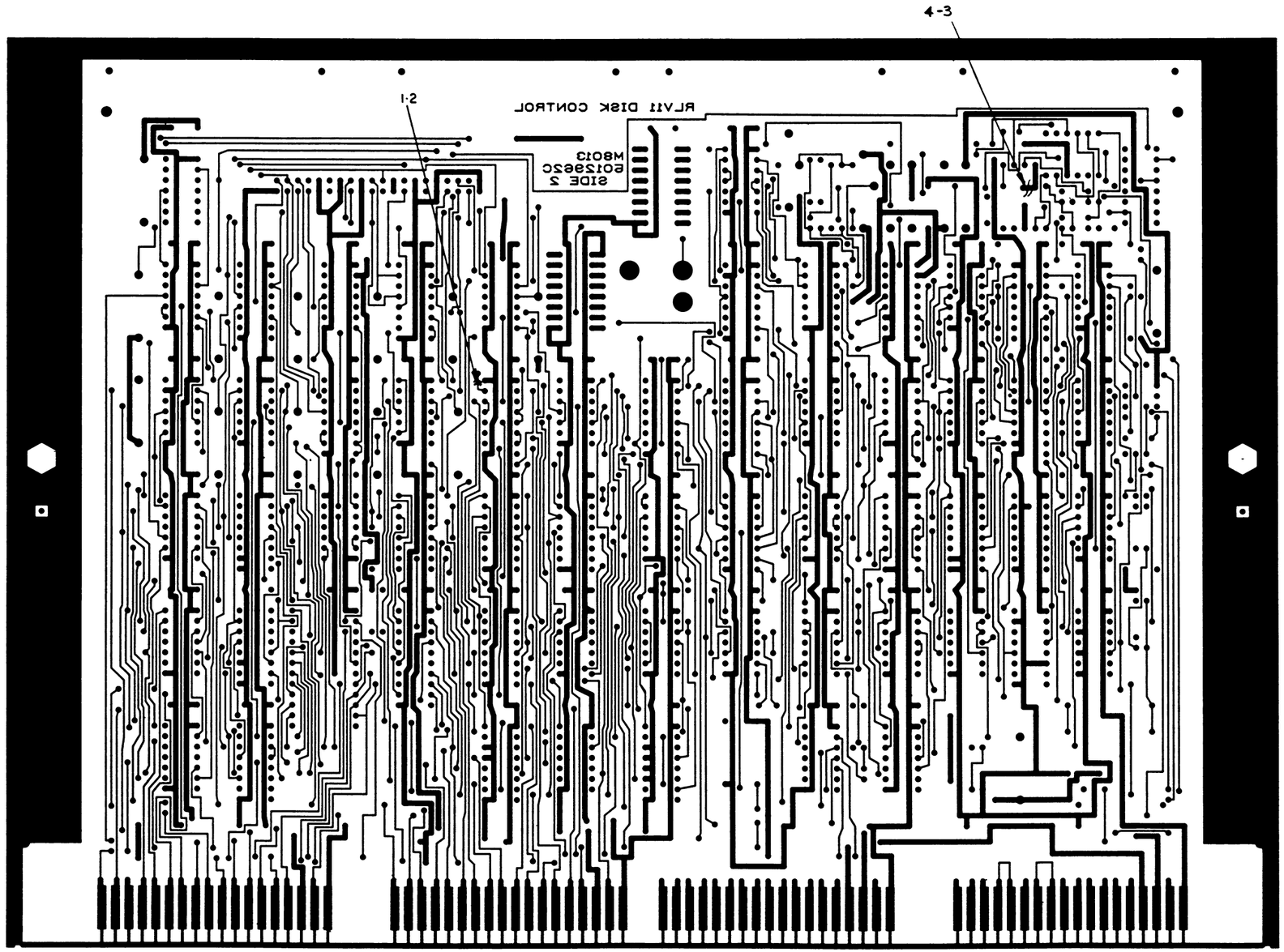
VIEWED FROM SIDE 1

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
RL V11 DISK CONTROL	D	UA	M8013-0-0	J
SCALE 2:1 SHEET 2 OF 4	DIST			

D UA M8013-0-0 J

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VIEWED FROM SIDE 1

REVISIONS		
CHK	CHANGE NO	REV

TITLE: RL V11 DISK CONTROL		CODE: D UA	NAME: M8013-0-0
SCALE 2:1	SHEET 3 OF 4	DIST	REV J

D UA M8013-0-0 J

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REWORK INSTRUCTIONS:

E.C.O.#1

ETCH CUTS SIDE 1:

1-1. BETWEEN E33-1 AND PTH TO THE RIGHT OF E33-16.

ETCH CUTS SIDE 2:

1-2. BETWEEN E43-2 AND PTH ABOVE AND TO THE LEFT OF E43-1

WIRE ADDS SIDE 1:

1-3. FROM E32-9 TO E36-13
1-4. FROM E35-2 TO E36-12
1-5. FROM E43-2 TO E36-11
1-6. FROM E33-1 TO E27-1

ECO #2

COMPONENT DELETES SIDE 1

2-1. R2, 330Ω (P/N, 13-00295-00)
2-2. R17, 180Ω (P/N, 13-01322-00)
2-3. R25, 470Ω (P/N, 13-00316-00)
2-4. E11, 7437 (P/N, 1910091-00)
2-5. E28, 74S112 (P/N, 1910545-00)

COMPONENT ADD SIDE 1

2-6 R17, 100Ω (P/N, 13-00229-00)
2-7 R25, 220Ω (P/N, 13-00271-00)
2-8 E11, 74S37 (P/N, 1912746-00)
2-9 E28, 74LS112 (P/N, 1912834-00)

ECO #4

ETCH CUTS

4-1 CUT ETCH AT LEFT SIDE OF C61, SIDE 1.
4-2 CUT ETCH AT LINE TO R17 AND R15, AT TOP OF R17, SIDE 1.
4-3 CUT ETCH AT LINE FROM TOP OF R15 TO FEED THRU UNDER R31, SIDE 2.
4-4 CUT ETCH AT E34-16 BETWEEN E34 AND R51 NEAREST R51, SIDE: 1.

WIRE ADDS:

4-5 BOTTOM OF R54 TO TOP OF R15.
4-6 TOP OF D5 (ANODE) TO LEFT SIDE OF C61 (TWO WIRES, REF: REWORK STEP 4-7).
4-7 LEFT SIDE OF C61 TO TOP OF C63 (REF: REWORK STEP 4-6).
4-8 TOP OF R31 TO E39 LOCATION, PIN 7 (REF: REWORK STEP 4-23).
4-9 E19 LOCATION, PIN 3 TO E34 LOCATION, PIN 3 (ROUTE WIRE UP BETWEEN R34 AND R33 THEN LEFT OVER R29 AND E34.)
4-10 FEED THRU TO THE LEFT OF E23, PIN 6 TO E39 LOCATION, PIN 14 (ROUTE WIRE UP TO C7 THEN LEFT TO C26 THEN UP) (TWO WIRES, REF: REWORK STEP 4-11).
4-11 E39 LOCATION, PIN 14 TO E39 LOCATION, PIN 15 (REF: REWORK STEP: 4-10).
4-12 E39 LOCATION, PIN 4 TO E39 LOCATION, PIN 8.
4-13 BOTTOM OF R22 TO E34, PIN 15 (ROUTE WIRE BELOW R41 AND E29).
4-14 E34 PIN 2 TO VC1 AT FEED THRU BELOW E34, PIN 9 (ROUTE WIRE ABOVE E34 THEN DOWN TO FEED THRU).
4-15 E34, PIN 7 TO E19 LOCATION, PIN 7.
4-16 E34, PIN 8 TO E34, PIN 9 (TWO WIRES, REF: REWORK STEP 4-17).
4-17 E34, PIN 8 TO E34, PIN 6 (REF: REWORK STEP 4-16).
4-18 E34, PIN 11 TO BOTTOM OF R51.

REWORK INSTRUCTIONS CONT.

ECO #4 (CONT.)

4-19 E39 LOCATION, PIN 13 TO E39 LOCATION, PIN 10 (REF: REWORK STEP 4-23).
4-20 BOTTOM OF R23 TO E34, PIN 16.

COMPONENT ADDS: (* ONLY THESE INSTRUCTIONS SHOWN ON UA DWG.)

* 4-21 E34 (P/N 19-11911-00) 74S124.
* 4-22 C80, C83 (P/N 10-12312-01) ABOVE E34 LOCATION AND E39 LOCATION.
* 4-23 R56 (P/N 13-02955-00) AT E39 LOCATION, PINS 7 AND 10 (REF: REWORK STEP 4-8 AND 4-18).
* 4-24 E39 (P/N 19-10645-00) AT PINS 1-4, 13-16.
* 4-25 C81 (P/N 10-00010-00) AT LOCATION E34 PINS 4 AND 5.
* 4-26 C82 (P/N 10-00020-00) AT LEFT OF D10 FEED THRUS TOP & BOTTOM.
4-27 R20 (P/N 13-03064-00)
4-28 R42 & R50 (P/N 13-00316-00)
4-29 R31 (P/N 13-05125-00)
4-30 R17 (P/N 13-02858-00).
4-31 R34 (P/N 13-14187-00).
4-32 R33 (P/N 13-12923-00).
4-33 R35 (P/N 13-05145-00).
4-34 R32 (P/N 13-13592-00).
4-35 R54 (P/N 13-00285-00).
4-36 R21 & R23 (P/N 13-00249-00)
4-37 C61 (P/N 10-00050-00)
4-38 C45, C68 (P/N 10-12312-01)

COMPONENT DELETES:

4-39 R31 (P/N 13-03047-00)
4-40 R17 (P/N 13-00229-00)
4-41 R20 (P/N 13-01322-00)
4-42 R34 (P/N 13-04862-00)
4-43 R33 (P/N 13-04858-00)
4-44 R35 (P/N 13-02645-00)
4-45 R32 (P/N 13-10630-00)
4-46 R54 (P/N 13-00228-00)
4-47 R21 & R23 (P/N 13-00260-00)
4-48 C61 (P/N 10-05784-00)
4-49 C45 & C68 (P/N 10-10274-00)
4-50 E19 (P/N 19-11911-00).
4-51 C62 (P/N 10-00011-00)
4-52 R42 & R50 (P/N 13000365-00)

ECO #5

COMPONENT DELETE

5-1 C82 (P/N 10-00020-00)

M8013-ML007

ETCH CUTS SIDE 1

7-1 CUT ETCH BETWEEN E25-PIN 6 AND E7 PIN 3 AT E7 PIN 3

WIRE ADDS SIDE 1

7-2 E25 PIN 11 TO E7 PIN 3
7-3 E25 PIN 12 TO CT2 C AT PTH ABOVE C75)
7-4 E25 PIN 13 TO E25 PIN 6

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RL VII DISK CONTROL	D	UA	M8013-0-0	J
SCALE	SHEET 4 OF 4	DIST.		

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* (BC2)CMI H
* (BC2)DATO H
* (BC3)RAM STATUS H
* BC2 WCO FLW(1) H
DC3 MIS MATCH H
DC5 SEC PULSE(0) H
DC5 DRIVE READY H
DC3 CRC ERR(0) H
(CTR)
DC2 CON 2 H
DC2 CON 1 H
DC2 CON 0 H
DC2 MAINT L
DC2 MAINT H (DV2)
DC2 EN SYS CLK H
DC3 SYS (0) H
DCI INIT A L
DC2 EN CON L
DC2 EN CON H
DC2 MAINT L
(AF1)
DC4 DS CLK H
DC5 STATUS CLK H
DC2 RD STATH
* (BC3) CRDY (1) DF2
DCI 1 HIGH
DCI EN RDSTAT H
DC2 PLS 4 L
DC2 PLS 5 L
DC2 PLS 2 L
DCI ROM 0 H
DCI WRT DATA AREA H
DCI WRT DATA AREA L
DC INIT B L
DCI INIT A L
DCI WC EN H
* (BC3) CRDY (1) L
SEQC RDY (1) L DCI
DCI TRACE L
DCS GATE SEC PLS L
DCI EN CRC ERR H
+5V
R46 1K
R45 1K
DCI 1 HIGH
DC2 BRANCH L
DC2 PLS 7L
DCI INIT B L
DCI 1 HIGH
DCI TRACE L
DCI CLK BC L
DCI WC EN H
DCI INIT A L
DCI AB N
DCI A7 H
SEE NOTE # 1
+12V
-5V
INH ROM L
DCI HIGH
DCI INIT B L
DCI NPR DIS N
DC2 STALL H
DCI SEQC RDY(1) L
DCI INSTR DIS H
DCI BC ENAB H
* (BC3) CLRERR H
DCI INIT A L
DCI INIT B L
DCI ROM 0 H
DCI ROM 1 H
DCI ROM 2 H
DCI ROM 3 H
DCI ROM 4 H
DCI ROM 5 H
DCI ROM 6 H
DCI ROM 7 H
MICRO SEQUENSER

NOTES: 1. FOR ROM PT. #23-017E2-00 INSERT W1 AND W3 DELETE W2 AND W4.
FOR ROM PT. #23-0588?-00 INSERT W2 AND W4 DELETE W1 AND W3.
2 * MEANS REFERING TO POINT ON D-CS-M8014-0-1

REVISIONS			
DASH	CHANGE NO.	REV.	
-00	M8013-00001	C	R. HULTMAN
-01	M8013-ML002	D	R. HULTMAN 6-21-78
-02	M8013-ML004	E	R. HULTMAN 22-AUG-78
-03	M8013-ML005	F	R. HULTMAN 21-NOV-78
-04	M8013-ML006	G	R. HULTMAN 5-JAN-78
-05	M8013-ML007	H	M. ZARICH 3-APR-79

DRN.		10-24-77
CHK.		12-27-77
ENG.		1-6-78
PROJ. ENG.		1-6-78
PROD.		1-5-78
NEXT HIGHER ASSY.		
D-UA-M8013-0-0		
SCALE	NONE	
SHEET	1 OF 5	

FIRST USED ON RLVII

digital

TITLE
RLVII
DISK CONTROL
(DCI)

SIZE D | CODE CS | NUMBER M8013-0-1 | REV. H

DIST.

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+5V
R40 1K
EN CON H AF1
74LS04 E6
DC2 EN CON L
74LS32 E35
DC2 PLSTL

74LS175 E41
DCI NPR DIS N
74LS08 E25
DW2 DC2 NPR LN H
DC3 CRC NOT ZERO L
DC2 RD DATA AREA H
DC2 EN LOOP LOCK H
DC2 EN LOOP LOCK L
DC2 EN OS CLK H
DC2 EN SYS CLK H

74LS175 E27
CUB DC2 DCT L
DC2 WRT CRC H
DC2 WRT MKR H
DCI INIT 6 L

74S138 E46
DCI ROM 5 H
DCI ROM 6 H
DCI ROM 7 H
DC2 PLS 5 L
DC2 PLS 4 L
DC2 PLS 2 L
DCI INSTR DIS H
DCI CLK BC L
DCI WC EN H

74LS175 E42
DC2 CON 0 H
DC2 CON 1 H
DC2 CON 2 H
DC2 BRANCH H
DC2 BRANCH L

74LS175 E33
DC2 STALL H
DJ2 DC2 OSK WRT H
DC2 WRT DBR H
DC2 RD STAT H
DC2 RD DATA AREA H
DJ2 DC2 CN WRT RQST H
* (DC3)CRDY (1) L (DF2)

74LS175 E26
DC2 TRACE HALT H
DV2 DC2 MAINT H
DC2 MAINT L
DC2 WRT GATE H
DC2 SEND DRV CMD H
DC3 CRC NOT ZERO L
74LS08 E36
DCI SEQC RDY (1) L
DCI ROM 1 H
DCI ROM 2 H
DCI ROM 3 H
DCI ROM 4 H

INITBL

74LS138 E37
DW2 DC2 SET CRDY L
DC2 SET ODT L
DC2 TST DCRC L
DB2 DC2 INC DA L
DC2 CLR MATCH L
DC2 TST MCRC L
DCI 1 HIGH

MICRO SEQUENCER LATCHES

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DC3 2 HIGH

DISABLE CRYS L BDI

EXT CRYS L BCI

+5V

CDZ DC3 82 MHZ

WRT PRECOMP

DC3 WRT DATA PLS H

DC3 WRT DATA PLS L

DCI INIT B L

DC3 2 HIGH

DC3 SYS (Ø) H

DC3 MUX DATA L

DC3 CRC (1) H

DC2 WRT CRC H

DCI WC EN H

DC2 WRT MKR H

DC2 WRT DHR H

DC2 MAINT L

DC4 DS DATA (1) H

DC2 EN LOOP LOCK H

(BC2) DA (1) L

DCI WRT DATA AREA H

DC4 MARKER (1) L

DC1 CLK BC L

DC5 DRIVE READY H

DC2 BRANCH H

DC2 EN DS CLK H

DC4 DS CLK H

DC2 CLR MATCH L

DC3 MIS MATCH H

CK2 DC3 MISMATCH L

HEADER MATCH DETECTION

CRC GENERATOR

DC3 2 HIGH

DCI EN CRC ERR H

DC3 CRC (1) H

DC3 CRC NOT ZERO H

DC3 CRC NOT ZERO L

DC2 SET OPI L

DMZ

DC3 PRESET OPI L

DC2 TST MCRC L

DC2 TST DCRC L

DLZ

DC3 CRC ERR (1) H

DC3 CRC ERR (Ø) H

RA19 1K

DC3 2 HIGH

(BC3) SER DATA OUT CN2

DCI WRT DATA AREA H

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLVII DISK CONTROL (DC3)	D	CS	M8Ø13-Ø-1	H
SCALE NONE SHEET 3 OF 5	DIST			

DEC FORM NO. SBD 138

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READ DATA PULSE GENERATOR

DC2 MAINT H DV2
DC3 WRT DATA PLS L
74S37 E11
74S37 E11
C2 100NS
R25 220
74S10 E14
DC4 EARLY ERROR L
PHASE/FREQUENCY ERROR DETECTION
74S04 E24
74S00 E29
74S00 E29
74S00 E29
74S10 E14
DC4 LATE ERROR L
74S04 E24
DC4 3 HIGH
DC5 READ DATA H
+5V
R51 1K
DC4 3 HIGH
74LS112 E28
DC2 EN LOOP LOCK L
74S04 E6

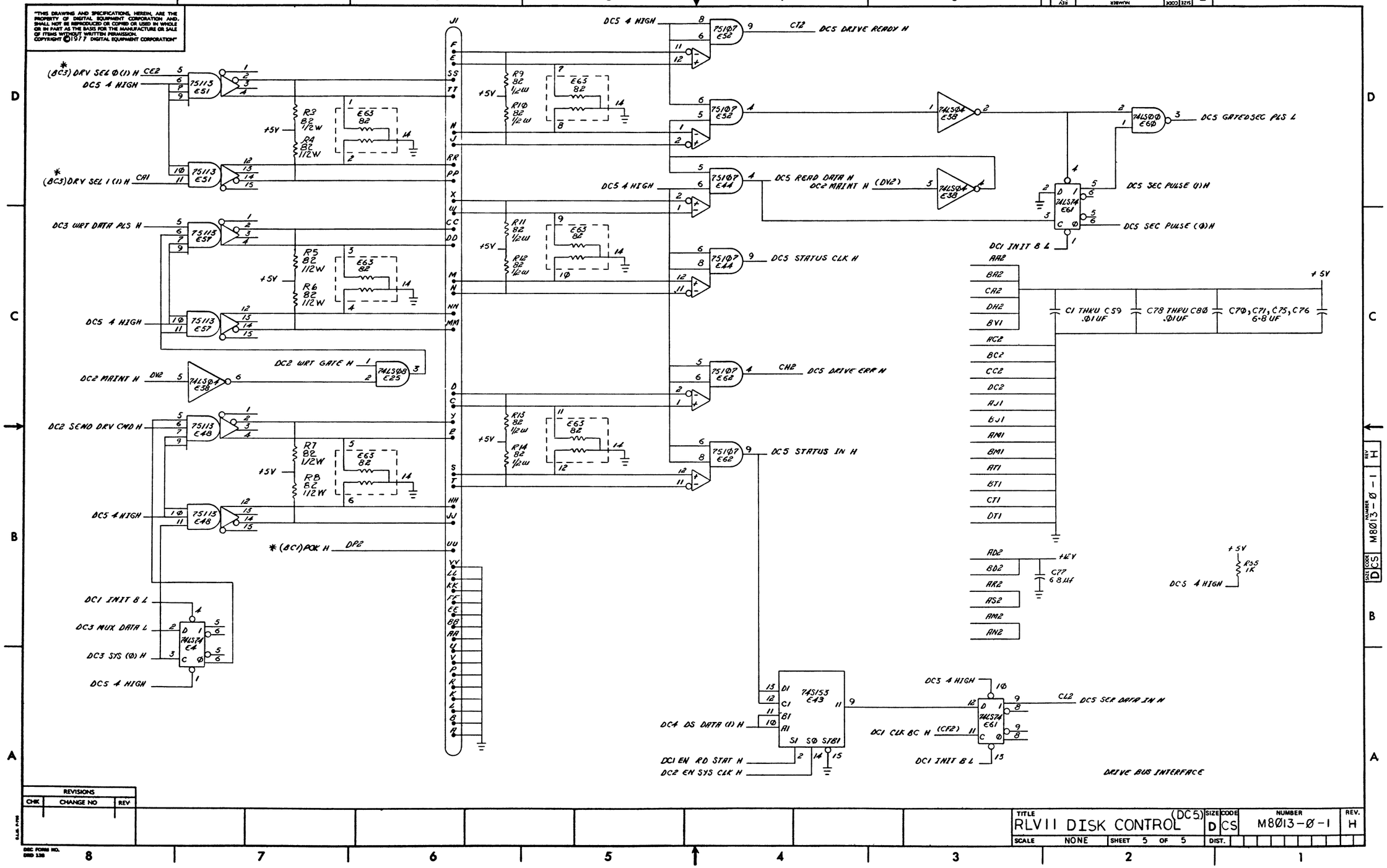
DC4 HI GAIN L (E23-9)
74S52 E39
R56 750 1%
+12V
D15 4M6.8RZ1 6.8V
R31 383 1%
Q5 2N4403
D6 IN4454
D7 IN4454
D8 IN4454
R42 470
D10 4M6.8RZ1 6.8V
R34 6.19K 1%
R50 470
Q6 2N4403
TP1 VCI
R21 150 1/2W
R22 180 1/2W
R23 150 1/2W
R24 180 1/2W
+12V
D11 4M5.1RZ1
D12 4M5.1RZ1
C80 .47UF
C81 39 PF
R33 2.49K 1%
R35 2.80K 1%
Q7 2N4403
DC4 LATE ERROR L
DC4 EARLY ERROR L
Q8 2N4403
Q9 2N4403
R20 75
C63 100 PF
D9 IN4454
R15 100 1%
R17 100 1%
C61 .033 UF
R32 4.87K 1%
R41 5K
C68 .47 UF
-10V
R54 270 1/2W
-10V
D5 6.8V 4M6.8RZ1
C45 .47 UF
74LS124 E34
CK EN
VCO CONTROL - CHARGE PUMP AND FILTER

DC4 3 HIGH
DC2 EN DS CLK H
74S74 E23
DC1 INIT B L
74S74 E13
DC4 3 HIGH
74S74 E13
READ DATA SEPARATOR
DC4 3 HIGH
DC4 DS DATA(1) H
74S74 E23
DC4 3 HIGH
DC4 MARKER(1) H
DC4 MARKER(1) L
74LS112 E28
* (BC3) CADY (1) L
DC4 HIGH GAIN L
+5V
R52 1K
EXT PLL CLK L
74S00 E5
74S02 E18
DC4 MARKER(1) L
74S02 E18
DC4 DS CLK H
+5V
R53 1K
INH VCO CLK L
74S00 E5
TP2 VCO
TP3 GND
74S00 E5
+12V
R43 5.1K
C66 5600 PF
C60 .01 MF
555 E1
CTL VIN DCG
R37 2.2K
R19 120
D13 IN754A
R26 220
Q3 MXA55
C72 15 MF
C73 15 MF
D14 IN754A
Q1 MXA05
C67 .047 UF
R27 220
D1 D672
D2 D672
R1 2.7 1/2W
-10V
C74 15 MF
LM320 10
C69 6.8 MF
-5V OUT
-10V AND -5V CHARGE PUMP

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLV11 DISK CONTROL (DC3)	D	CS	M8013-0-1	H
SCALE NONE	SHEET 4 OF 5	DIST		

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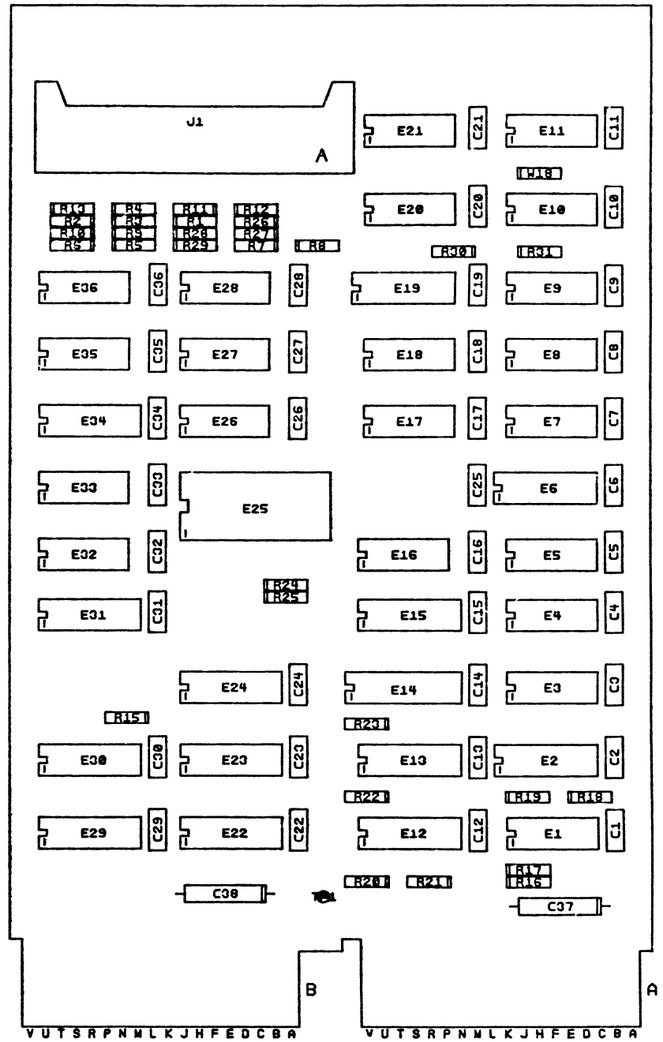


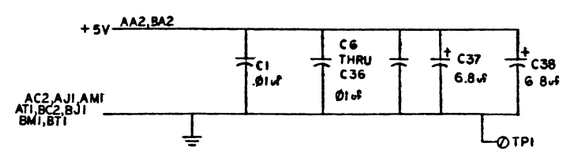
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLVII DISK CONTROL (DC5)	D	CS	M8Ø13-Ø-1	H
SCALE NONE SHEET 5 OF 5	DIST.			

DEC FORM NO. DRD 330

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NOTES:
1. JUMPER REMOVED EQUALS ASSERTION.
2. REFERENCE DESIGNATION C2-C5 AND E2-E5 ARE NOT USED.
3. JUMPERS ARE TO BE IMPLEMENTED USING 30 AWG WIRE-WRAP WIRE. SEE THE LOGIC HANDBOOK FOR RECOMMENDED TOOLS.

STEP E	+ Y AXIS ____ STEP = ____ TIMES
REPEAT	→ X AXIS ____ STEP = ____ TIMES

CHK	CHANGE NO	REV
SJW	M7946-ABOCK	E

SIGNATURES	DATE
DRN. J.VINCENT	10-75
CHK'D. FERGUSON	11-75
MECH.ENG. M.LEWANDOWSKI	11-75
PROJ.ENG. M.LEWANDOWSKI	11-75
PROD. D. DEROME	11-75
SCALE 2/1	
SHT. 1 OF 3	
NEXT HIGHER ASSY. D-UA-M7946-0-0	

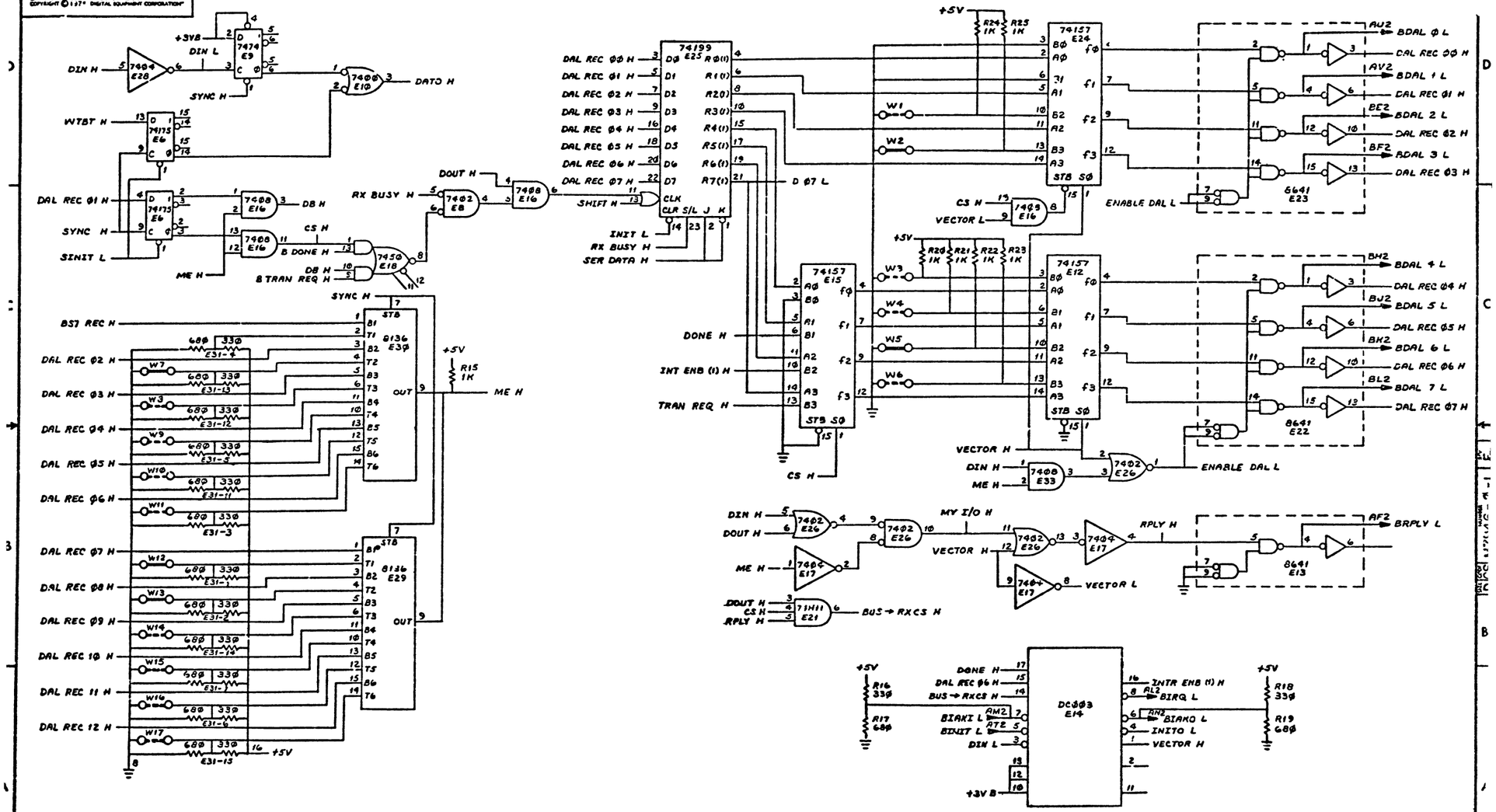
digital

TITLE RXVII
LSI 11 INTERFACE

SIZE	CODE	NUMBER	REV
D	CS	M7946-0-1	E

1 MS# 150994

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REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE	CODE	NUMBER	REV.
RXVII LSI 11 INTERFACE		D	CS	M7946-Ø-1	E
SCALE	SHEET 2 OF 3	DIST			

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+5V R1 180Ω
J1 BB RX DATA L
R2 390Ω
8643 E36 pin 3 — SER DATA H

RX SHIFT L — J1 LL
+5V R9 180Ω
R10 390Ω
SHIFT H — 7404 E28 — B SHIFT L

RX TRANS REQ L — J1 7
+5V R11 180Ω
R12 390Ω
8641 E34
BTRAN REQ H
RUN (Ø) H — 7408 E7 — TRAN REQ H
7402 E8 — RX BUSY H

+5V R3 180Ω
J1 X RX DONE L
R4 390Ω
8640 E36 — B DONE H
7404 E28 — BDONE L
7400 E33 — DONE H (RUN (Ø) H)

+5V R5 180Ω
RR RX OUT L
R6 390Ω
8640 E36 — FROM RXØ1 H
7404 E28 — TO RXØ1 H

+5V R7 180Ω
J RX ERROR L
R8 390Ω
8640 E36
8881 E27 — BV2 — BDAL 15 L
CS H, DIN H — 7408 E33

BSYNC L — AJ2 — 8640 E1 — SYNC H
BDOUT L — AS2 — 8640 E1 — DOUT H
BDIN L — AH2 — 8640 E1 — DIN H
BWTBT L — AH2 — 8640 E1 — WTBT H

BU2 — BDAL 14 L
8641 E34

BUS → RXCS H
7450 E18 — INIT L — 7404 E17 — INIT H
7404 E17 — SINIT L
INITO L — 7400 E17
W18

J1 N RX INIT L
+5V R13 120Ω
8641 E34

AP2 — BBS7 L
BS7 REC H
BM2 — BDAL 8 L
CAL REC Ø8 H
8641 E13

8281 E35 (D3 D2 D1 DØ; R3(1) R2(1) R1(1) RØ(1); CLR LD CLKØ CLK1)
INIT H, RUN (1) H — 7402 E8 — +3V A
B SHIFT L

7404 E28 — D Ø7 L — 7450 E20 — 7404 E28 — TO RXØ1 H — 8881 E27 — RX DATA L — J1 BB
BDAL 9 L — BM2 — 8640 E32 — DAL REC 09 H
BDAL 10 L — BP2 — 8640 E32 — DAL REC 10 H
BDAL 11 L — BP2 — 8640 E32 — DAL REC 11 H
BDAL 12 L — BP2 — 8640 E32 — DAL REC 12 H

74LS196 E19 (J C K; PRESET)
+3V A

DATO H — 7400 E11
TO RXØ1 H — 7400 E11
FROM RXØ1 H — 7400 E11
DATO H — 7400 E11
DATO H — 7408 E7
DAL REC 00 H

+5V R28 180Ω
+3V A
R29 390Ω
+5V R30 180Ω
+3V B
R31 390Ω

AR2 AS2

BDONE L — 7400 E10
BDONE H — 7400 E10
DB H — 7450 E20
CS H — 7450 E20

+3V A
74174 E9 (D C RUN)
RUN (1) H
RUN (Ø) H
MY I/O H — 7409 E7
RUN (Ø) H
INIT H — 7402 E8
RX BUSY H

+5V R26 180Ω
R27 390Ω
8881 E27
RUN (1) H
FX RUN L — J1 D

REVISIONS
CHK | CHANGE NO. | REV

TITLE RXVII LSI 11 INTERFACE
SIZE D CODE DCS NUMBER M7946-Ø-1 REV. E
SCALE — SHEET 3 OF 3 DIST

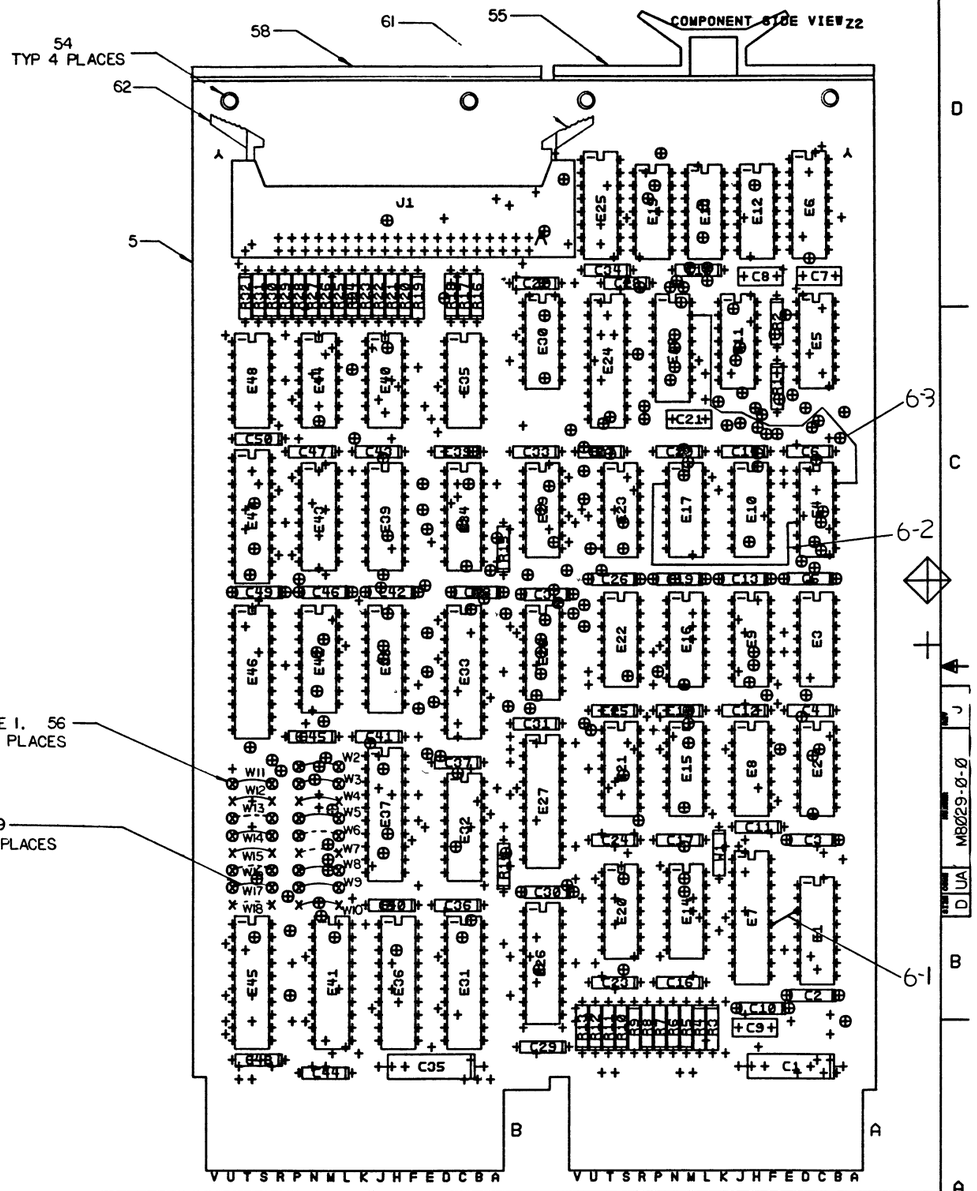
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REWORK, WIRE ADDS

6-1 ADD ON SIDE 1, A WIRE FROM E7 PIN 15 TO E1 PIN 3

6-2 ADD ON SIDE 1, A WIRE FROM E4 PIN 5 TO E17 PIN 2

6-3 ADD ON SIDE 1, A WIRE FROM E4 PIN 13 TO E18 PIN 15



NOTES:
1. ITEM *56 ARE WIRE WRAP PINS, W2 THRU W18

STEP & REPEAT	↑ Y AXIS ____ STEP ____ TIMES
	→ X AXIS ____ STEP ____ TIMES

CHK	CHANGE NO	REV
	REVISED AND REDRAWN ML005	F
WK	M8029-ML004	H
	M8029-SK001	J

DRN.	J FITZGERALD
CHK'D.	
MECH. ENG.	
PROJ. ENG.	
PROD.	
SCALE	2/1
SHT.	1 OF 1

ETCH REV. D-P3

NEXT HIGHER ASSY. B-DD-M8029-Ø

digital

TITLE RXV21 LSII
RXØ2 CONTROLLER

SIZE	CODE	NUMBER	REV
D	UA	M8029-Ø-Ø	J

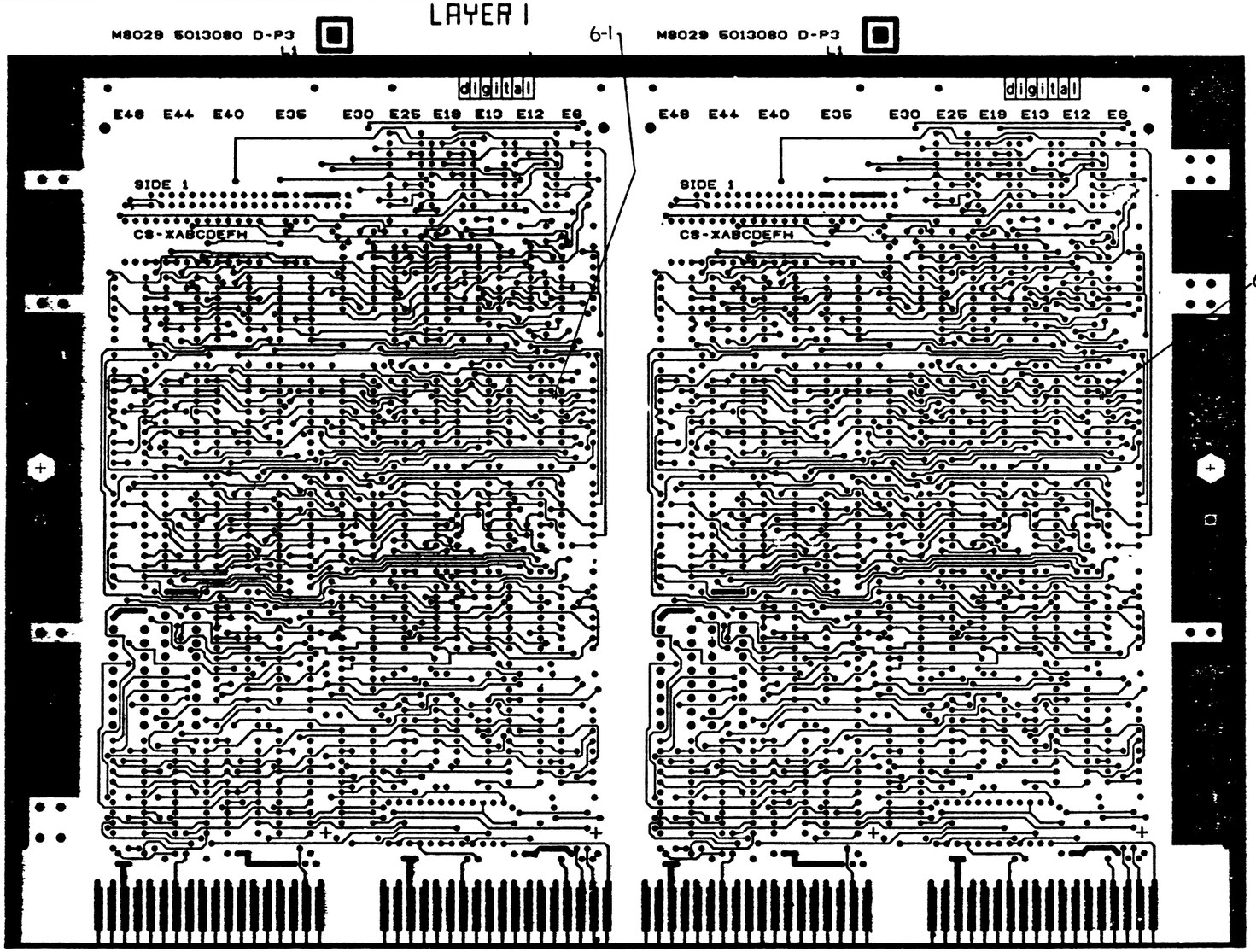
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REWORK INSTRUCTION.

6-1: CUT ETCH ON SIDE 1 OF E4. ETCH COMING BETWEEN PINS 2&3 OF E4.

LAYER 1



NOTES:

CHK	CHANGE NO	REV
	ORIG	F
	M9029ML5	H
	M9029ML6	J
	M9029ML7	K

SIGNATURES	DATE
DRN. POWERS	2/1980
CHK'D.	
ENG.	
PROJ. ENG.	
PROD.	

digital

TITLE: ETCH CUT DRAWING

SCALE 2:1 | SIZE D | CODE EC | NUMBER 5013080-0-0 | REV H

SHT. 1 OF 2

ETCH REV D FIRST USED ON

DEC 5013080-0-0 H

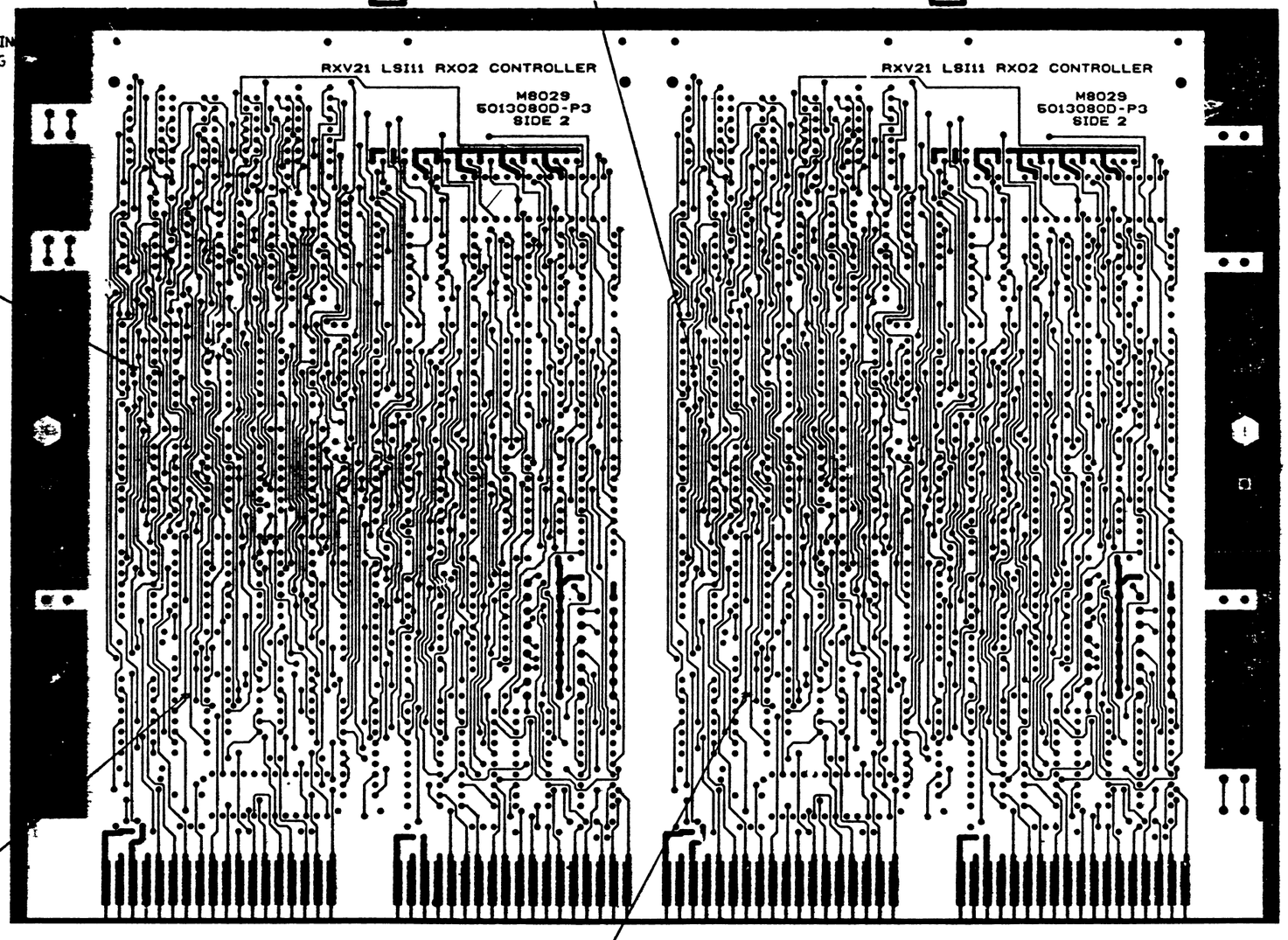
1 MS#

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REWORK INSTRUCTION:

6-2: CUT ETCH ON SIDE 2 AT E4 TO RIGHT OF PIN 11, IMMEDIATELY ABOVE FEEDTHOLE (SECOND ETCH IN

6-3: CUT ETCH ON SIDE 2 AT E7 PIN 15 BY CUTTING ETCH THAT GOES BETWEEN E7 PIN 15 AND E16 PIN 8.



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
ETCH CUT DRAWING	D	EC	5013080-0-0	H
SCALE 2:1 SHEET 2 OF 2	DIST.			

DEC 5013080-0-0 H

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74LS174 E43
DI TS BUS 9 H
DI TS BUS 8 H
DI TS BUS 4 H
DI TS BUS 3 H
DI TS BUS 2 H
DI TS BUS 1 H
D5 D4 D3 D2 D1 D0
R5(I) R4(I) R3(I) R2(I) R1(I) R0(I)
DI FUNCT 2 H
DI FUNCT 1 H
DI FUNCT 0 H
CLR CLK
D2 INIT L
D3 WRT CSR PLS H

8097 E39
D4 BTR H → DI TS BUS 7 H
DI TS BUS 9 H
DI TS BUS 8 H
D4 B ERROR H → DI TS BUS 15 H

8097 E38
DI TS BUS 12 H
DI TS BUS 4 H
DI TS BUS 0 H
DI TS BUS 13 H

8097 E39
D3 IE H → DI TS BUS 6 H
D3 RD CSR L
D4 B DONE H → DI TS BUS 5 H

8097 E38
+3V2
DI TS BUS 11 H
DI TS BUS 14 H

8097 E42
DI TS BUS 3 H
D2 DB SEL 1 L

74LS299 E37
D2 INIT L
D3 DB CLK H
D4 SER DATA H
D2 LO SEL 0 H
D2 DB SEL 1 H
CLR CLK SR SL S0 S1 ENA 1 ENA 2
DI TS BUS 7 H
DI TS BUS 5 H
DI TS BUS 1 H
DI TS BUS 0 H
DI TS BUS 2 H
DI TS BUS 4 H
DI TS BUS 6 H
DI DATA 7 H

74LS257 E34
+3V2
D4 RX AC LO H
D3 NXM (I) H
B3 A3 B2 A2 B1 A1 B0 A0
OUT CONT S0
DI EN MUX L
D4 B DONE H
DI TS BUS 3 H
DI TS BUS 11 H

74LS299 E33
D2 SHFT RT H
D2 HI SEL 0 H
CLR CLK SR SL S0 S1 ENA 1 ENA 2
DI TS BUS 15 H
DI TS BUS 13 H
DI TS BUS 9 H
DI TS BUS 8 H
DI TS BUS 10 H
DI TS BUS 12 H
DI TS BUS 14 H
DI DATA 15 H

74LS08 E22
D4 ENA 12 BIT L
D3 RD DB L
D3 EN DATA L
DI EN MUX L

8097 E42
DI TS BUS 11 H
D2 DB SEL 1 L
DI DATA 11 H

REVISIONS			
DSR	CHANGE NO.		REV.
M.H.	M8029-00001		C
J.GLAVIN			
E.R.	M8029-ML002		D
C.YOUSE			
	M8029-ML003		E
J.RYAN			
	M8029-ML005		F
D. POWER			
M.HILDEBRANT	M8029-ML006		H
K. KOPPELMAL	M8029-SHOOT		J
A.P. SOLOMON			

DRN		10/25/77
CHK'D		10/31/77
ENG.		12/21/77
PROJ. ENG.		2/6/78
PROD.		2/6/78
NEXT HIGHER ASSY.	B-DD-M8029-0	
SCALE		
SHEET	1 OF 4	

FIRST USED ON RX02
digital
TITLE
RXV21 LSI11 (DI)
CONTROLLER
SIZE D | CODE CS | NUMBER M8029-0-1 | REV. J
DIST.

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B DAL 13 L BT2 — DC005 E41 BUS 3 — DAT 3 — D2 TS BUS 13 H
B DAL 12 L BS2 — BUS 2 — DAT 2 — D2 TS BUS 12 H
B DAL 11 L BR2 — BUS 1 — DAT 1 — D2 TS BUS 11 H
B DAL 14 L BU2 — BUS 0 — DAT 0 — D2 TS BUS 14 H
+3V2 — JA3
JA2
JA1 — MATCH
BBS 7 L AP2 — MEN B
JAV3
JAV2
JAV1
XMIT REC

B DAL 9 L BN2 — DC005 E45 BUS 3 — DAT 3 — D2 TS BUS 9 H
B DAL 8 L BM2 — BUS 2 — DAT 2 — D2 TS BUS 8 H
B DAL 7 L BL2 — BUS 1 — DAT 1 — D2 TS BUS 7 H
B DAL 15 L BV2 — BUS 0 — DAT 0 — D2 TS BUS 15 H
JA3
JA2
JA1 — MATCH
MEN B
JAV 3
JAV 2
JAV 1
XMIT REC

B DAL 6 L BK2 — DC005 E36 BUS 3 — DAT 3 — D2 TS BUS 6 H
B DAL 5 L BJ2 — BUS 2 — DAT 2 — D2 TS BUS 5 H
B DAL 4 L BH2 — BUS 1 — DAT 1 — D2 TS BUS 4 H
B DAL Ø L AU2 — BUS Ø — DAT Ø — D2 TS BUS Ø H
JA3
JA2
JA1 — MATCH
MEN B
JAV 3
JAV 2
JAV 1
XMIT REC
XMIT EN 1 H

B DAL 1Ø L BP2 — DC005 E31 BUS 3 — DAT 3 — D2 TS BUS 1Ø H
B DAL 3 L BF2 — BUS 2 — DAT 2 — D2 TS BUS 3 H
B DAL 2 L BE2 — BUS 1 — DAT 1 — D2 TS BUS 2 H
B DAL 1 L AV2 — BUS Ø — DAT Ø — D2 TS BUS 1 H
JA3
JA2
JA1 — MATCH — D2 MATCH H
MEN B
JAV 3
JAV 2
JAV 1
XMIT REC
D3 XMIT EN 2 H
D3 DAL REC H

D3 ENB VEC H
W11 W10 W9 W8 W7 W6 W5 W4 W3 W2
W18 W17 W16 W15 W14 W13 W12
R9 270 +5V

+3V2
D3 MAS RPLY H
D3 LOAD BAR L
D3 EN ADDR H

DC006 E47 CNTIA — 128 D/F — D2 TS BUS 7 H
CLK-A — 64 D/F — D2 TS BUS 6 H
S-A — 32 D/F — D2 TS BUS 5 H
16 D/F — D2 TS BUS 4 H
CLK-C — 8 D/F — D2 TS BUS 3 H
S-C — 4 D/F — D2 TS BUS 2 H
2 D/F — D2 TS BUS 1 H
1 D/F — D2 TS BUS Ø H
RD
LD — MAX-A
RD-A — MAX-C

DC006 E46 CNTIA — 128 D/F — D2 TS BUS 15 H
CLK-A — 64 D/F — D2 TS BUS 14 H
S-A — 32 D/F — D2 TS BUS 13 H
16 D/F — D2 TS BUS 12 H
CLK-C — 8 D/F — D2 TS BUS 11 H
S-C — 4 D/F — D2 TS BUS 1Ø H
2 D/F — D2 TS BUS 9 H
1 D/F — D2 TS BUS 8 H
RD
LD — MAX-A
RD-A — MAX-C

D4 SER DATA H — 74LSØØ E9 — 74LSØØ E9 — D2 SHFT RT H
D4 DONE L
DI DATA 7 H — 74LSØØ E9
D4 RX DONE H

D3 WRT CSR PLS H — E4Ø — 74LS32
D3 WRT CSR L — 74LS161 E32 CLR — LD — CLK — CNT EN — CRY EN — CO
D2 INIT L
+3V2
D2 TS BUS 12 H — DØ — DI — D2 — D3 — RØ(I) — R1(I) — R2(I) — R3(I)
D2 TS BUS 13 H
D3 EN ADDR H — 8881 E2Ø — 13 ACI — D2 BAD 16 H
8881 E2Ø — 1Ø ADI — D2 BAD 17 H

D3 MASTER L — 74LS32 E2
D4 OUT H
D3 WRT DB L — 74LSIØ E3Ø
D3 WRT CSR L
D2 DB SEL 1 H
7404 E23 — DB SEL 1 L
D4 RX DONE H — E2 — 74LS32
D4 ENA 8 BIT H — 74LS32 E28 — D2 LO SEL Ø H
D4 ENA 8 BIT L — E28 — 74LS32 — D2 HI SEL Ø H

D3 WRT CSR H — 74LSIØ E17
D2 TS BUS Ø H
D4 B DONE H
D2 GO L

D4 LD BAR H — E17 — D2 LOAD BAR L
D3 WRT DB H
D3 SRPLY H
74LSIØ

D2 B INIT L — 8640 E14 — 7432 E4 — D2 INIT H
7404 E23 — D2 INIT L

D2 TS BUS 14 H — E22 — D2 PROG INIT H
D3 WRT CSR PLS H
74LSØ8

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE	CODE	NUMBER	REV.
RXV21 LSI11 CONTROLLER	(D2)	D	CS	M8029-Ø-1	J
SCALE	SHEET 2 OF 4	DIST.			

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R8 680 R7 330 +5V

+5V R5 330 D3 NPR REQST (I) H BOMGI L AR2 R6 680

DC0I0 E7: REQ, BDMGI, DATIN, DATIO, CNTEN, BUSYNC, RPLY, TMOUT, CLK, INIT, BDMR, MASTER, BDMGO, SYNC, DIN, DOUT, ADREN, DATEN

D4 OUT H, +3V2, D3 SYNC H, D3 REPLY H, D3 8.2 MHZ, D2 INIT H, E11 74LS02

8881 E20 BNI D3 B SACK L; ANI D3 B DMR L; AS2 D3 B DMG O L

7404 E23 MASTER L, D3 MDIN H, 7432 E4, D3 MASTER H

D3 REPLY H, 7408 E16 D3 MAS RPLY H; D3 M DIN H; E19 74LS04 D3 M DIN L

D3 SYNC O H; D3 M DOUT H; D3 EN ADDR H; D3 EN DATA L

8881 E20 AK2 D3 BWT BT L

74LS04 E19, D3 MAS RPLY H, 74LS02 E11 D3 NXM (0) H; D3 NXM (1) H

D3 RD DB L, 7408 E16, E19 74LS04 D3 XMIT EN 2 H

+3V1, 74LS74 E12, D3 SYNC 0 H

D3 RD CSR L, 7408 E16, 8640 E14 D3 XMIT EN 1 H; 7408 E16 D4 ENA 12 BIT L D3 DAL REC H

C7 1000pf R2 392 K 1% +5V, 74123 E6, +3V1 74LS74 E12, D2 INIT L

+3V1 74LS74 E10 D4 NPR REQ H; D3 NPR REQST (1) H, D3 NPR REQST (1) L

+5V 14 8.2MHZ OSC E8 8 W1 D3 8.2 MHZ 7

B RPLY L AF2, D3 SRPLY H, B DIN L AH2, B DOUT L AE2, B SYNC L AJ2, 8641 E1

D3 REPLY H; D3 DIN H, 74LS04 E15 D3 DIN L; D3 D OUT H, 74LS04 E15 D3 D OUT L; D3 SYNC H, 74LS04 E15 D3 SYNC L

D3 SEL CS L, D3 PROC OUT L, 74LS02 E21, 7404 E23 D3 WRT CSR L; D3 WRT CSR H

D3 WRT CSR PLS H, 74LS02 E21 SRPLY L

D3 SEL DB L, D3 PROC OUT L, E21 74LS02, E15 74LS04 D3 WRT DB L; D3 WRT DB H

+5V R10 330 AM2 R11 680

DC003 E26: RQSTA, BIAKI, BINIT, BDIN, RQSTB, ENA DAT, ENB DAT ENB CLK, ENA ST, BIRQ, BIAKO, INITO, VECTOR, VEC RQST, ENB ST ENA CLK

D4 B DONE H, D2 INIT L, D3 DIN L, DI TS BUS 6 H; D3 IE H, AL2 D3 BIRQ L, D3 ENB VEC H

+5V R13 330 AN2 D3 BIAKOL R12 680

D3 WRT CSR PLS H

D3 PROC OUT L, D3 SRPLY L, E2 74LS32; D4 SHIFT L, D3 LOAD BAR L, D4 INHB DB H, 74LS10 E17 D3 DB CLK H, D2 MATCH H

D3 M DIN L, D3 MDIN H, R15 1K 1%, E9 74LS00, C21 120 pf 5%

C9 220pf 1% +5V R4 4.64K 1%

74LS04 E15 D3 SRPLY L; D3 SRPLY H

R3 1K +5V

DC004 E27: SYNC, DAL 2, DAL 1, DAL 0, WTBT, DOUT, DIN, VECTOR, ENB, RXCX, BRPLY, SEL 6, SEL 4, SEL 2, SEL 0, OUT HB, OUT LB, INWD

D4 ENA 12 BIT H, DI TS BUS 1 H, +3V2, D3 ENB VEC H

74LS32 E28: D3 RD DB L; D3. RD CSR L; D3 IN WRD L

D3 SEL CS L, D3 SEL DB L, D3 PROC OUT L

REVISIONS

CHK	CHANGE NO.	REV.

TITLE		SIZE	CODE	NUMBER	REV.
RXV21 LSI11 CONTROLLER (D3)		D	CS	M8029-0-1	J
SCALE	SHEET 3 OF 4	DIST.			

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D4 BUF DONE L
D4 DONE L
D4 RX DONE H
74LSØ2 E3
8640 E14
D4 BB DONE H
D4 INHB DB H

+3V1
D3 D2 D1 DØ
RQ(I) R1(I) R2(I) R3(I)
74LS193 E25
D2 INIT H
D2 GO L
D4 CNTR CLK H
CUP CDN CRY BOR

25GX8 E24
AØ A1 A2 A3 A4 A5 A6 A7
YØ Y1 Y2 Y3 Y4 Y5 Y6 Y7
CS1 CS2
D4 NPR MODE H
D4 DEFUNCT Ø H
D4 DEFUNCT 1 H
D4 OUT H
D4 RX DONE H
D4 B DONE H
D4 BBTR H

74174 E18
D5 D4 D3 D2 D1 DØ
R5(I) R4(I) R3(I) R2(I) R1(I) RØ(I)
CLK CLR
D4 RUN CLOCK H
D4 NPR REQ H
D4 LD WC H
D4 ENA 16 BIT H
D4 NPR MODE H
D2 INIT L

D3 MAS RPLY H
D4 RUN CLOCK H
7432 E4
D3 WRT DB H
D4 SHIFT H
D2 INIT H
E3 74LSØ2
74LS574 E1Ø
D4 RUN (1) H
D4 RUN (Ø) L
8881 E35
D4 RX RUN L

D4 RX AC LO H
D4 BB DONE H
E4Ø 74LS32
D4 B DONE H

E15 74LSØ4
D4 BUF DONE L

+5V R32 180 VV D4 RX DMA H
+5V R26 1K FF D4 RX 12 BIT L
+5V R19 120 N D4 RX INIT L

D2 INIT H
8881 E35
B BPOK H
8640 E14
D4 BUS POK L

D4 SHIFT L
D4 ENA 12 BIT L
74LS32 E4Ø
D4 CNTR CLK H
D2 GO L
D2 LOAD BAR L
D4 TR PLS L
E3Ø 74LS1Ø
74LSØ4 E19
D4 LATCH CLK L

D4 LD WC H
+5V
JI
RX DONE L X R22 180
RX OUT L RR R29 180
RX ERROR L J R18 180
RX SHIFT L LL R27 180
RX TRANSFER REQUEST L T R21 180
RX AC LO L TT
R23 R30 R17 R28 R20 R31 390
8640 E44
8640 E48
74LSØ4 E19
D4 DONE L
D4 RX DONE H
D4 OUT H
74LS32 E4Ø
D4 B ERROR H
D4 ERROR H
74Ø4 E23
D4 SHIFT L
D4 SHIFT H
D4 TR H
D4 RX AC LO H

D4 ENA 12 BIT H
DI DATA 11 H
D4 ENA 8 BIT H
DI DATA 7 H
D4 ENA 16 BIT H
DI DATA 15 H
74LS54 E13
D4 OUT H
8640 E48
8881 E35
+5V R25 180
R24 390
8640 E48
D4 SER DATA H
BB D4 RX DATA L

C8 100PF RI 10K +5V
+3V1
74LSØ2 E11
D4 TR H
D4 LD WC H
74123 E6
D4 TR PLS L

D4 RUN CLOCK H
D2 INIT L
74LSØ8 E22
D4 TR H
D4 RUN (1) H
E5 74S74
D4 ENA 12 BIT L
D4 ENA 16 BIT H
D4 ENA 12 BIT H
74LSØ2 E11
74LSØ4 E19
D4 ENA 8 BIT L
D4 ENA 8 BIT H

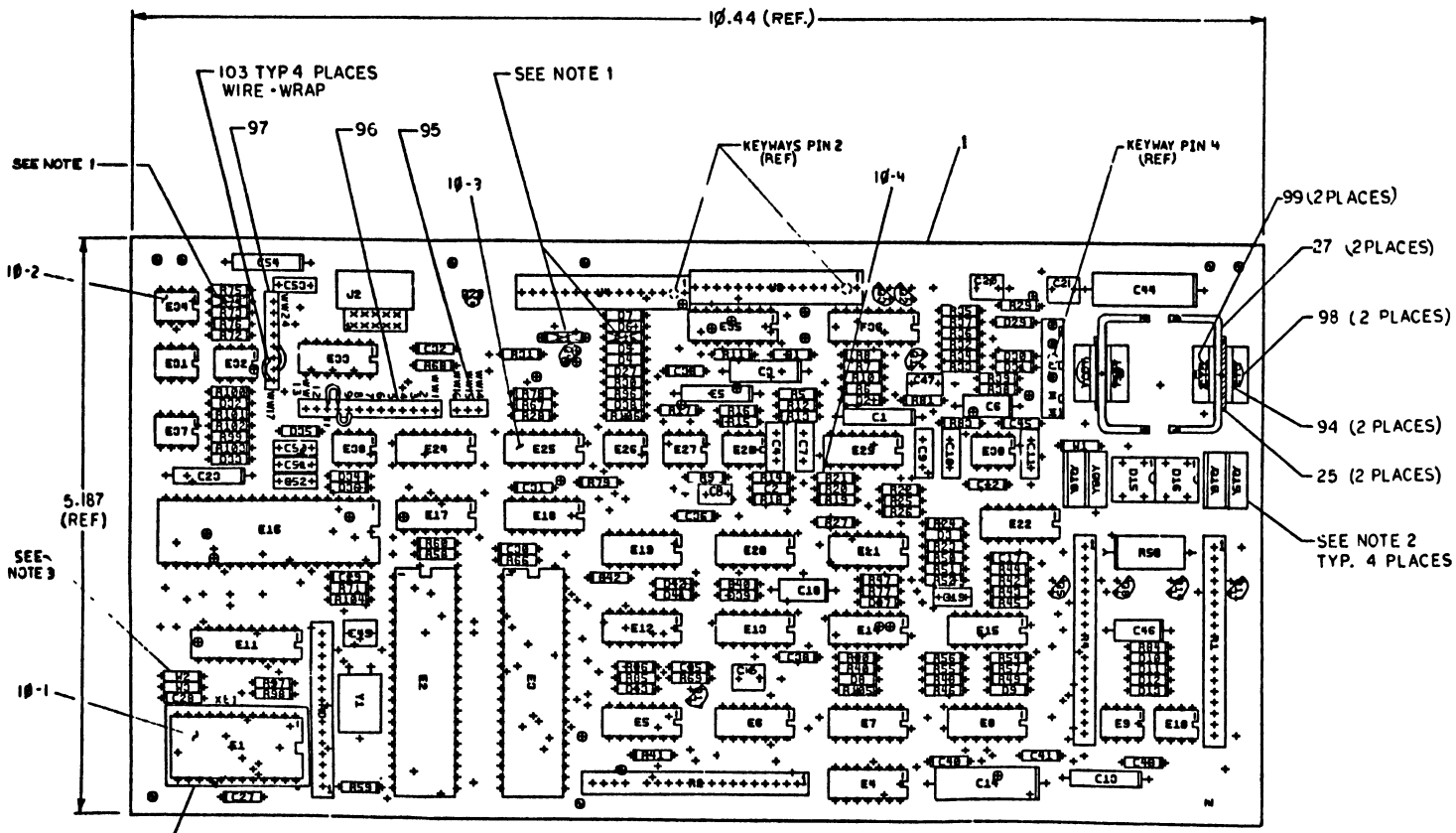
D4 BBTR H
D4 LATCH CLK L
D2 INIT H
D4 RUN (1) H
E5 E3 74S74 74LSØ2
D4 BTR H
+5V R16 1K R14 1K +3V2

DI FUNCT 2 H
DI FUNCT 1 H
74LSØ2 E21
E29 74LS74
D4 DEFUNCT 1 H
D4 DEFUNCT 1 H
74LS1Ø E3Ø
DI FUNCT Ø H
D4 DEFUNCT Ø H
D4 BUF DONE L
D3 NPR REQST (1) L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE	CODE	NUMBER	REV.
RXV21 LSI11 CONTROLLER	(D4)	D	CS	M8029-Ø-1	J
SCALE	SHEET 4 OF 4	DIST.			

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COMPONENT SIDE VIEW

NOTES:
1. C15, L1 & R74 NOT USED
2. MOUNT Q9,Q10,Q15 & Q16
 SKL ABOVE BOARD SURFACE.
3. W2 IS OPTIONAL DO NOT INSTALL.

CHG/CHANGE NO.	REV
RE-VISED & RE-DRAWN	H
	J
	K
	L

ETCH REV. F-P1

SIGNATURES	DATE
DRN. D. MOWERS	10/11
CHK D. [illegible]	[illegible]
MECH. ENG. [illegible]	[illegible]
PROJ. ENG. [illegible]	[illegible]
PROD. [illegible]	[illegible]
SCALE 2/1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. B-CO-5413489-0	

digital

TITLE SERIAL TU58

SIZE E | CODE UA | NUMBER 5413489-00 | REV L

ECO #10. REWORK:

SIDE 1:

10-1. CHANGE E1 TO 23389E2-03.
10-2. CHANGE E34 TO 1919542-21.
10-3. CHANGE E25 TO 1910534-00.
10-4. CHANGE R21 TO 1301310-00.

NOTES:

1. MANUFACTURING TEST MUST INCLUDE 'BOOT-ON-BREAK' IN THE MANUFACTURING PROCESS. TEST OF THE FEATURE IS ACCOMPLISHED BY CONNECTING PIN WW 15 TO PIN WW 16 THEN BREAKING THE CONNECTION AND RECONNECTING. IF THE PINS ARE CONNECTED, THE UNIT WILL AUTOBOOT ON 'POWER UP' AS WELL.

REVISION HISTORY

REV	ECO NUMBER	DATE

TITLE: SERIAL TU58

DOCUMENT NUMBER: EU 5413499-0-0 REV -

SCALE: —— SHEET 2 OF 2

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CART L
N/C
PERMIT L
S GND
MOTOR +
MOTOR −
+12V
TACH
LED
H GND
ERASE RT
ERASE I
ERASE Ø
HEAD RT
HEAD Ø
HEAD I
J3/J4 TYPICAL CONNECTION

E11 88 REG 74LS373 LATCH
ALE
OCE
+5V

E1 8316E ROM 2K×8
389E2-27
A3
A8 A9 A10
A11
R97 10K
W2
CS1 CS2 CS3
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
W3
R98 10Ω
A11

R58 10K
R59 10K
R60 220K
READY
HOLD
INTR
TRAP
TRAP Hø
X1
Y1 4915Z MHz
X2
RESET L
RESET IN
E2 8085 CPU
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
A8 A9 A10 A11 A12 A13 A14 A15
S0 S1 ALE WR RD INTA HLDA RESET OUT CLOCK IO/M SOD
S0 H S1 H ALE WRL RDL RESET H CLK H IO/M WRT DATA H
RST5.5 RST6.5 RST7.5 SID
RST 5.5 RST 6.5 RST 7.5
RD STROBE H
RD DATA −

R100 470
R101 2.55K 1%
R102 20K 1%
R103 12K
R99 10K
+12V +12V +5V
D32 5.1V
E37 393
M RESET L
D33 DG72
C49 .47μf
R104 100K
+5V
A13 IO/M RDL
LS27 E18
RESET L
R67 10K
E24 LSIØ
(RAMCS L)
A14 A15 A12 A13
LS27 E18
LSØØ E19

E3 RAM I/O TIMER 8155
IO/M RD L WR L ALE
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
CE L
RESET H
CLK H
RESET
TIMER IN
TIMER OUT
PC5 PC4 PC2 PC3 PC1 PC0
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
TMR OUT L
BOOT L
30 IPS H
ERASE ENA L
GAIN REDUCE L
SEL TRK Ø L
SEL DRV B L
REVERSE H
WRT ENB H
RUN L
MARK H (SW BOOT L)
OE
RJN TP L
A CART L
B CART L
VEL TP H
WRT PERMIT L
TP2
TP1
TP3
D28
R77 4.7K
E25
R78 470Ω
R68 10K

R69 2.4K +5V +3V
MARK H
TMR OUT L
E5 LS107
E12 LS107
E25

E7 BIN CTR 74LS197
1D-A 1D-B 2D-B 4D-B CLK A CLK B LOAD CLR
1R-A 1R-B 2R-B 4R-B
CHG CLK H
38.4KB CLK H
3ØIPS H
LSØØ E19
E12 LS107
VEL CLK H
+3

E33 DUAL BIN CTR 74LS393
38.4KB CLK H
RESET H
1R-B 2R-B 1R-A 2R-A 4R-A 8R-A
WW4 WW3 WW2 WW1 WW8 WW7 WW6 WW5 WW9
WW10 WW11 WW12 WW13
(RCV CLK) (XMIT CLK)
AUX B AUX A
E25 E24 LS10 E24 LS10
RDL WRL IO/M A3
R3A R3M 2.4K R3J 2.4K R11 2.4K

E16 UART 6402
Vcc
RRD DRR TBRL RRC TRC
TRO RRI SFD CLS1 CLS2 EPE CRL PI TBRE PE OE DR FE TRF6 NC RST
RESET H
R3N 15 2.4K
RST 5.5
OE
RST 6.5
TRAP H
R3K 2.4K
R3P 2.4K
BOOT L
E17 LSØØ
R72 68K
R73 10K
R75 2K
R76 4.7K
E32 9636
E34 9639
E35 9638
xMIT+ xMIT− AUX A AUX B RCV+ RCV−
J2

CHG CLK H
E17 74LSØØ
E38 MHØØ26
C50 .22μf
C53 .22μf
C54 6.8μf
D35 D672
D39 D672
C23 6.8μf
C51 .22μf
D36 D672
C52 .22μf
-12V
+V

C27 THRU C32, C35, C36, C38, C40 THRU C43
.01μf
GND
C33 .01μf
+12V

INTERFACE

REVISIONS			
SYM	CHANGE NO		REV.
	5413489-MI 001	M LEIS	D
	5413489-MI 003	M LEIS	E
	5413489-MI 004	M LEIS	F
	5413489-ML 007	M LEIS	J
	5413489-ML 006	M LEIS	H
	5413489-SH 008	A. RAYMOND	K
	5413489-SH 010	R. GLEIM	L

DRN M. LEIS	7-1978	FIRST USED ON TU58
CHK'D M LEIS	7-2078	digital
ENG EQUIP LES	7-28	TITLE TU58 ELECTRONICS:
PROJ ENG	8/11/78	SERIAL
PROD	8-1-78	
NEXT HIGHER ASSY.	B-DD-5413489-0	SIZE D CODE CS NUMBER 5413489-0-1 REV. -
SCALE		DIST
SHEET 1 OF 2		

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"AGC" "AMP" "BIT DETECT" "TACH AMP" "1/4 BIT DELAY" "SERVO AMP" "ERASE HEAD DRIVER"

DRIVE "A" DRIVE "B"

GAIN REDUCE L WRITE L WRT DATA H WRT ENB H WRT PERMIT L

SEL DRV B L SEL Ø H (SEL Ø L) (SEL A L) (WRITE OK L)

RUN A H RUN B H RUN TP L RUN A H

SEL TRK Ø L ERASE ENA L SEL Ø H

RD DATA H RD STROBE H

VEL TP H VEL CLK H

REVERSE H R H F H

A CART L B CART L

M RESET L

J1 POWER INPUT +V +12VIN +5V

W1

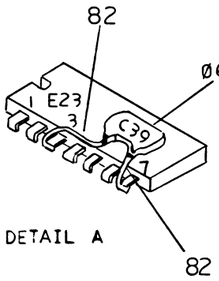
J3 J4 J5

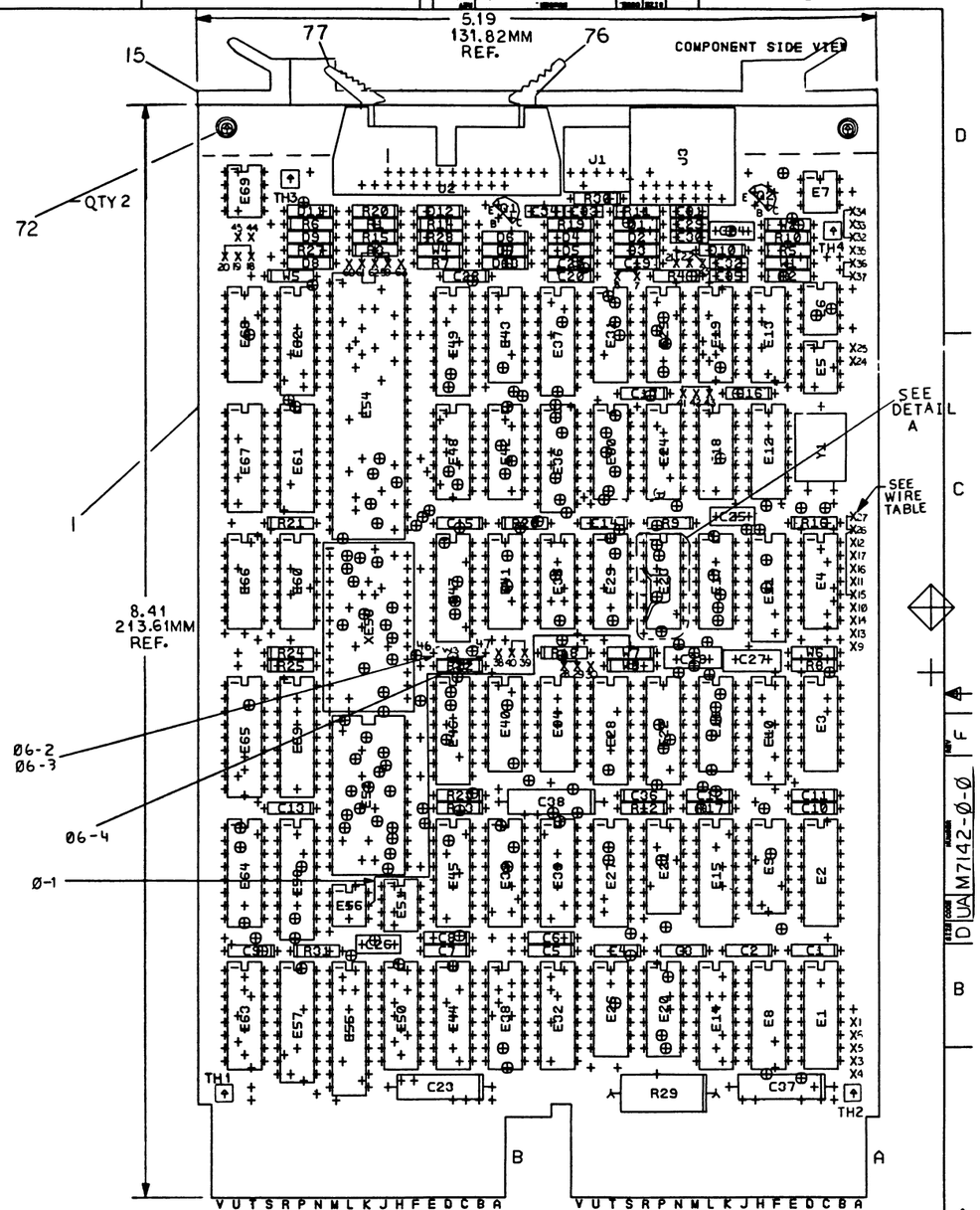
REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
TU58 ELECTRONICS: SERIAL	D	CS	54 13489-0-1	L
SCALE —	SHEET 2 OF 2		DIST	

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WIRE TABLE		
ITEM NO.	FROM	TO
74	UA61	UA59
	UA62	UA59
	UA26	UA27
	UA15	UA26
	UA18	UA20
	UA21	UA23
	UA34	UA32
	UA36	UA37
	UA39	UA40
	UA41	UA43
	UA7	UA8
	UA28	UA29
74	UA46	UA47





NOTES:
1. REF. DES. C18 IS NOT USED.
2. FINE LINE, 8 MIL-LINE 8 MIL-SPACE.
3. W6 & W8 ARE OPTIONAL

STEP E	↑ Y AXIS 0 STEP 0 TIMES
REPEAT	→ X AXIS 5250 STEP 1 TIMES

CHK	CHANGE NO	REV	
	REVISED & REDRAWN M7142-MK003	C	N.Sansonetti 7/18/79
			B.FILGATE 8/7/79
	M7142-HK004	D	N.Sansonetti 9/7/79
			B.FILGATE 11/6/79
	M7142-MK005	E	N.Sansonetti 3/4/80
			B.FILGATE 3/11/80
	M7142-MK6	F	N.Sansonetti 7/11/80
			W.AUGER 7/29/80

ETCH REV. C-P1

SIGNATURES	DATE
DRN.	2/13/79
CHK'D.	2/20/79
MECH. ENG.	3/30/81
PROJ. ENG. B. FILGATE	3/30/81
PROD. WILLIAM J BARTON	3/30/81
SCALE 2/1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. B-DD-M7142-Ø	

digital

TITLE SERIAL VIDEO BD.

SIZE	CODE	NUMBER	REV
D	UA	M7142-Ø-Ø	F

DUA M7142-Ø-Ø F

1 MS# 301670

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REWORK INSTRUCTIONS M7142-MKØØ4

WIRE ADDS SIDE 1 AS SHOWN (P/N 9105740-55).

Ø-1 FROM E56-5 TO PTH ABOVE W7.

REWORK INSTRUCTIONS M7142-MKØØ6:

FOR ETCH CUTS REFER TO D-EC-5013895-Ø-Ø.

COMPONENT DELETE:

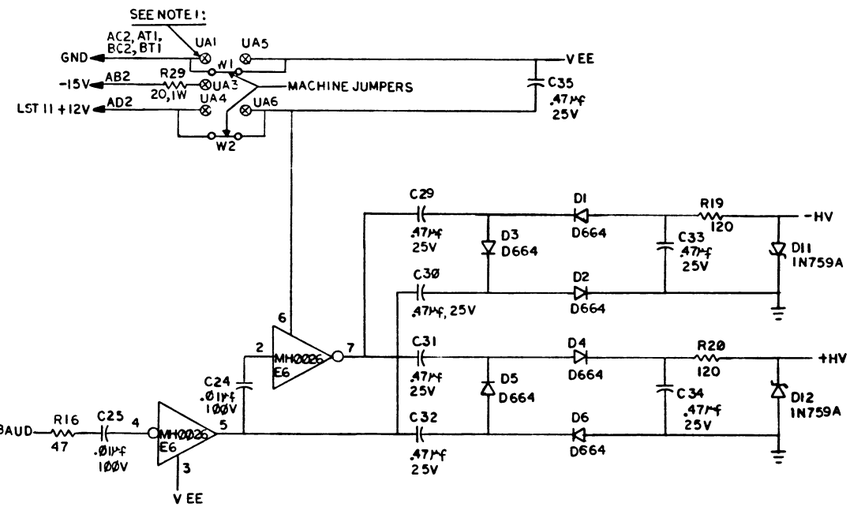
Ø6-2. DELETE W3 P/N(9ØØ9185-ØØ).

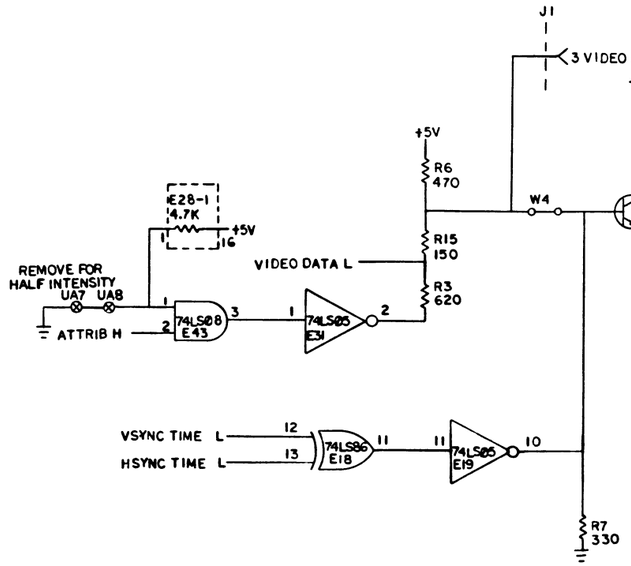
COMPONENT ADDS:

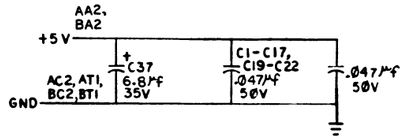
Ø6-3. ADD WW POST UA46 AT W3-1 P/N(9ØØ9217-ØØ).
Ø6-4. ADD WW POST UA47 AT W3-2. P/N(9ØØ9217-ØØ).
Ø6-5. ADD CAP., C39, 100 pF, P/N(1Ø-ØØØ16-ØØ) FROM E23-3 TO E23-7 & SLEEVE LEADS OF C39 WITH P/N 9107278-00.

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POWER OPTIONS	
SUPPLY	W1 INSTALLED OR JUMPER UA1 TO UA5
+ 12VDC	W2 INSTALLED OR JUMPER UA4 TO UA6.
- 15VDC	W1 REMOVED AND JUMPER UA3 TO UA5
	W2 REMOVED AND JUMPER UA1 TO UA6







W4	VIDEO OPERATION
IN	RS170
OUT	HI-Z

M7142 IC POWER PIN ASSIGNMENTS

IC	+5V	GND	+HV	-HV
14 PIN ICS	14	7	—	—
16 PIN ICS EXCEPTION: LS76	16 5	8 13	— —	— —
9636	—	4	8	5
555	8	1	—	—
9637	1	4	—	—
6402	1	3	—	—
2114-2	18	9	—	—
E52, XE53	24	12	—	—
B1-Ø1	20	10	—	—

NOTES:
1. ⊗ DENOTES #30 WIRE WRAP POST.
2. UNLESS OTHERWISE SPECIFIED:
 (A) RESISTOR VALUES ARE EXPRESSED IN OHMS, 1/4W, 5%.
3. NC DENOTES NO CONNECTION.

REVISIONS			
SYM	CHANGE NO.	REV.	
	M7142-MK001	A	H.Simmons 13-JAN-79 B.FILGATE
	M7142-MK002	B	H.Simmons 20-SEP-79 B.FILGATE
	M7142-MK003	C	H.Simmons 31-DEC-79 B.FILGATE
	IN7142-MK004	D	H.Simmons 9-APR-80 B.FILGATE
	M7142-MK005	E	H.Simmons 24-MAR-81 B.FILGATE
	M7142-MK006	F	H.Simmons 02-NOV-82 W.AUGER

POWER SUPPLY AND VIDEO OUTPUT STAGE

DRN. H.Simmons	08-JAN-79	FIRST USED ON	digital
CHK'D J.Falkowski	12-JAN-79		
ENG. Bruce Zeh	9-1979	TITLE	
PROJ. ENG. B.FILGATE	4-1-1980	SERIAL VIDEO MODULE	
PROD. W. BARTON	16-JUNE-81		
NEXT HIGHER ASSY.			
D-UA-M7142-Ø-Ø		SIZE D	CODE CS
SCALE		NUMBER M7142-Ø-1	REV. F
SHEET 1 OF 8		DIST.	

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W6	W7	W8	REMOTE INIT FUNCTION
OUT	OUT	IN	NONE
IN	OUT	IN	BREAK (FE)
OUT	IN	OUT	FF RECEIVE
IN	IN	OUT	FF OR BREAK (FE)

INIT L
74LS279 E22
FF STRB L
W7
W8
W6
FE H
74LS368 E11
R17 240
C36 .047 MF 50V
74LS132 E20
INIT H
+5V E28-13 4.7K
+5V E28-6 4.7K
C23 10 MF 20V
+5V E49-6 4.7K
74LS04 E12
N TEST L

+5V E28-12 4.7K
SPARE

38400 BAUD
INIT H
N TEST L
74LS368 E11
74LS393 E4
CLK1
CLK2
19200 BAUD
9600 BAUD
4800 BAUD
2400 BAUD
1200 BAUD
600 BAUD
300 BAUD
150 BAUD

C27 33 PF 100V
13.5168MHZ Y1
74LS04 E17
C28 56PF 100V
R8 680
R9 680
74LS04 E12
74LS368 E11
N TEST L
+5V
74LS161 E2
CLR
LD
CLK
CNT EN
CRY EN
CY
DOT CLK L
COL1H
COL0H
COL2H
INIT L
74LS161 ÷11 E1
74LS04 E12

+5V
R12 7.5K
R13 5.6K
R31 1.2K
555 E51
VCC
DCG
R
OUTPUT
TRIG
THRESH
CR
C38 39 MF, 10V
C26 .01 MF 100V
≈150MS
≈350MS
WINK GATE DRIVE L

CLOCKS

DRN.			FIRST USED ON
CHK'D			
ENG.			TITLE
PROJ. ENG.	BFILGATE		SERIAL VIDEO MODULE
PROD. W.	BARTON		
NEXT HIGHER ASSY.	D-UA-M7142-0-0		
SCALE			SIZE D CODE CS NUMBER M7142-0-1 REV. F
SHEET	2 OF 8		DIST.

D CS M7142-0-1 F

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Y AXIS REFRESH

V BLANK H
H SYNC TIME L
SCROLL CONTROL H
74LS02 E24
INIT L
74LS161 E8
DA DB DC DD QA QB QC QD CLR LD CLK CNT EN CRY EN CY
RY1 H
RY2 H
RY3 H
RY4 H
NC
74LS32 E20
74LS32 E21
+5V
E49 4.7K
WRITE TIME H
74LS04 E30
D7
BLANK L
D8
H BLANK H
74LS05 E31
VIDEO HOLD L
E28 4.7K
74LS161 E14
ROW0 H
ROW1 H
ROW2 H
74LS10 E16
RY0 H
H BLANK H
INIT H
74LS393 E3
CLKA CLRA QA QB QC QD CLRB CLKB
(SCAN 256)
(SCAN 200)
V BLANK H
V BLANK L
74LS279 E10
74LS04 E30
74LS10 E16
74LS27 E9
74LS04 E12
V SYNC TIME L
V SYNC TIME H
J1
≈ 520µS
60HZ
VERTICAL DRIVE L

V SYNC TIME

X AXIS REFRESH

RX0 H
RX1 H
RX2 H
RX3 H
74LS161 E62
INIT L
SHIFT LOAD TIME L
+5V
74LS161 E61
RX4 H
RX6 H
NC
RX5 H
RX0 H RX2 H RX6 H
74LS10 E34
74LS04 E17
SHIFT LOAD TIME H
INIT L
74LS76 E36
H BLANK L
H BLANK H
+5V
RX0 H RX2 H
RX6 H
74LS11 E40
RX1 H RX3 H
COL 80 H
RX0 • RX2 • RX6 H
RX6 H RX4 H RX3 H
74LS20 E26
RX5 H
74LS04 E17
74LS279 E22
H SYNC TIME L
RX3 H
H BLANK CLR L

H BLANK L
RX4 H
RX3 H
74LS10 E16
74LS279 E10
H SYNC TIME L
74LS368 E11
HORIZONTAL DRIVE H
15360 HZ
≈ 27µS

SYNC MONITOR CONTROL

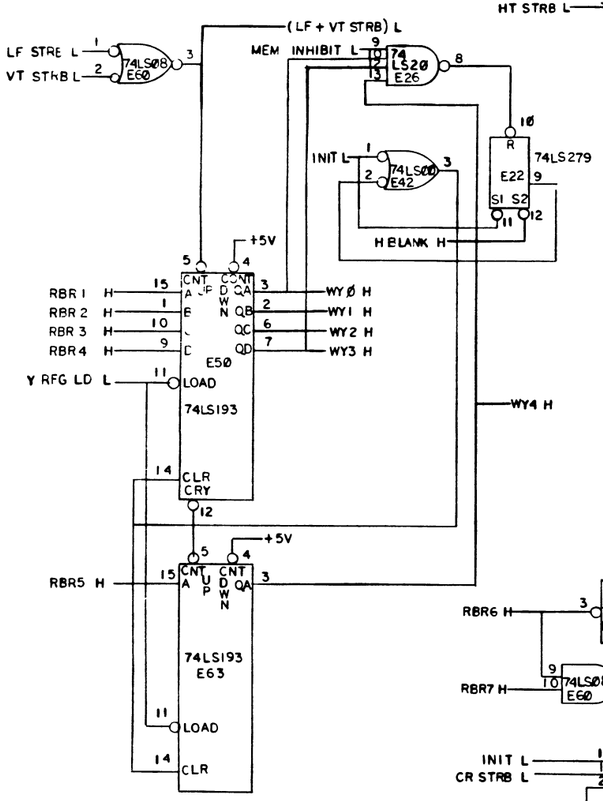
DRN TH Symmons	9 Jan 79	FIRST USED ON	digital
CHK'D Tom Hastings	12 JAN 79		
ENG Bruce Eyer	4-JAN-79	TITLE	SERIAL VIDEO MODULE
PROJ ENG BFILGATE	4-JAN-79		
PROD W BARTON	18 JAN 79		
NEXT HIGHER ASSY.			
D-UA-M7142-0-0		SIZE D	CODE CS NUMBER M7142-0-1 REV. F
SCALE			
SHEET 3 OF 8		DIST.	

REVISIONS: REV. / CHANGE NO. / CHK

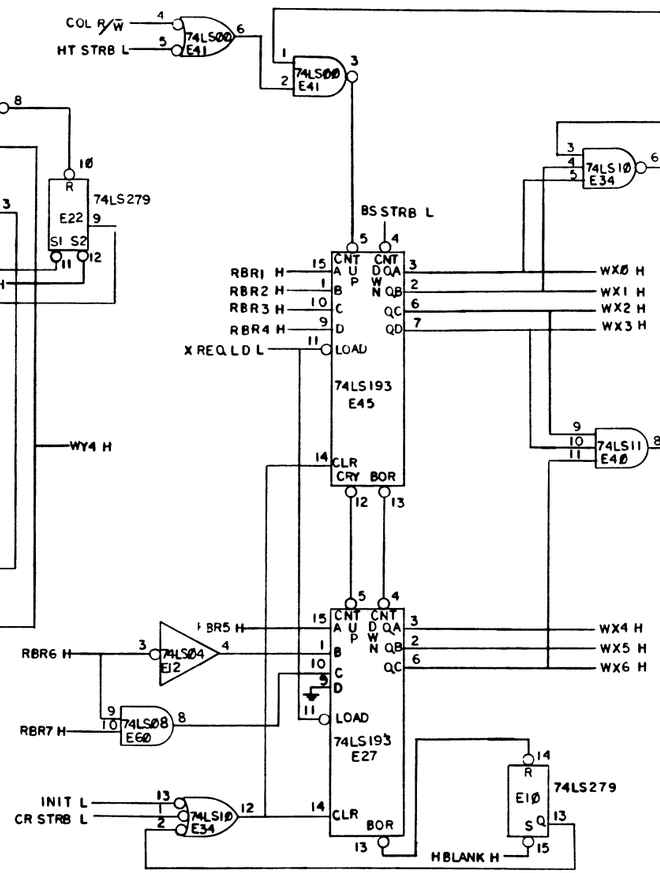
D-CS-M7142-0-1 REV. F

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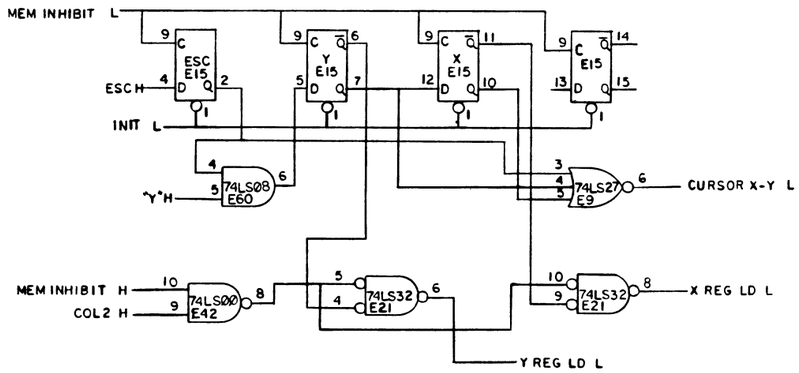
Y AXIS CURSOR



X AXIS CURSOR



X-Y LOAD
74LS175



CURSOR REGISTERS

DRWN	15-DEC-78	FIRST USED ON	20-0250
CHK'D	12-JAN-79	TITLE	SERIAL VIDEO MODULE
ENGR	19-JAN-79		
PROJ ENGR	FILGATE 24-JAN-79		
PROG MGR	BARTON 31-JAN-79		
NEXT HIGHER ASSY.	D-UA-M7142-0-0	SIZE D	CODE CS
SCALE		NUMBER M7142-0-1	REV. E
SHEET	4 OF 8	DIST.	

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TO / FROM	8 DATA BITS NO PARITY	7 DATA BITS EVEN PARITY	7 DATA BITS ODD PARITY
UA61	UA59	UA60	UA60
UA62	UA59	UA60	UA60
UA63	——	UA59	UA60

●DENOTES #30 WIREWRAP POST

BAUD RATE SELECTION

- 150 BAUD — ●UA9
- 300 BAUD — ●UA10
- 600 BAUD — ●UA11
- 1200 BAUD — ●UA12
- 2400 BAUD — ●UA13
- 4800 BAUD — ●UA14
- 9600 BAUD — ●UA15
- 19200 BAUD — ●UA16
- 38400 BAUD — ●UA17

INSTALL FOR LOCAL COPY

UART 2113937 E54

PARITY INH / EIGHT DATA BITS — EVEN PARITY

MEM INHIBIT L

RRD H

T UART H

BREAK L

FE

FE H

RCLK

TCLK

INIT H

KB STRB H

RCV DATA −

RCV DATA +

KB1 KB2 KB3 KB4 KB5 KB6 KB7 KB8

TBR1 H(LSB) TBR2 H TBR3 H TBR4 H TBR5 H TBR6 H TBR7 H TBR8 H

DR H

RBR1 H(LSB) RBR2 H RBR3 H RBR4 H RBR5 H RBR6 H RBR7 H RBR8 H

CUSOR XY L

N TEST L

MEM INHIBIT L

ESC H

Y H

NON DSPLY L

COL2 H

COL1 H

XMT DATA +

XMT DATA −

CLK

SPARES

OPERATION MODE	WIRE WRAP JUMPERS			
	UA18	UA21	UA34	UA36
RS423	UA20	UA23	UA32	UA37
20 MA	UA19	UA22	UA33	UA35

M7142 COMMUNICATION

DRWN H Davis/Moore	08-Jan-79	FIRST USED ON
CHK'D Lally	4-19-79	
ENG Blum	4-19-79	TITLE
PROD. ENG. S FILGATE	3-Jan-81	SERIAL VIDEO MODULE
PROD. W BARTON	30-Jan-81	
NEXT HIGHER ASSY.		
D-UA-M7142-0-0		SIZE D · CODE CS · NUMBER M7142-0-1 · REV. F
SCALE —		
SHEET 5 OF 8		DWG.

D CS M7142-0-1 F

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+5V
E28-7
4.7K
ROW R/W
RX4 H
74LS201 E29
AY4 L
74LS04 E30
WY4 H
74LS257 F64
WX0 H
RX0 H
WX1 H
RX1 H
WX2 H
RX2 H
WX3 H
RX3 H
OUT CONT S0
N TEST L
COL R/W
ADRS 0 H
ADRS 1 H
ADRS 2 H
ADRS 3 H
74LS257 E33
WX4 H
RX4 H
WX5 H
RX5 H
WX6 H
RXC H
AY4 L
(AX4) H
(AX5) H
(AX6) H
N TEST•AY4 L
E55
74S471
MEMORY MAP
23-044B1-00
AD A
AD B
AD C
AD D
AD E
AD F
AD G
AD H
ADRS 4 H
ADRS 5 H
ADRS 6 H
ADRS 7 H
ADRS 8 H
ADRS 10 H
ADRS 12 I
74LS257 E36
WY0 H
RY0 H
WY1 H
RY1 H
WY2 H
RY2 H
WY3 H
RY3 H
ROW R/W
(AY0 H)
(AY1 H)
(AY2 H)
(AY3 H)
N TEST•AY4 L
S2 S1
N TEST L
WRITE L
RRD H
74LS74 E12
74LS00 E23
ADRS 10 L
74LS132 E20
ADRS 10 H
+5V
R21 R22 R23 R24 R1 R25 R26 R27
3.9K
RBR 7 H
RBR 6 H
RBR 5 H
RBR 4 H
RBR 3 H
RBR 2 H
RBR 1 H
E57 E58 E65 E59
2114-2
I/O1 I/O2 I/O3 I/O4
WE CS
RATRIB H
RBR 8 H
R30 1.2K
74LS05 E31
DIØ D664
SO STRB L
74LS279 E10
INIT L
SI STRB L
UA38 UA39 UA28 UA40
UA29 UA30
COL Ø H
COL 1 H
COL 2 H
74LS27 E9
BLANK L
74LS04 E17
SHIFT LOAD TIME L
SHIFT LOAD TIME H
74LS00 E42
SHIFT/LOAD
23120E2-00
E52
ROW Ø H
ROW 1 H
ROW 2 H
CE
SEE ROM SELECTION TABLE BELOW
UA47
UA46
XE53 SOCKET 2716/ 2316
OE CE
DOT CLOCK L
INIT L
SHIFT/LOAD
CLK
CLR
Q H
DOT VIDEO H
E46
74LS166
CLK SER
INH INP
E49-11 4.7K
E49-15 4.7K
SPARES

ATTRIBUTE CONTROL		
TO / FROM	SI/SO	BIT 8
UA40	UA39	UA38

CHARACTER SET OF SELECTED ROM	JUMPER
FIRST CHARACTER SET	UA28 — UA29
SECOND CHARACTER SET	UA28 — UA30
ATTRIBUTE SELECTED CHARACTER SET	UA28 — UA40

ROM SELECTION TABLE	
E52	CONNECT UA46 TO UA47.
XE53	CONNECT UA47 TO UA30.

MEMORY

REVISIONS		
REV.	CHANGE NO.	CHK

DRN		
CHK'D		
ENG		
PROJ. ENG.	BFILGATE	
PROD	WBARTON	
NEXT HIGHER ASSY.	D-UA-M7142-0-0	
SCALE		
SHEET	6 OF 8	

FIRST USED ON
digital
TITLE
SERIAL VIDEO MODULE
SIZE D | CODE CS | NUMBER M7142-0-1 | REV. F
DIST.

1978

8136 E39

RX0 H 2
WX0 H 1
RX1 H 4
WX1 H 3
RX2 H 6
WX2 H 5
RX3 H 10
WX3 H 11
RX4 H 12
WX4 H 13
RX5 H 14
WX5 H 15
9
7

+5V 16 E28-8 4.7K 8

8136 E32

RX6 H 2
WX6 H 1
RY0 H 4
WY0 H 3
RY1 H 6
WY1 H 5
RY2 H 10
WY2 H 11
RY3 H 12
WY3 H 13
RY4 H 14
WY4 H 15
9
7

VIDEO HOLD L — D13 D664

74LS379 E37
13 D Q 15
9 C G Q 14
1
DOT CLOCK L
SHIFT LOAD TIME L

+5V 16 E49-14 4.7K 14

REMOVE FOR ALL REVERSE — W5

INSTALL FOR BLINK

INSTALL FOR REVERSE
UA41 UA42 UA43
ATTRIB L

+5V 16 E28-14 4.7K 14

74LS86 E18 (1, 2, 3)
74LS86 E18 (4, 5, 6)

CURSOR L

+5V 16 E28-4 4.7K 4

74LS379 CURSOR TIME E37
5 D Q 7
9 C G Q 6
1
DOT CLOCK L
SHIFT LOAD TIME L

WINK GATE DRIVE L

74LS32 E21 (12, 13, 11)
74LS00 E23 (9, 10, 8)
DOT VIDEO H

74LS86 E18 (9, 10, 8)
74LS05 E19 (13, 12)
VIDEO DATA L

74LS00 E23 (12, 13, 11)
CURSOR L

RATRIB H 9
BLANK L 10
74LS08 E43 (8)

74LS379 ATTRIB LATCH E37
4 D Q 2 — ATTRIB H
9 C G Q 3 — ATTRIB L
1
DOT CLOCK L
SHIFT LOAD TIME L

VIDEO HOLD L — D9 D664

UA44
UA45
INSTALL TO INHIBIT CURSOR

74LS04 E17 (5, 6)
SPARE

74LS379 E37
12 D Q 10
9 C G Q 11
1
DOT CLOCK L
SHIFT LOAD TIME L
SPARE

74LS74 E28 (1, 2, 3, 4, 5, 6)
10, 12, 9, 11, 13
SPARE

CURSOR & ATTRIBUTE LOGIC

DRWN	H. Dennison	22 DEC 78	
CHK'D		17 Nov 78	
ENG.		4-19-79	
PROJ. ENG.			
PROD'N	BARTON		
NEXT HIGHER ASSY.	D-UA-M7142-0-0		
SCALE			
SHEET	7 OF 8		

SERIAL VIDEO MODULE

SIZE D | CODE CS | NUMBER M7142-0-1 | REV. F | DIST.

D CS M7142-0-1 F

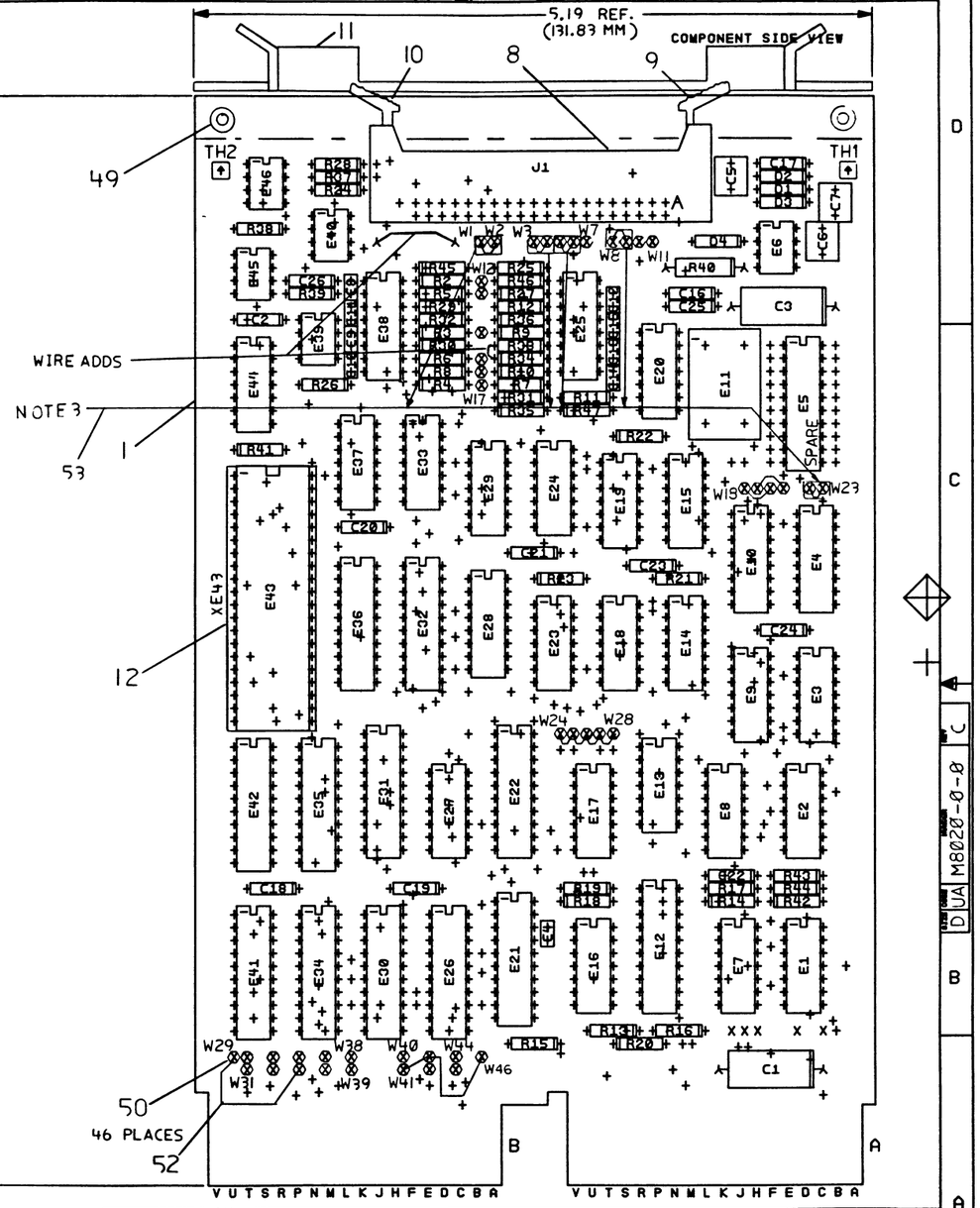
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DR H
COL 8Φ H
74LS08 E43
MEM INHIBIT H
+5V
74LS74 MEM INHIBIT
E48
74LS02 E24
RRD H
74LS74 MEM DATA WRITE
COL R/W̄
SHIFT LOAD TIME L
NON DSPLY L
MEM INHIBIT L
INIT L
74LS74 V BLANK L
E13
74LS05 E31
RATRIB H
74LS74 CLEAR MEMORY
74LS05 E19
COL2 H
74LS00 E41
WRITE L
74LS00 E42
WRITE TIME H
H BLANK H
74LS74 ERASE NEW LINE
E25
74LS74 ERASE
74LS08 E43
ROW R/W̄
LF STRB L
WY3 H
WY4 H
74LS00 E23
C39 100 pF
74LS279 SCROLL ENB
E22
INIT L
(LF + VT STRB) L
74LS00 E41
SET LF QUEUED L
74LS02 E66
74LS74 SCROLL PEND
E68
INIT H
LF QUEUED L
+5V
E49-13 4.7K
LF QUEUED L
V BLANK L
74LS01 E29
(LF + VT STRB) L
LF QUEUED H
H BLANK L
74LS01 E29
74LS76 PULSE SYNC
E36
SHIFT LOAD TIME L
74LS161 E67
DA DB DC DD
QA QB QC QD
CLR LD CLK CNT EN CRY EN CY
INIT L
74LS74 SCROLL
E35
SCROLL CONTROL H
SHIFT LOAD TIME H
≈ 5ΦΦ NS
74LS74 E35
LF QUEUED L
LF QUEUED H
HIGH SPEED SCROLL WHEN HIGH, SMOOTH OTHERWISE.
SET LF QUEUED L

MEMORY & SCROLL CONTROL

DRN	Peg Conroy 4-JUN-79	FIRST USED ON
CHK'D	J. Talbot 27 JUN 79	
ENG.	Bruce Hyatt 27 JUN 79	TITLE
PROJ. ENGR	FILGATE	SERIAL VIDEO MODULE
PROD.	W BARTON	
NEXT HIGHER ASSY.		
D-UA-M7142-Φ-Φ		SIZE D CODE CS NUMBER M7142-Φ-1 REV. F
SCALE		
SHEET 8 OF 8		DIST.

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NOTES: 1. E5 IS A SPARE IC LOCATION.
2. C4 IS NOT USED.
3. WIRE WRAP AT THESE LOCATIONS MAY BE REPLACED BY JUMPERS. 12-18783-00 AS REQUIRED.

STEP E	↑ Y AXIS .44 STEP .44 TIMES
REPEAT	→ X AXIS 5.250 STEP 1 TIMES

CHK	CHANGE NO	REV
JF	M8020-UA-COA	B
	H.Zimmerman 7/14/80	
	J. McCOY 10/6/80	
JF	M8020-MK3	C
	H.Zimmerman 7/11/84	
	M. LAWRENCE 2/25/85	

ETCH REV. B

SIGNATURES	DATE
DRN. M. Farabee	3/-1/80
CHK'D. G. Pathenakis	3/-10/80
MECH. ENG. L. M. Cox	5/21/80
PROJ. ENG. [illegible]	5/21/80
PROD. R. Farland	6/24/80

digital

TITLE DPV 11

SIZE	CODE	NUMBER	REV
D	UA	M8020-0-0	C

SCALE 2/1
SHT. 1 OF 2
NEXT HIGHER ASSY. K-DD-M8020-0

1 MS# 302225

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M8020 REWORK:

ETCH CUT SIDE 1:

1. REFER TO D-EC-5013958-0-0

WIRE ADD SIDE 1:

1. ADD WIRE FROM PIN 2 OF R33 TO PIN 1 OF R34.
 (USE #30 AWG INSULATED WIRE, P/N 9105740-55).
2. ADD WIRE FROM LARGE PAD, NEXT TO E40 PIN 6, TO
 LARGE PAD NEXT TO W1

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
DPV11	D	UA	M8020-0-0	C
SCALE NONE / SHEET 2 OF 2	DIST.			

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NOTES:
1. NOS. IN PARENTHESIS ARE PINS FOR THE 20 PIN IC LOCATION. THE DC003 IS AN 18 PIN IC WITH PIN ONE OF THE DC003 MATCHING PIN ONE OF THE IC LOCATION.
2. JUMPER PINS ARE NOT ON THE PARTS LIST. RESERVED FOR FUTURE USE.
3. ADDRESS SHOWN IS 160010. VECTOR SHOWN IS 0300.
4. E38 AND E25, (P/N 19-15123-02) MAY BE TI 26LS32-2 OR AMD 26LS34.

ADDRESS SELECT
VECTOR SELECT
S1 REC LB
S1 REC HB
S1 XMIT
S3 VECTOR
S1 DA0 H
S1 DA1 H
S1 DA2 H
S1 DA3 H
S1 DA4 H
S1 DA5 H
S1 DA6 H
S1 DA7 H
S1 DA8 H
S1 DA9 H
S1 DA10 H
S1 DA11 H
S1 DA12 H
S1 DA13 H
S1 DA14 H
S1 DA15 H
S1 DIN/H
S1 DIN/L
S1 INIT
S1 SYNC/H
S1 SYNC/L
S1 W REG Ø
S1 R REG Ø
S1 ADDR2
S1 ADDR1
S1 W REG 4
S1 R REG 4
S1 ADDR Ø
S1 WRITE USYNR/T
S1 ENA LB
S1 ENA HB
S1 BYTE OP
S1 INWD/H
S1 DP ENA
S1 IN/OUT
S1 XMIT
S1 ADR Ø
S1 B RPLY/L
S1 600NS/L
S3 SR CLK
S1 DC04-17
S1 DC04-16
S1 DC0415
S1 DC0414
S1 DC04-15
S1 DC04-14
S1 DC04-16
S1 DC04-15
S1 DC04-14
S1 DC04-16
S1 DC04-17
S1 DC0415
B DIN/L
B INIT/L
B SYNC/L
BD OUT/L
BWTBT/L
AR2
AS2
AC2, BC2, AT1, BT1, AM1, BJ1
N.C.

REVISIONS			
ORIG.	CHANGE NO.	REV.	
	M8020-MK0001	B	J. MCCOY
	M8020-MK0002	C	F. BACKES

DRN.		4/29/80
CHK'D		
ENG.		
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.		
B-DD-M8020-0-		
SCALE NONE		
SHEET 1 OF 4		

FIRST USED ON 1103

digital

TITLE
DPV11
LOGIC DIAGRAM
S1

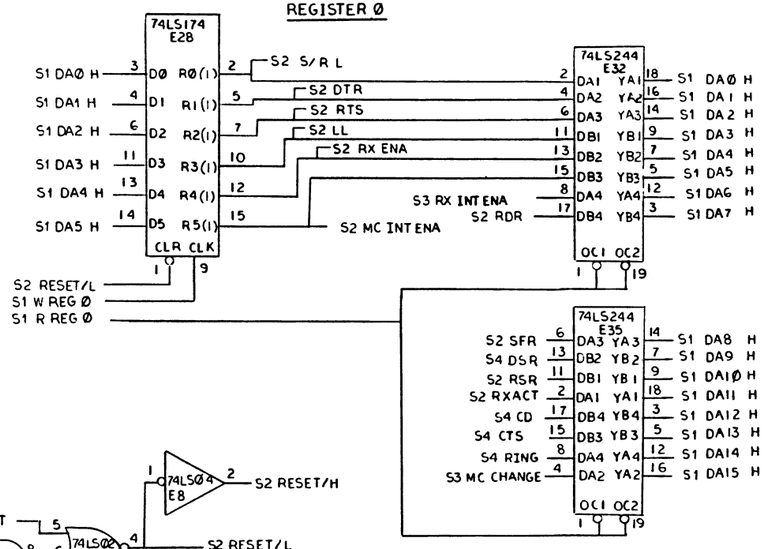
SIZE	CODE	NUMBER	REV.
D	CS	M8020-0-1	C

DIST.

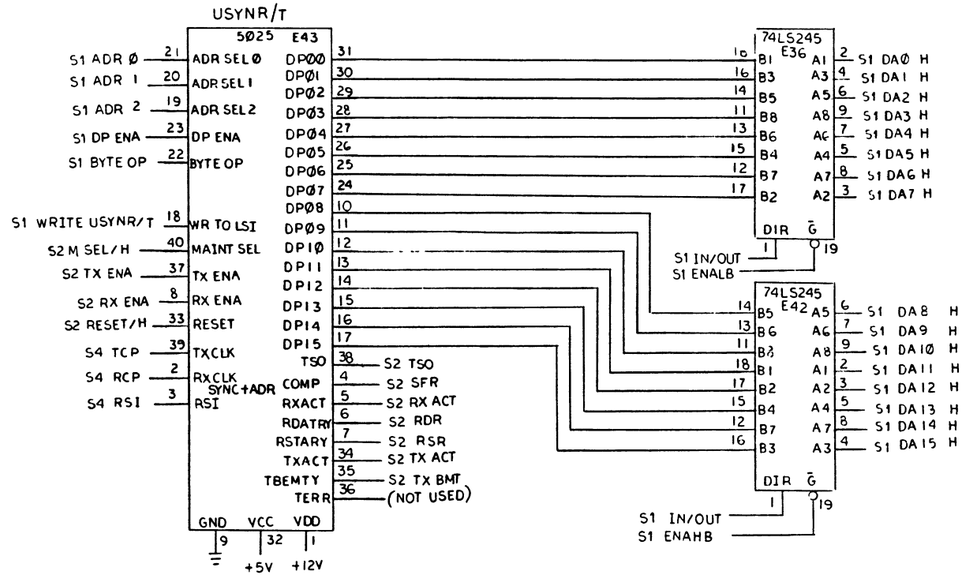
D CS M8020-0-1 C
B

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REGISTER 0



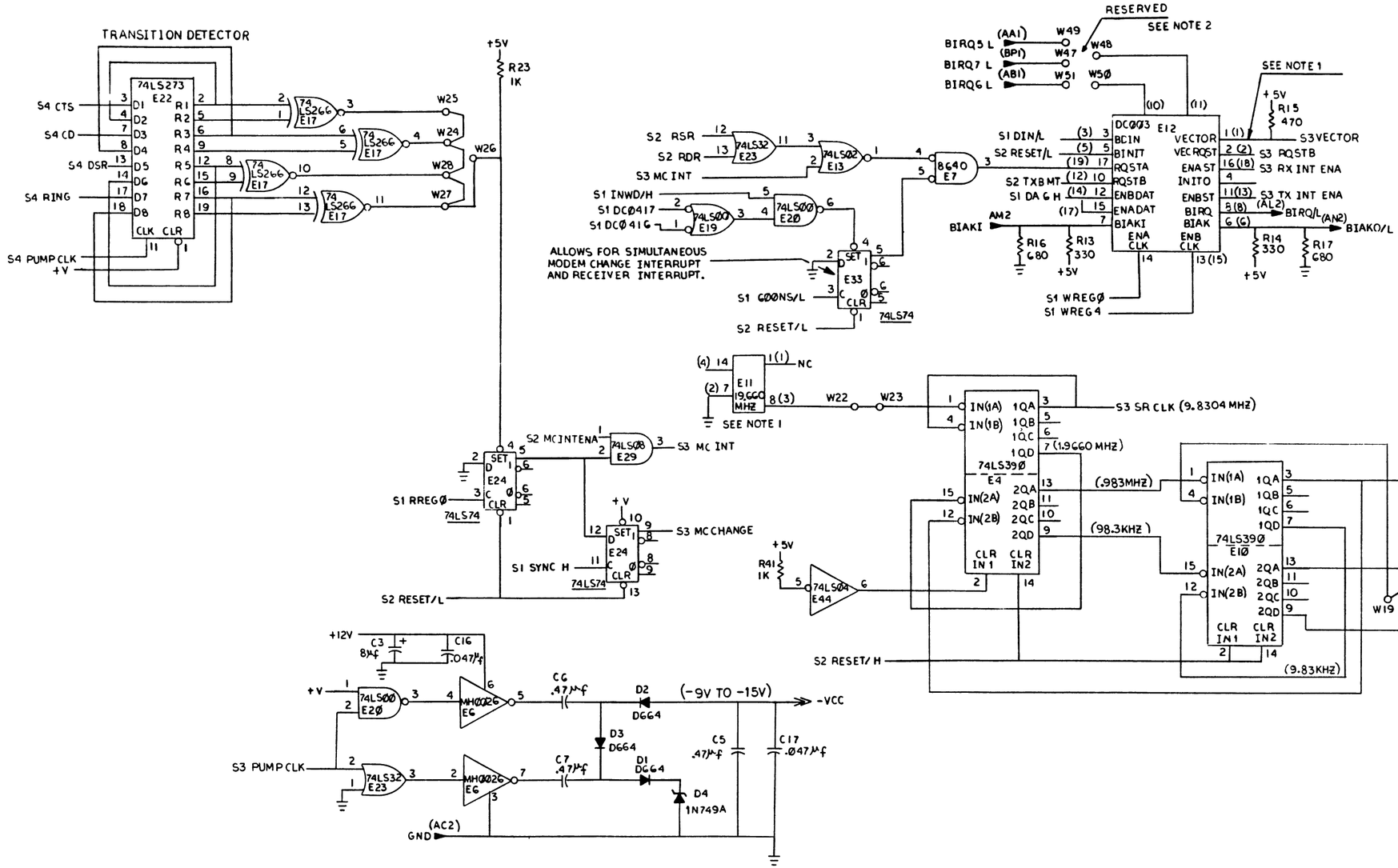
USYNR/T



REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
DPV11, LOGIC DIAGRAM (S2)	D	CS	M8020-0-1	C
SCALE NONE — SHEET 2 OF 4	DIST.			

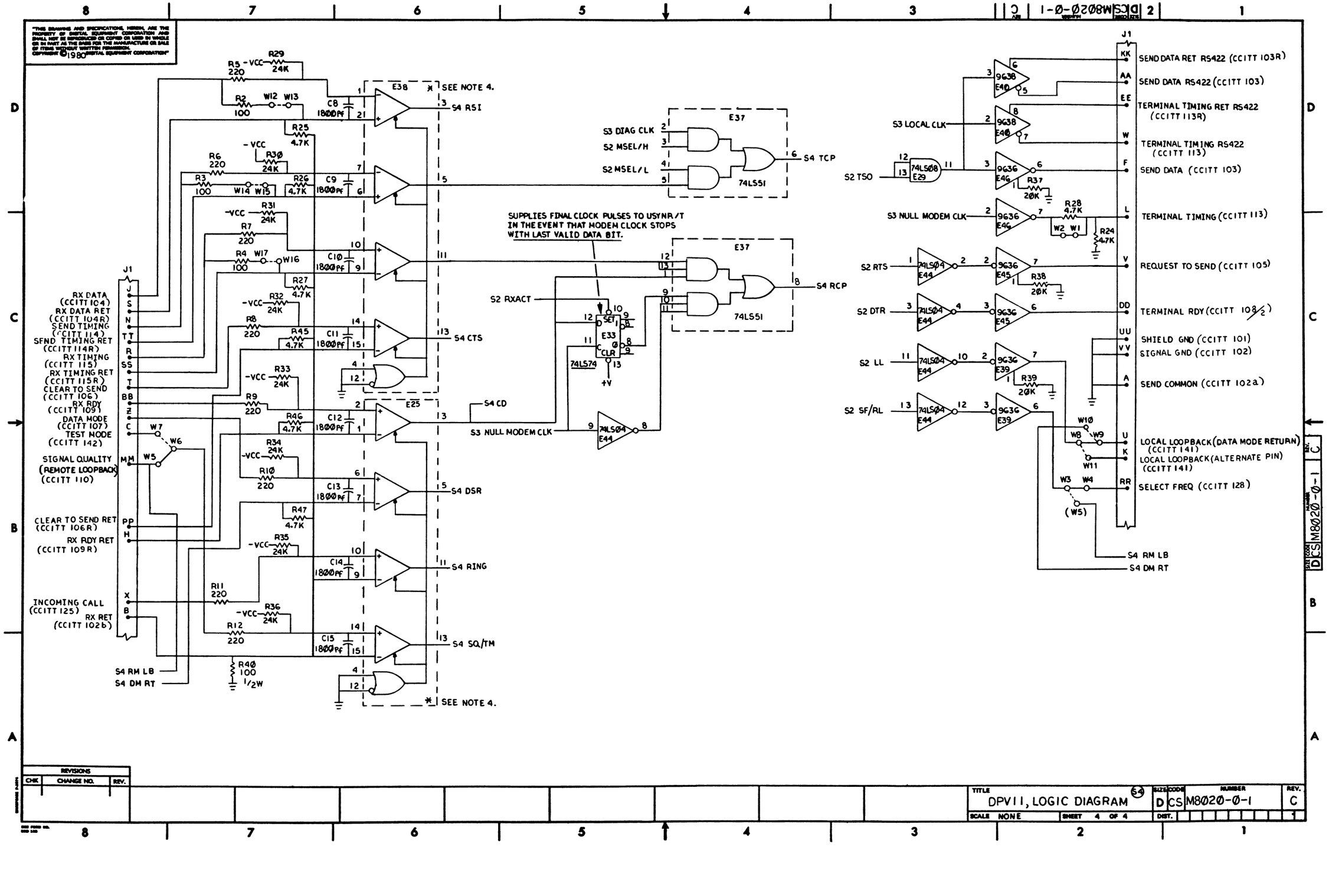
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REVISIONS		
CHK	CHANGE NO.	REV

TITLE		SIZE	CODE	NUMBER	REV.
DPV11, LOGIC DIAGRAM	(S3)	D	CS	M8020-Ø-1	C
SCALE NONE	SHEET 3 OF 4	DIST.			

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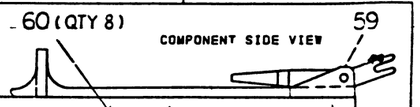
REVISIONS		
CHK	CHANGE NO.	REV.

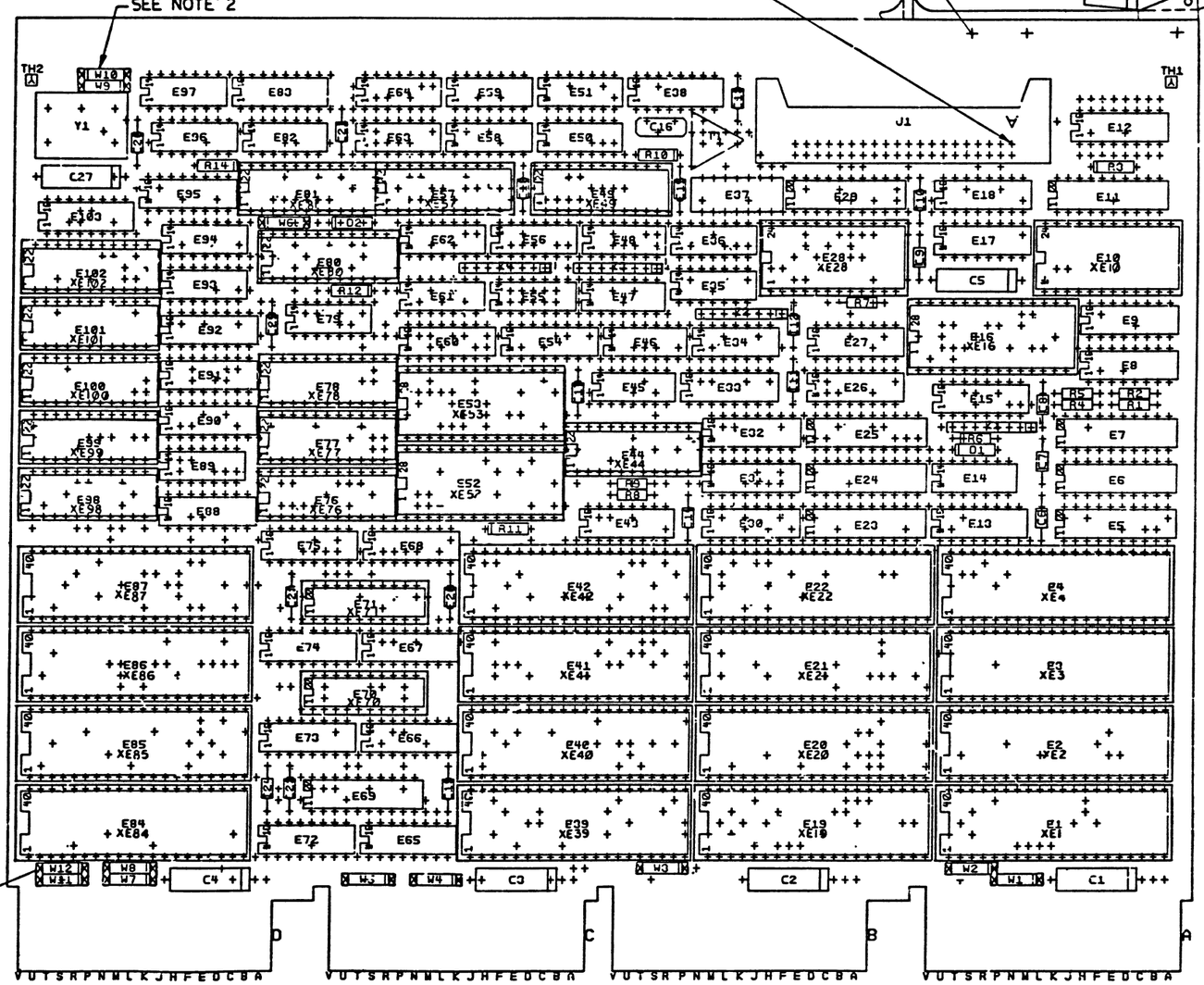
TITLE		SIZE	CODE	NUMBER	REV.
DPV11, LOGIC DIAGRAM (S4)		D	CS	M8020-0-1	C
SCALE NONE	SHEET 4 OF 4	DIST.			

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NOTES CONT

6. PIN "A OR 1" ON J1 IS CUT OUT TO KEY THE CONNECTOR.





NOTES: 1. ITEM *58 COMES IN PAIRS & MIGHT HAVE TO BE CUT TO GO ON EITHER SIDE OF "W" JUMPERS.
2. W10 IS A SPARE JUMPER, BUT IS INSERTED.
3. SPARE LOCATIONS ARE: E12
4. USE ITEM *64 ON W1, W2, W4, W5, W6, W9, W10.
5. W3, W7, W8, W11, W12 ARE USED FOR UBUS OPERATION & MODULE IS NOT BUILT WITH THEM.

STEP E	+ Y AXIS 0	STEP 0 TIMES
REPEAT	→ X AXIS 0	STEP 0 TIMES

CHK	CHANGE NO	REV

ETCH REV. C
P.C. DESIGN DATA REV A

SIGNATURES	DATE
DRN.	11/5/80
CHK'D.	11-14-81
MECH. ENG.	12/16/81
PROJ. ENG.	12/16/81
PROD.	12/16/81

digital

TITLE: FPF-11

SCALE 2/1 | SIZE D | CODE UA | NUMBER M8188-C-0 | REV A

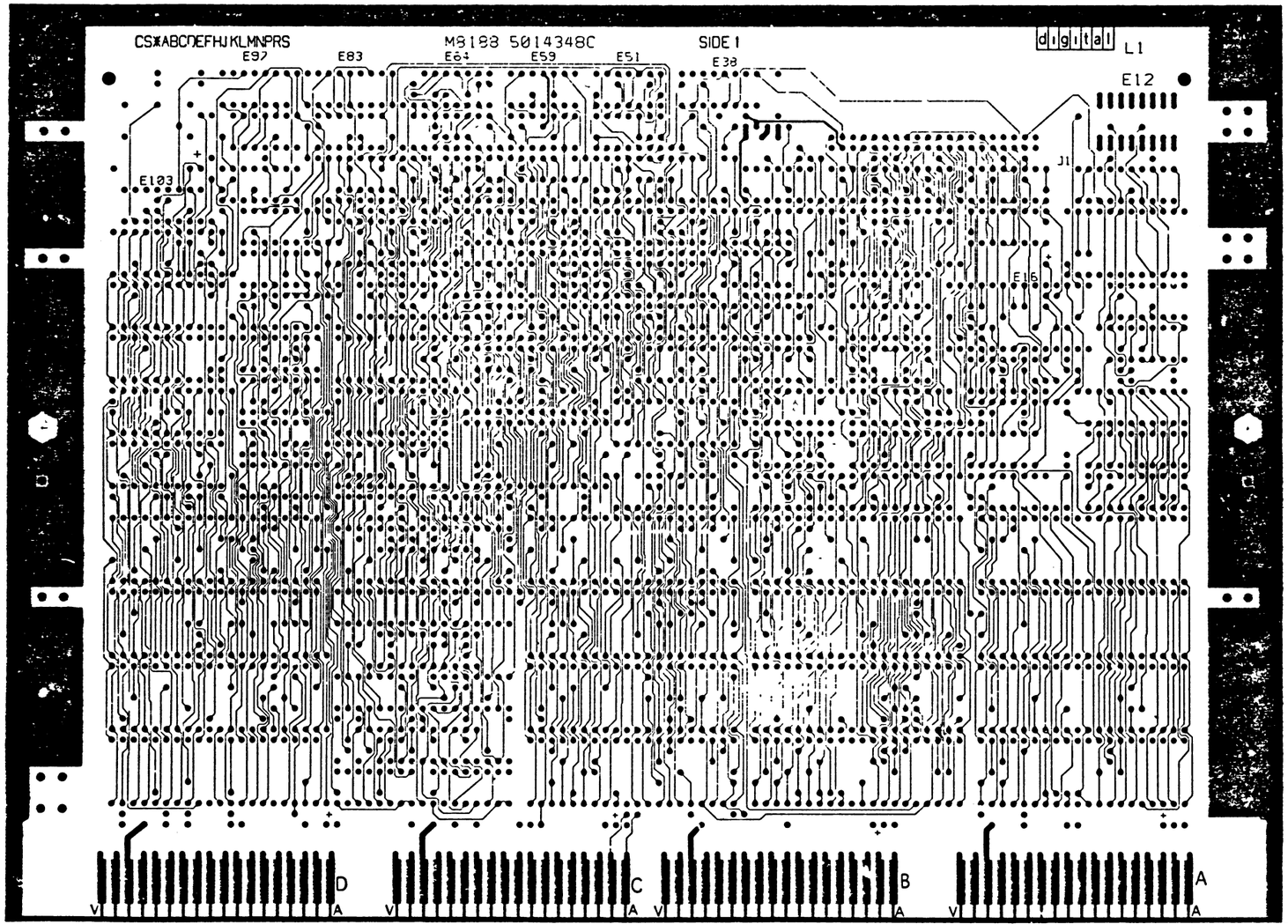
SHT. 1 OF 1

NEXT HIGHER ASSY. B-DD-M8188-0

WO# 19C-27

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LAYER 1

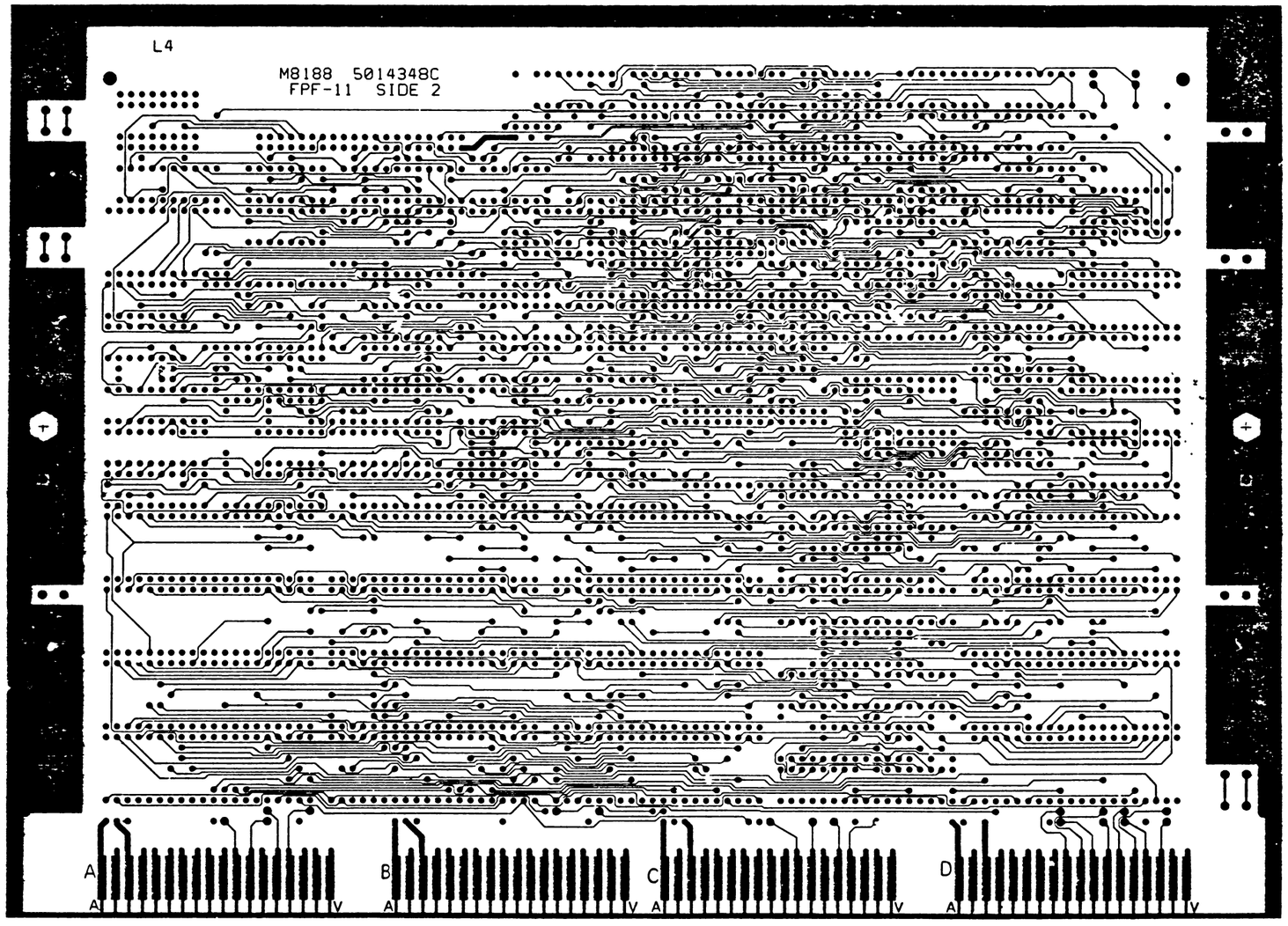


DRN			FIRST USED ON	FPF-11	digital
CHK'D			TITLE	ETCH CUT DRAWING	
ENG					
PROJ ENG					
PROJ MGR					
NEXT HIGHER ASSY.					
0-UA-M8188-0-0			SIZE	CODE	NUMBER / REV.
SCALE 2/1			D	EC	5014348-0-0 / A
SHEET 1 OF 2			DIST		

REVISIONS			
	CHANGE NO	CHK	REV

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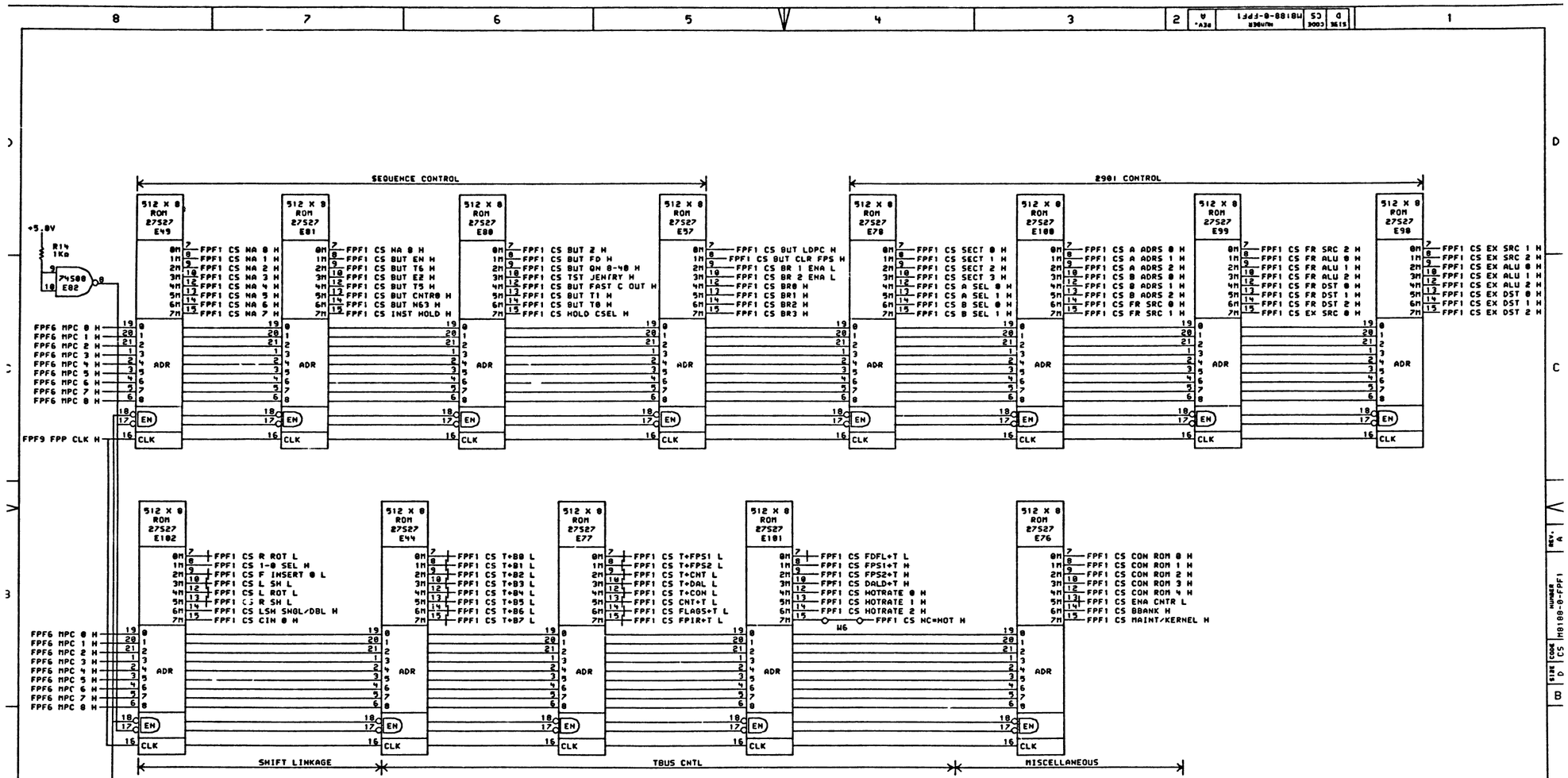
LAYER 4



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
ETCH CUT DRAWING	D	EC	5014348 - 0 -0	A
SCALE 2/1	SHEET 2 OF 2		DIST	

DEC 5014348-0-0 A



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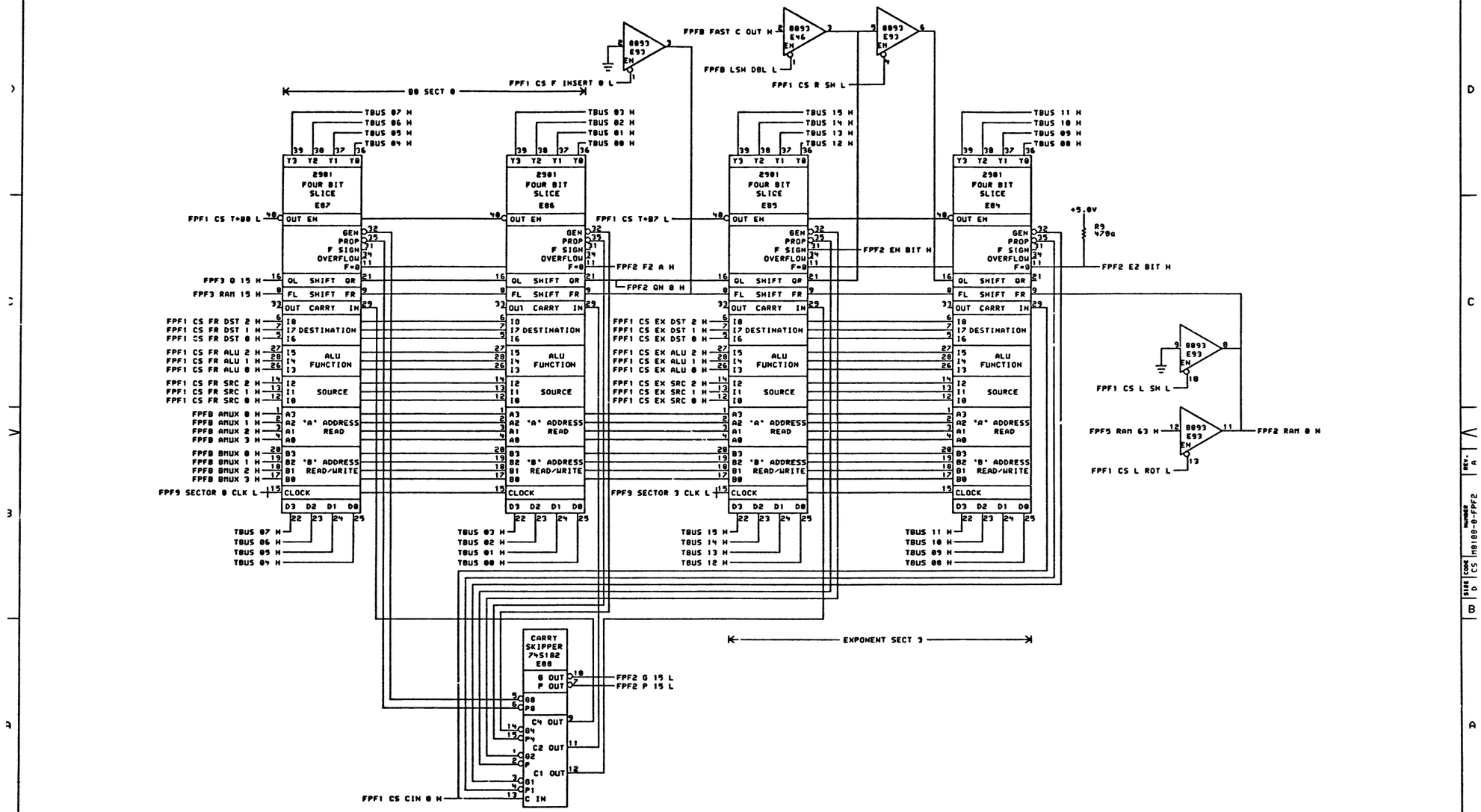
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: S. Lemay
CHK: D. Grant
DATE: 16-FEB-81
ENG: Mark Davis
DATE: 16-FEB-81
DATE:
BOARD LOCATION:
SHEET 1 OF 1
PS:<TOWER>FPF1B.DR4 16-FEB-81 13:14
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FPF11

TITLE: CONTROL STORE

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF1	A



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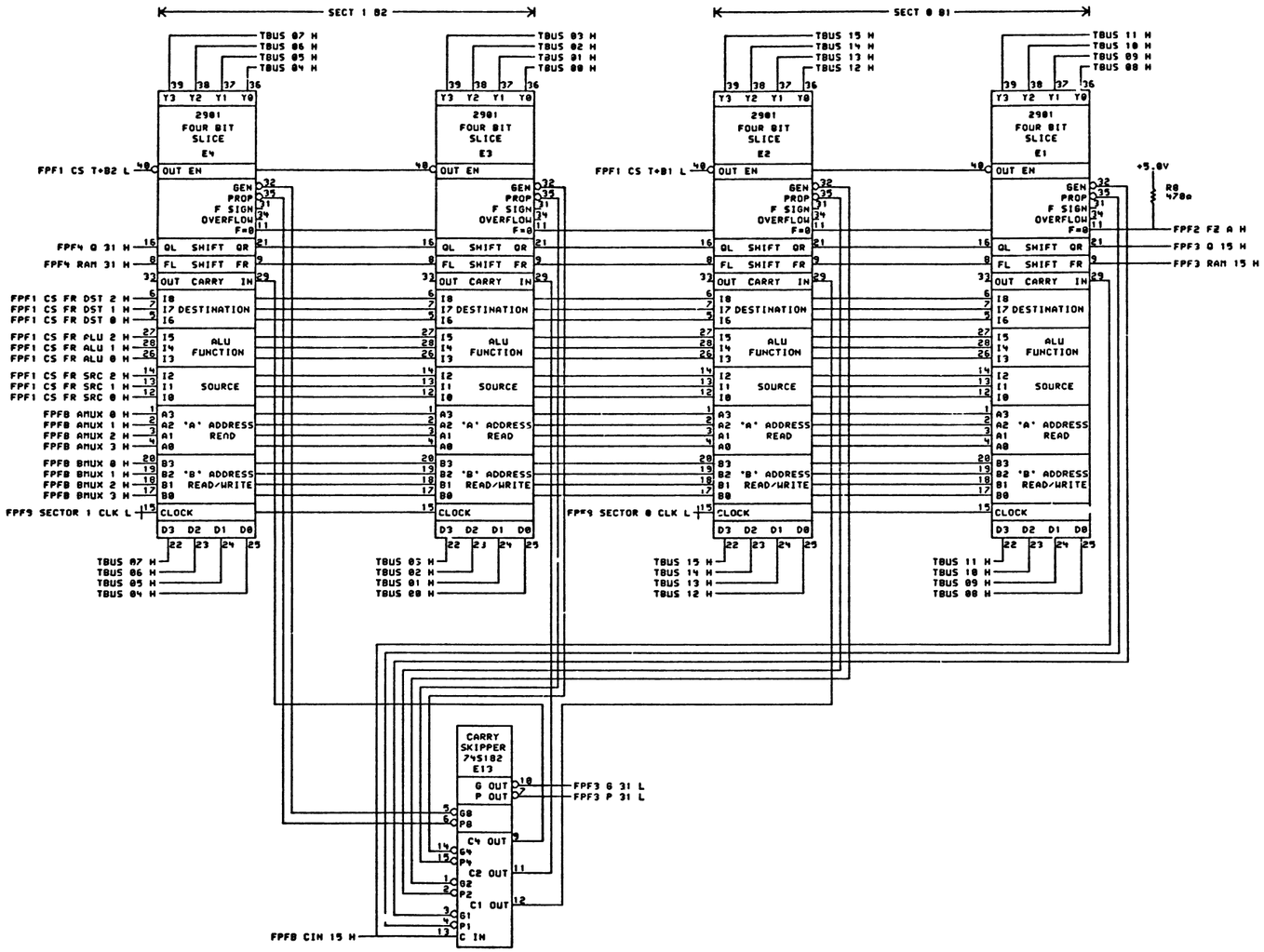
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRW K. Toomey 16-FEB-81
CHK [illegible] 16-FEB-81
ENG [illegible] 16-FEB-81
DATE
BOARD LOCATION:
SHEET 1 OF 1
PS$<TOWER>FPF2B.DRW 16-FEB-81 13:41
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FPF11

TITLE: BYTES 0 & 7

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF2	A



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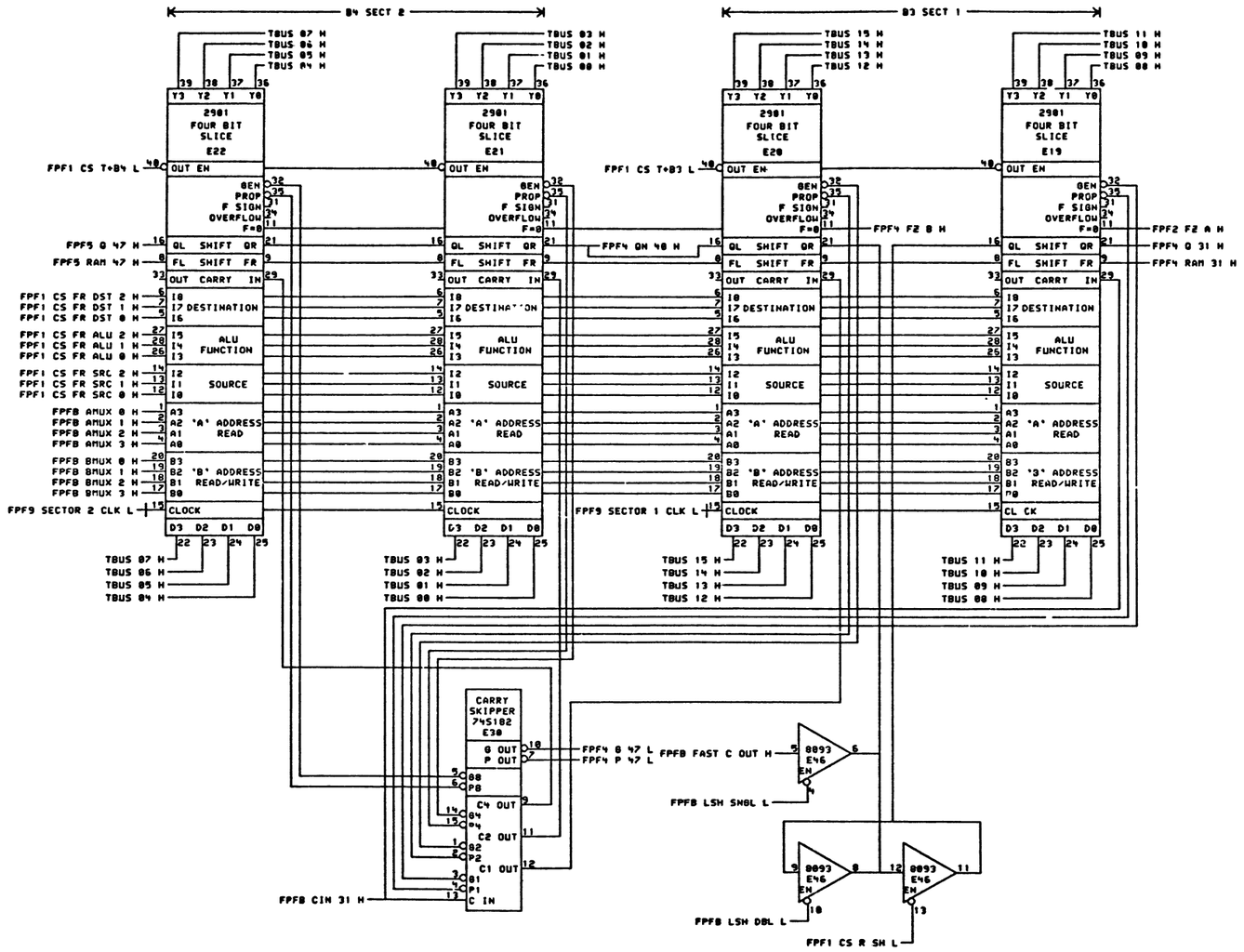
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRW T. Zamolyi 16-FEB-81
CHK'D D. Orf 16-FEB-81
ENG Chuck Downes 16-FEB-81
DATE 16-FEB-81
BOARD LOCATION:
SHEET 1 OF 1
PS:<TOWER>FPF30.DRW 16-FEB-81 13:43
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FPF11

TITLE: BYTES 2 & 1

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF3	A



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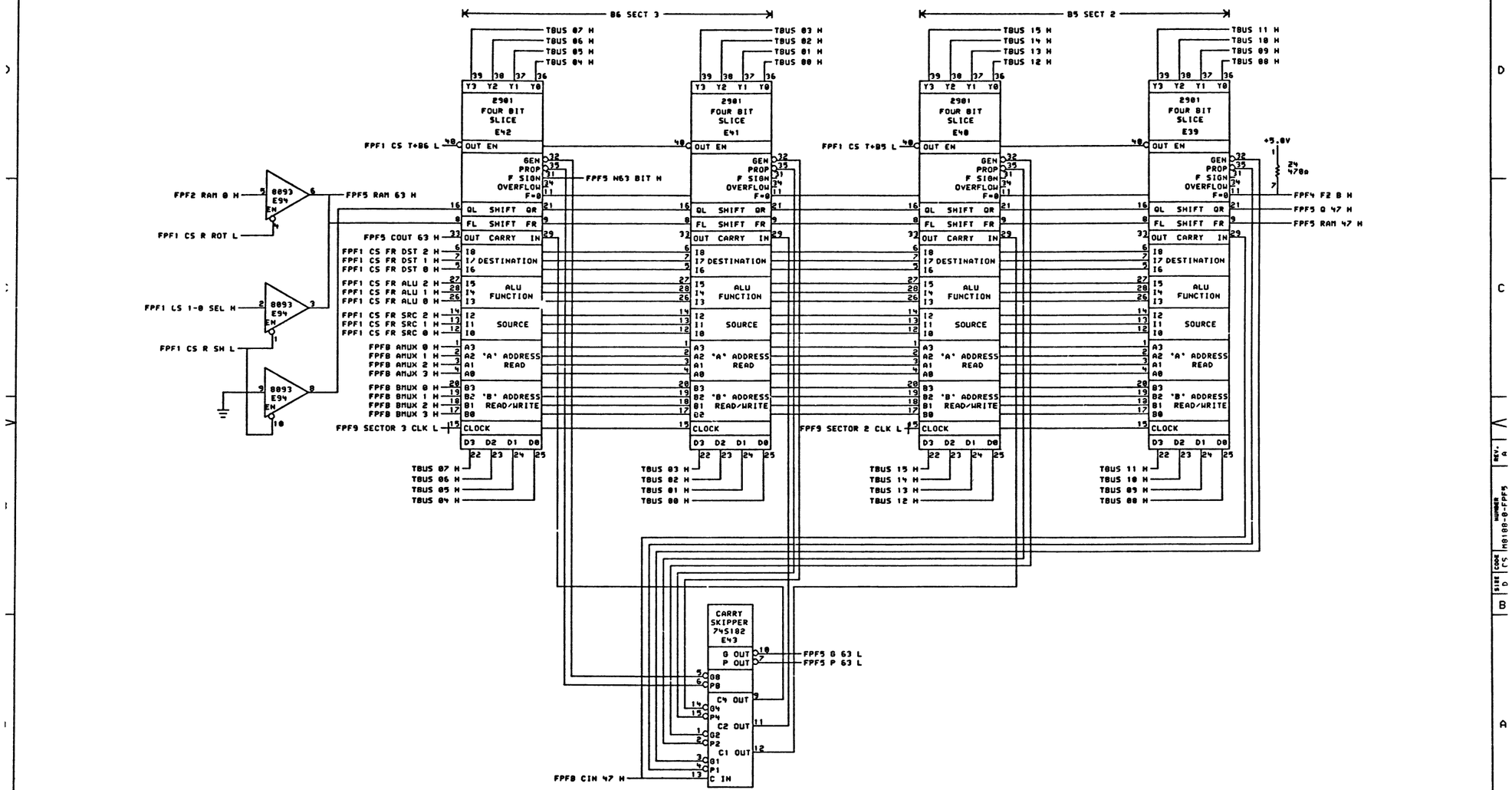
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: K. Looney — DATE: 15-FEB-81
CHK'D: — DATE:
ENG: Chuck Dewar — DATE: 18-FEB-81
BOARD LOCATION:
SHEET 1 OF 1
PS:<TOWER>FPF4B.DRW — 16-FEB-81 13:45
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FPF11

TITLE: BYTES 4 & 3

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF4	A



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: K. Lovely — DATE: 16-FEB-81 — ENG: Chuck Davies — DATE: 19-FEB-81
CHK'D: A.B. — DATE — BOARD LOCATION: — SHEET 1 OF 1
PS:<TOWER>FPF50.DRW — 16-FEB-81 13:46 — NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: FPF11 — B-DD-M8188-0

TITLE: BYTES 6 &5

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF5	A

TBUS	RELEVANT BUT
T0	Y8
T1	Y9
T5	Y61
T6	Y62

MPC LOGIC

FPF1 CS MA 8 H
FPF1 CS MA 7 H
FPF6 MAB 7 L
FPF1 CS MA 6 H
FPF6 MAB 6 L
FPF1 CS MA 5 H
FPF6 MAB 5 L
FPF1 CS MA 4 H
FPF6 MAB 4 L
FPF1 CS MA 3 H
FPF1 CS MA 2 H
FPF1 CS MA 1 H
FPF1 CS MA 0 H
FPF9 JAM MPC ZERO H
+5.0V
23 470Ω
24 470Ω
74S05 E48
74S05 E55
74S02 E36
74S02 E35
74S02 E58
FPF6 MPC 8 H
FPF6 MPC 7 H
FPF6 MPC 6 H
FPF6 MPC 5 H
FPF6 MPC 4 H
FPF6 MPC 3 H
FPF6 MPC 2 H
FPF6 MPC 1 H
FPF6 MPC 0 H

FPF1 CS MAINT/KERNEL H
FPFA STAT 3 H
FPF2 E2 BIT H
FPF1 CS BUT E2 H
TBUS 05 H
FPF1 CS BUT T5 H
TBUS 06 H
FPF1 CS BUT T6 H
FPF5 N63 BIT H
FPF1 CS BUT N63 H
FPF1 CS BUT CNTR0 H
TBUS 01 H
FPF1 CS BUT T1 H
FPF8 FAST C OUT H
FPF1 CS BUT FAST C OUT H
FPF8 QN 8-40 H
FPF1 CS BUT QN 8-40 H
TBUS 00 H
FPF1 CS BUT T0 H
FPF7 LDPC ON IFETCH H
FPF1 CS BUT LDPC H
FPFA FD (1) H
FPF1 CS BUT FD H
FPF2 EN BIT H
FPF1 CS BUT EN H
FPF8 2 BIT H
FPF1 CS BUT 2 H
FPF7 CLR FPS H
FPF1 CS BUT CLR FPS H
74S03 E58
74S03 E50
74S03 E47
74S03 E56
74S03 E61
FPF6 NAB 3 L
FPF6 NAB 2 L
FPF6 NAB 1 L
FPF6 NAB 0 L

FPFA CNTR BORROW L
74S05 E55

IR DECODE PLA
BRANCH PLA
ARRAY PROGRM 825101 E53
ARRAY PROGRM 825101 E52
0F 1F 2F 3F 4F 5F 6F 7F
FPF6 NAB 0 L
FPF6 NAB 1 L
FPF6 NAB 2 L
FPF6 NAB 3 L
FPF6 NAB 4 L
FPF6 NAB 5 L
FPF6 NAB 6 L
FPF6 NAB 7 L
FPF1 CS BR0 H
FPF1 CS BR1 H
FPF1 CS BR2 H
FPFA FPS FMM H
FPFA FPIR 00 H
FPFA FPIR 01 H
FPFA FPIR 02 H
FPFA FPIR 03 H
FPFA FPIR 04 H
FPFA FPIR 05 H
FPFA FPIR 06 H
FPFA FPIR 07 H
FPFA FPIR 08 H
FPFA FPIR 09 H
FPFA FPIR 10 H
FPFA FPIR 11 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
FPF1 CS BR3 H
FPFA FL (1) H
FPFA FPS FID H
FPFA FPS IUV H
FPFA FPS IU H
FPFA FPS IV H
FPFA FPS IC H
FPFA FPS FT H
FPFA GR 7 L
FPFA STAT 2 H
FPFA STAT 1 H
FPFA STAT 0 H
FPFA FD (1) H
EN FUSE CHIP
FPF1 CS BR 1 ENA L
FPF1 CS BR 2 ENA L
R11 180Ω

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REVISIONS
CHK | CHANGE NO. | REV

digital
DRN D. Toomey DATE 16-FEB-81
CHK'D Jack Hall DATE 16-FEB-81
ENG Mike Davis DATE 16-FEB-81
BOARD LOCATION:
SHEET 1 OF 1
PS1(TOWER)FPF60.DRW 16-FEB-81 13:48
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FP11

TITLE: NADRS SEQUENCER
SIZE D | CODE CS | NUMBER M8188-0-FPF6 | REV. A

MIB ENCODER L

512 X 8 ROM 82S115 E28

512 X 8 ROM 82S115 E10

MIB ENCODER H

R3 180Ω

FPF1 CS INST HOLD H

FPF9 T FON2 CLK H

74S02 E50

FPF7 HOLD L

FPF6 MPC 0 H
FPF6 MPC 1 H
FPF6 MPC 2 H
FPF6 MPC 3 H
FPF6 MPC 4 H
FPF6 MPC 5 H
FPF6 MPC 6 H
FPF6 MPC 7 H
FPF6 MPC 8 H
P.U.

ADR

EN

LATCH

DUAL QUAD BUFFER 74LS244 E29

DUAL QUAD BUFFER 74LS244 E11

A0 A1 A2 A3 EN

A0T A1T A2T A3T

B0 B1 B2 B3 EN

B0T B1T B2T B3T

MIB 00 H
MIB 01 H
MIB 02 H
MIB 03 H
MIB 04 H
MIB 05 H
MIB 06 H
MIB 07 H
MIB 08 H
MIB 09 H
MIB 10 H
MIB 11 H
MIB 12 H
MIB 13 H
MIB 14 H
MIB 15 H

FPF9 MIB T/S ENA L

MIB RCVR

ANALOG SWITCH SD5000 E26
ANALOG SWITCH SD5000 E17
ANALOG SWITCH SD5000 E10
ANALOG SWITCH SD5000 E8

SOURCE

FPF7 RMIB 00 L
FPF7 RMIB 01 L
FPF7 RMIB 02 L
FPF7 RMIB 03 L
FPF7 RMIB 04 L
FPF7 RMIB 05 L
FPF7 RMIB 06 L
FPF7 RMIB 07 L
FPF7 RMIB 08 L
FPF7 RMIB 09 L
FPF7 RMIB 10 L
FPF7 RMIB 11 L
FPF7 RMIB 12 L
FPF7 RMIB 13 L
FPF7 RMIB 14 L
FPF7 RMIB 15 L

+12V

Z1 4.7KΩ
Z2 4.7KΩ
R4 4.7KΩ
R5 4.7KΩ
22 4.7KΩ

V2 BUS

E34 NUMBER
E14 NUMBER

6 D FF 74S174 E15
6 D FF 74S174 E27
6 D FF 74S174 E9

R0 R1 R2 R3 R4 R5
D0 D1 D2 D3 D4 D5

P.U.
FPF9 T FON2 CLK H

SET CLK

MIB DECODER

ARRAY PROGRM 82S100 E16

0F FPF7 LDPC ON IFETCH H
1F FPF7 CLR FPS H
2F FPF7 JENTRY FPP H
3F
4F
5F
6F
7F

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

EN FUSE CHIP

R7 180Ω

C5 15μF 20V

+5.0V

R6 33Ω

D1 7498 4.3V 1/4W

*NOTE: PIN "A" ON J1 IS CUT OUT TO KEY THE CONNECTOR.

J1

NC	A	B	NC
MIB 15 H	C	D	CHIP CLK H
MIB 14 H	E	F	DAL 00 H
MIB 13 H	H	J	DAL 01 H
MIB 12 H	K	L	DAL 02 H
MIB 11 H	M	N	DAL 03 H
MIB 10 H	P	R	DAL 04 H
MIB 09 H	S	T	DAL 05 H
MIB 08 H	U	V	DAL 06 H
MIB 07 H	W	X	DAL 07 H
MIB 06 H	Y	Z	DAL 08 H
MIB 05 H	AA	BB	DAL 09 H
MIB 04 H	CC	DD	DAL 10 H
MIB 03 H	EE	FF	DAL 11 H
MIB 02 H	HH	JJ	DAL 12 H
MIB 01 H	KK	LL	DAL 13 H
MIB 00 H	MM	NN	DAL 14 H
RESET H	PP	RR	DAL 15 H
CSEL L	SS	TT	T FON2 CLK L
+12V	UU	VV	FON2 GND

Q BUS JUMPERS

AM2	IAK 1	W1	AM2
AR2	DMG 1	W2	AS2
CM2	IAK 2	W4	CM2
CR2	DMG 2	W5	CS2

U BUS JUMPERS

CA1	NPG H	W3	CB1
DK2	B07 H	W8	DL2
DP2	B05 H	W12	DR2
DS2	B04 H	W11	DT2
DM2	B06 H	W7	DM2

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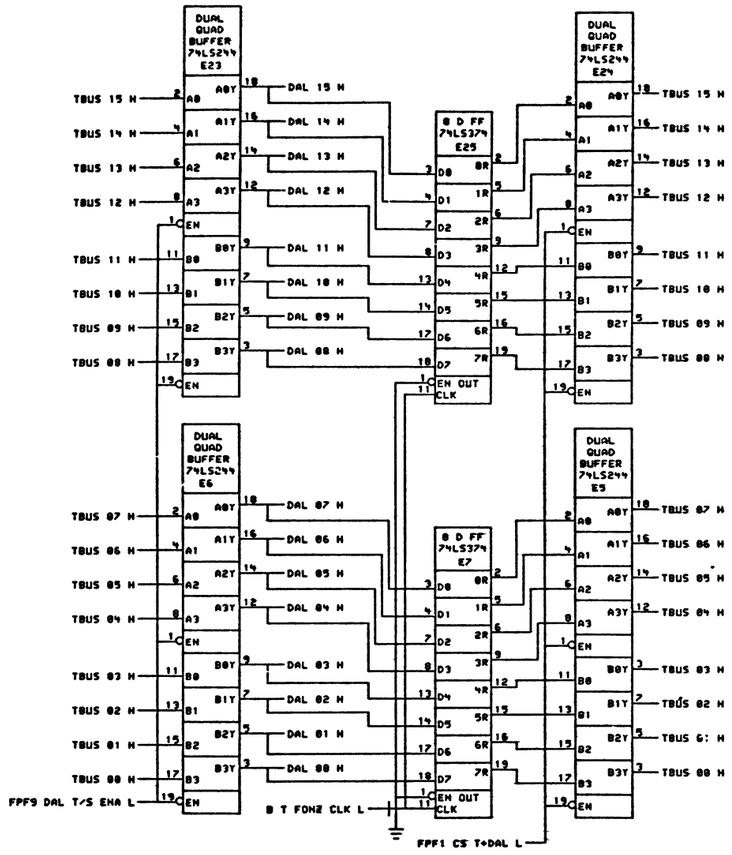
REVISIONS

CHK	CHANGE NO.	REV
JJ	78 ECO M8028	C
	FOR RELEASED PRINT	
	A FILE	

DRN		DATE	ENG. T. BOWEN
CHK'D	D_DE_OR:O	DATE	BOARD LOCATION:
PS:<BOWEN>FPF78.DR4	26-AUG-81 08:40		NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:	FP11		8-DD-M8188-0

TITLE: MIB INTERFACE

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF7	C



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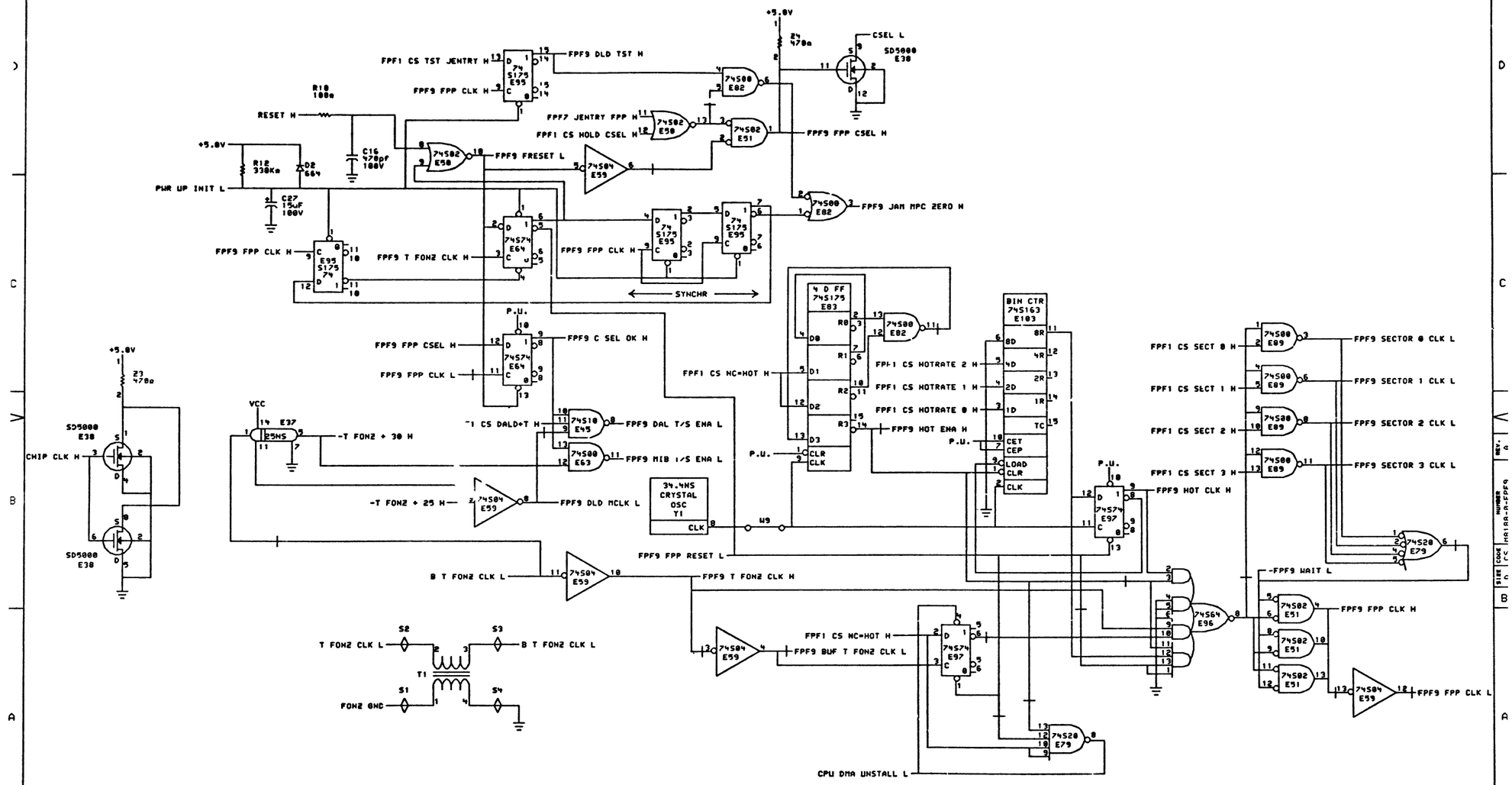
REVISIONS		
CHK	CHANGE NO.	REV

PS4(TOWER)FPF88.DRW 16-FEB-81 13:52
FIRST USED ON OPTION/MODEL: FPF11

DRN [illegible] DATE 16-FEB-81
CHK [illegible] DATE
ENG [illegible] DATE 18-FEB-81
BOARD LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY: B-DD-M8188-0

TITLE: DAL INTERFACE

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF8	A



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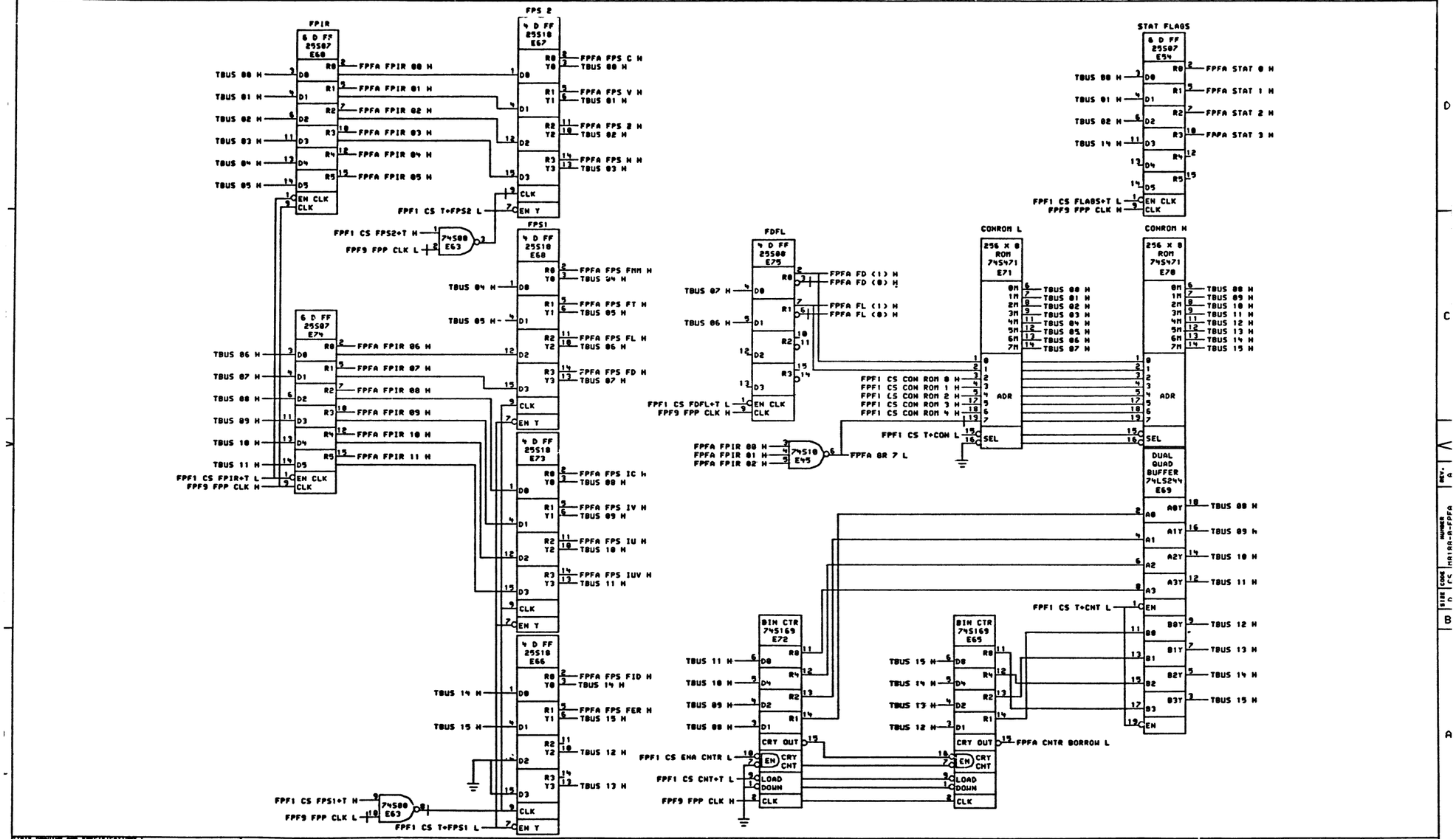
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: [illegible] DATE: 16-FEB-81 ENG: Chuck Dawes DATE: 18-FEB-81
CHK: [illegible] DATE: BOARD LOCATION:
SHEET 1 OF 1
PS:<TOWER>FPF98.DRW 16-FEB-81 13:54 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: FPF11 B-DD-M8188-0

TITLE: RESTE,CSEL,MIB & DAL ENA LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPF9	A



REVISIONS		
CHK	CHANGE NO.	REV

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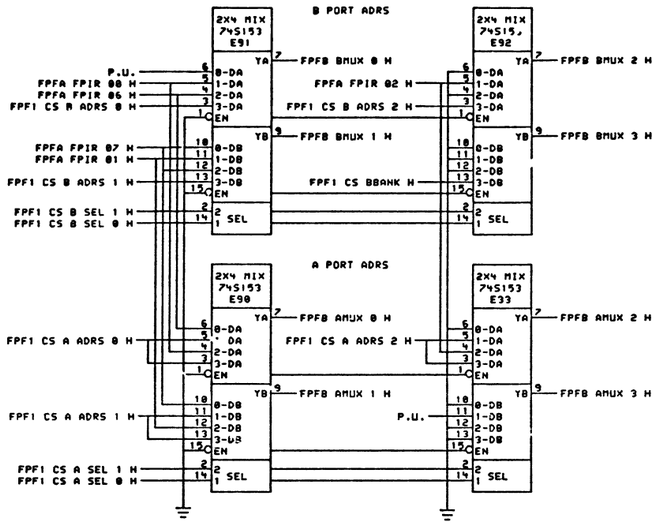
digital

DRN: J. Landry
CHK: D. Gill
DATE: 16-FEB-81
ENG: Luis Davis
DATE: 19-FEB-81
DATE
BOARD LOCATION:
SHEET 1 OF 1

P5:<TOWER>FPFA0.DRW 16-FEB-81 13:57
FIRST USED ON OPTION/MODEL: FPF11
NEXT HIGHER ASSEMBLY: B-DD-M8188-0

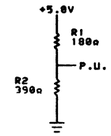
TITLE: T-BUS RESOURCES

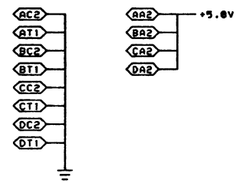
SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPFA	A



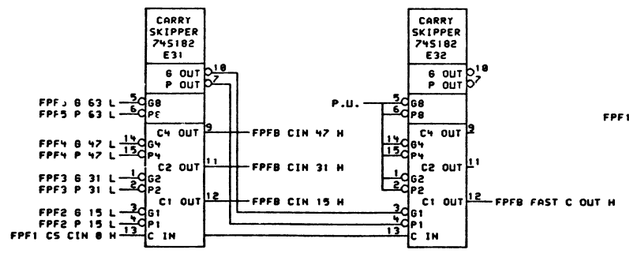
B PORT
CHANNEL
0 X3.OR.X1 = AC.OR.1
1 X7:X0 =FSRC
2 X3:X0 =AC
3 X17:X10 = B ROM * BBANK

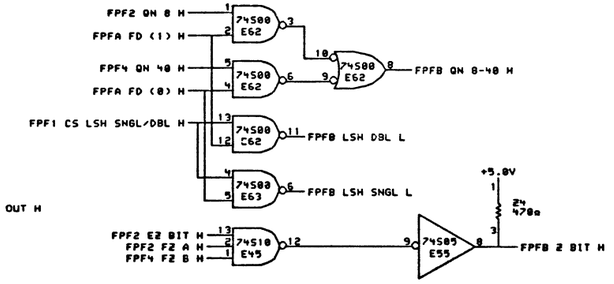
A PORT
CHANNEL
0 X3:X0 =AC (FPIR (7:6))
1 X17:X10 =A ROM
2 X7:X0 =F SRC / FDST (FPIR (2:0))
3 LO ADRS





CARRY LOGIC





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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRW K.Toomey 16-FEB-81
CHK D.Kelly 16-FEB-81
ENG Alex Davies 18-FEB-81
PS:<TOWER>FPFB8.DRW 16-FEB-81 15:13
FIRST USED ON OPTION/MODEL: FPF11
NEXT HIGHER ASSEMBLY: B-DD-M8188-0

TITLE: MISC. SLICE LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FPFB	A

SIZE	CODE	NUMBER	REV.
D	CS	M8188-0-FFFC	A

+5.0V\VX GND TTL\8818\ +5.0V\VX GND TTL\8818\

C1 15uF 15V
C2 15uF 15V
C3 15uF 15V
C4 15uF 15V
C6 .047uF 50V
C7 .047uF 50V
C8 .047uF 50V
C9 .047uF 50V
C10 .047uF 50V
C11 .047uF 50V
C12 .047uF 50V
C13 .047uF 50V
C14 .047uF 50V
C15 .047uF 50V
C26 .047uF 50V

C17 .047uF 50V
C18 .047uF 50V
C19 .047uF 50V
C20 .047uF 50V
C21 .047uF 50V
C22 .047uF 50V
C23 .047uF 50V
C24 .047uF 50V
C25 .047uF 50V

W10
SPARE

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REVISIONS

CHK	CHANGE NO.	REV
	1	1

digital

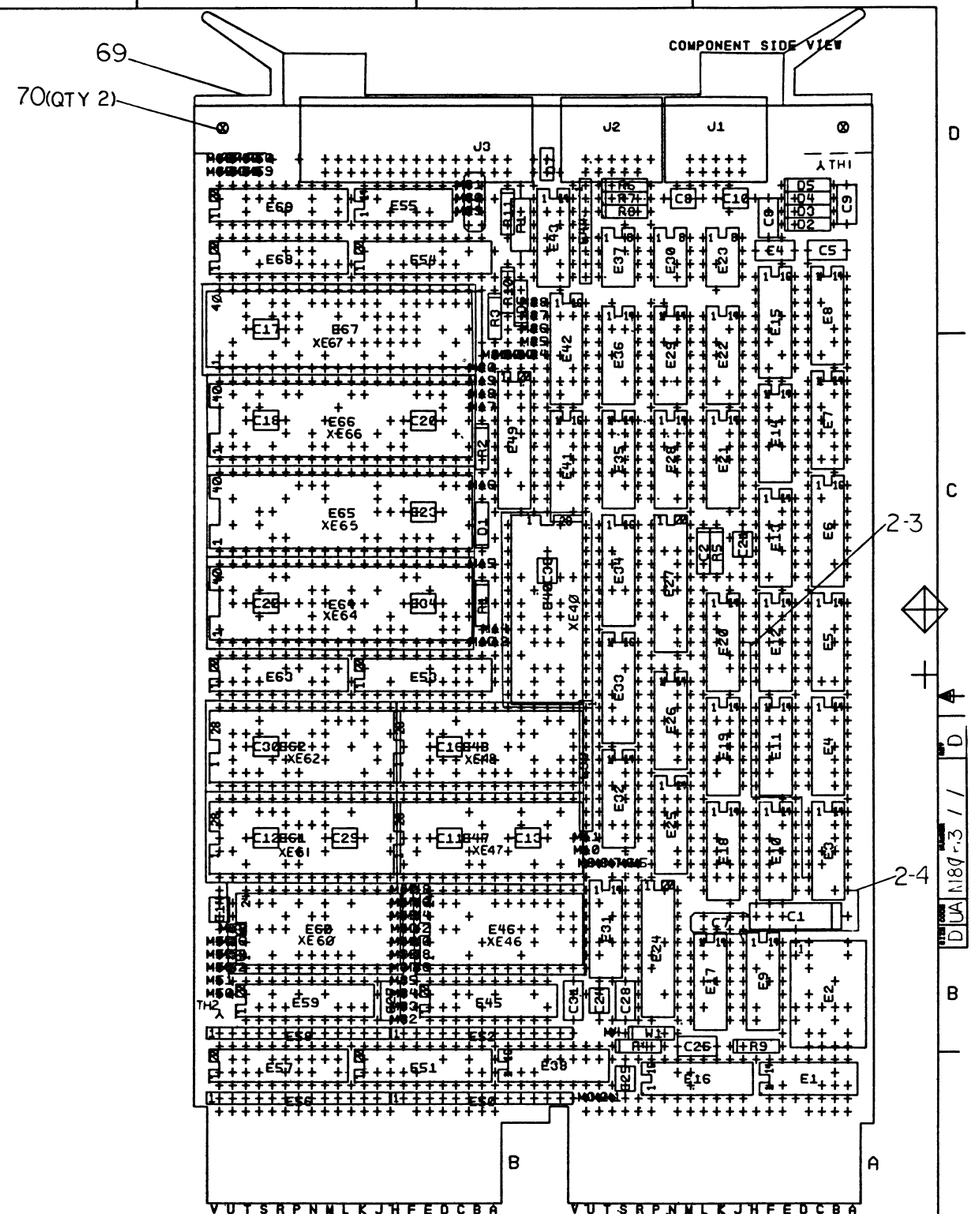
DRN: S. Looney DATE: 16-FEB-81
CHK'D: [illegible] DATE:
ENG: Chuck Dawes DATE: 16-Feb-81
BOARD LOCATION:
SHEET 1 OF 1
PS:<TOWER>FPFC8.DRW 16-FEB-81 14:57
NEXT HIGHER ASSEMBLY: B-DD-M8188-0
FIRST USED ON OPTION/MODEL: FPF11

TITLE: CAP DRAW

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JUMPER SHIP CONFIGURATION

CONFIGURATION	WIRE WRAP JUMPERS FROM	TO
START ADDRESS 10,000	M26 M25 M27	M25 M24 M28
BREAK DETECTED ON SLU1	M14 M30	M13 M31
60HZ REAL TIME CLOCK	M19	M17
28(24)-PIN SOCKET	M22 M23 M39 M41 M40 M51 M36 M43 M34 M37 M42 M38 M58	M23 M24 M41 M40 M51 M57 M56 M34 M5 M42 M5 M47 M32
PARALLEL I/O	M66 M59 M63	M65 M60 M61
BATTERY BACKUP NOT SELECTED	M1 M1	M2 M4
TIME-OUT (HALT)	M7 M8	M6 M9



NOTES:

STEP E	↑ Y AXIS .0 STEP .0 TIMES
REPEAT	→ X AXIS 5.250 STEP 2 TIMES

CHK	CHANGE NO	REV
	M8063-MR1	B
	M8063-MR2	C
	M8063-MR3	D

ETCH REV. C

SIGNATURES	DATE
DRN.	5/12/81
CHK'D.	6/1/81
MECH.ENG. Barry Meakin	6/1/81
PROJ.ENG. Barry Meakin	6/1/81
PROD.	6/24/81
SCALE 2/1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. 8-DD-M8063-0	

digital

TITLE KXT11-AA

SIZE D | CODE UA | NUMBER M8063-0-0 | REV D

WO# 190494

REWORK INSTRUCTIONS

ECO #2

2-1 AND 2-2 FOR ETCH CUTS REFER
TO D-EC-5014484-0-0

WIRE ADDS, SIDE 1, AS SHOWN
2-3 E20-11 TO E3-6
2-4 E3-8 TO E9-1

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. D. Toomey 16-FEB-82
CHK'D. R.W. CAUNTER 25NOV81
ENG. B. MASKAS 25NOV81
BOARD LOCATION:
SHEET 2 OF 2
DSK:M8063I.T2P[4,27] 16-FEB-82 15:31
NEXT HIGHER ASSEMBLY: B-DD-M8063-0
FIRST USED ON OPTION/MODEL: KXT11-AA

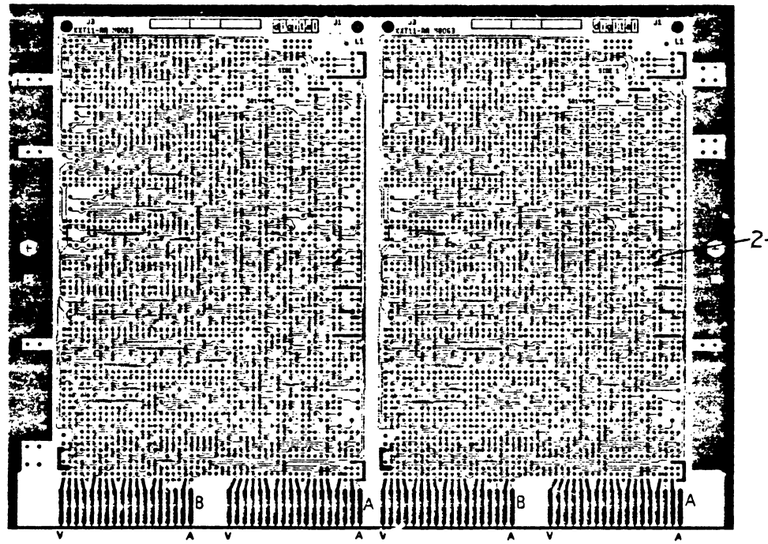
TITLE: KXT11-AA

SIZE	CODE	NUMBER	REV.
D	UA	M8063-0-0	D

SIZE D | CODE UA | NUMBER M8063-0-0 | REV. D

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KXT11-AA SHEET 1 09 APR 81 13 22 22 42311



REVISIONS			
	CHK	CHANGE NO	REV
1	JJ	M8063-MR2	B
2	JJ		
3	JJ		
4	B	MASKAS	

DRN		FIRST USED ON: KXT11-AA
CHK		TITLE: ETCH CUT DRAWING
ENG		
PROJ ENG		
PROD		
NEXT HIGHER ASSY: 0-UA-M8063-0-0		
SCALE: 1/1		
SHEET: 1 OF 3		

digital

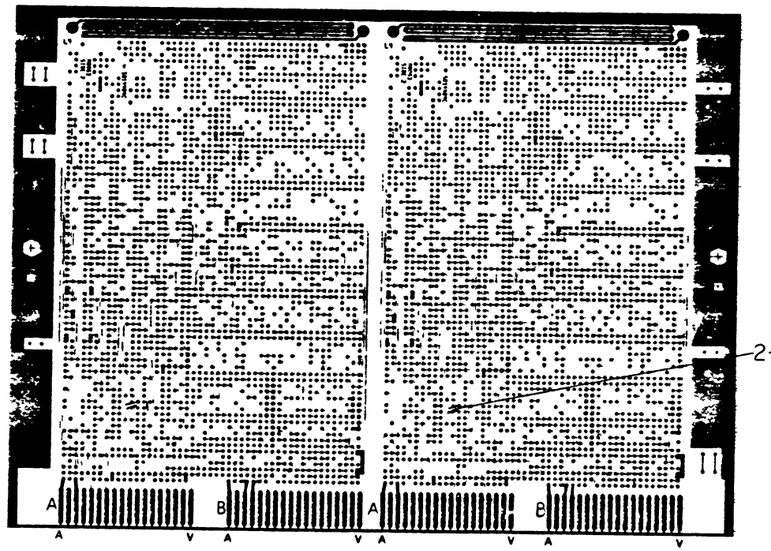
SIZE	CODE	NUMBER	REV
D	EC	5014484-0-0	B

DIST

NEXT ASSY	CODE	NUMBER	REV
	EC	5014484-0-0	B

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KA11-AA SHEET 5 08 APR 81 13 55 55 MSA11



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
ETCH CUT DRAWING	D	EC	5014484-0-0	B
SCALE 1/1 SHEET 2 OF 3	DIST			

DEC 5014484-0-0 B

REWORK INSTRUCTIONS

ECO #2

ETCH CUTS, SIDE 1, AS SHOWN
2-1 CUT AT E12-13

ETCH CUTS, SIDE 2, AS SHOWN
2-2 AT 2ND PTH TO THE RIGHT OF E9-1

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: D. Landry | DATE: 09-NOV-81 | ENG: B. MASKAS | DATE: 9NOV81

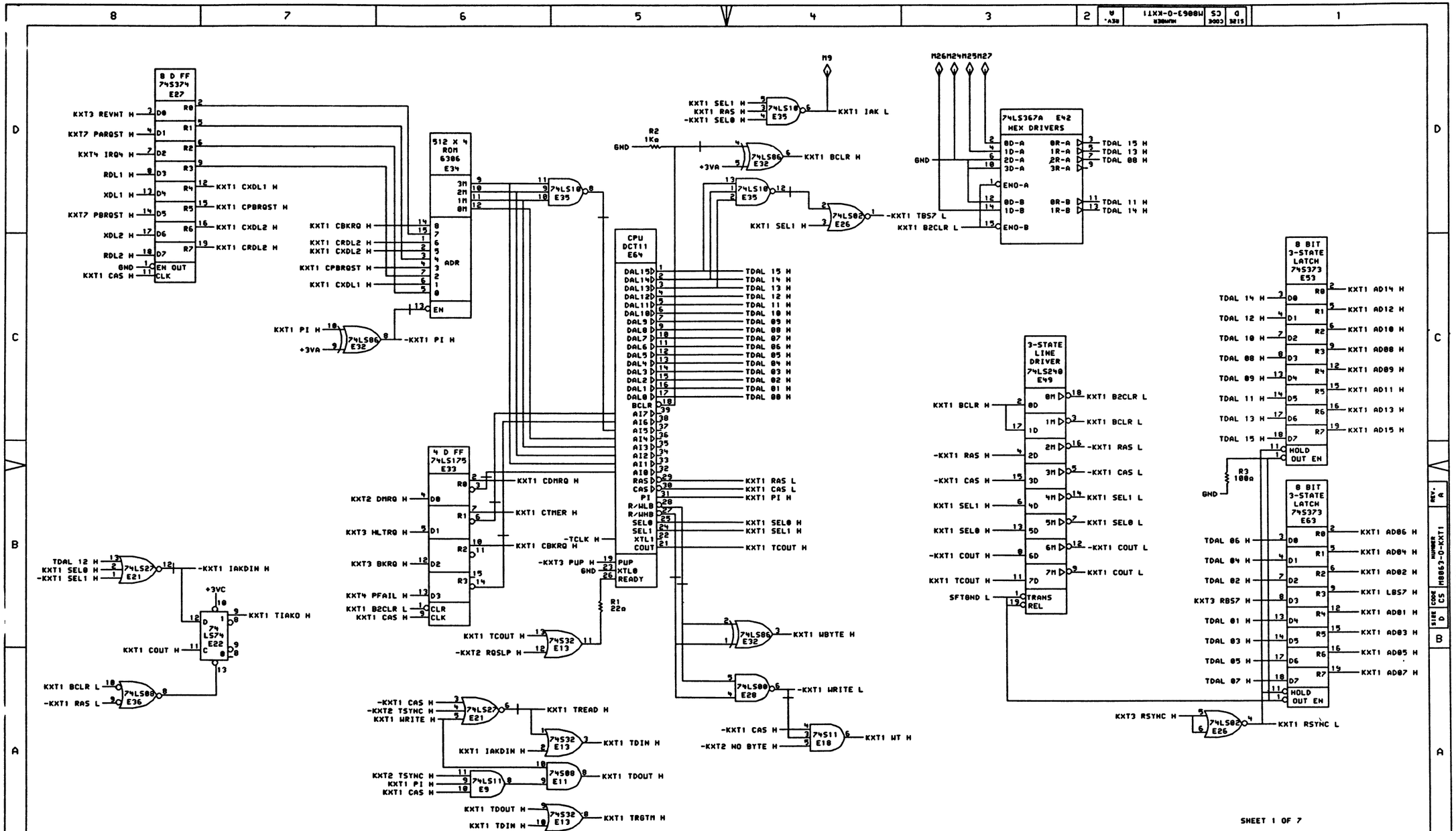
CHK'D: D. CAUNTER | DATE: 9NOV81 | BOARD LOCATION: SHEET 1 OF 1

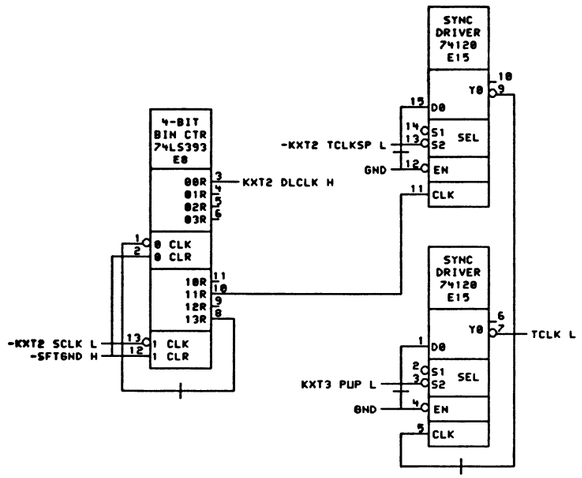
DSK:M8063.TJP[4,27] 09-NOV-81 09:09 | NEXT HIGHER ASSEMBLY: D-UA-M8063-0-0

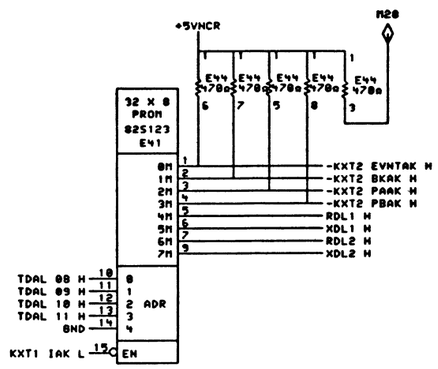
FIRST USED ON OPTION/MODEL: KXT11-AA

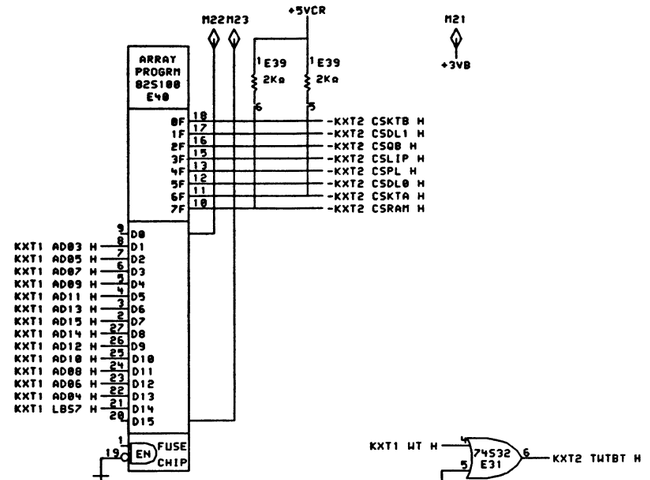
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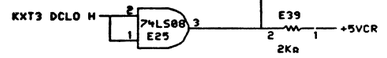
SIZE	CODE	NUMBER	REV.
D	EC	501484-0-0	B

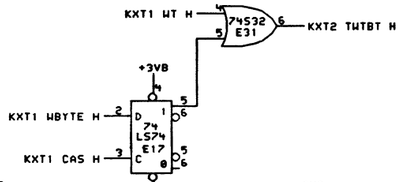

8 D FF 74S374 E27
KXT3 REVNT H
KXT7 PARQST H
KXT4 IRQ4 H
RDL1 H
XDL1 H
KXT7 PBRQST H
XDL2 H
RDL2 H
GND
KXT1 CAS H
EN OUT
CLK
KXT1 CXDL1 H
KXT1 CPBRQST H
KXT1 CXDL2 H
KXT1 CRDL2 H
512 X 4 ROM 6306 E34
KXT1 CBKRQ H
KXT1 CRDL2 H
KXT1 CXDL2 H
KXT1 CPBRQST H
KXT1 CXDL1 H
ADR
EN
KXT1 PI H
+3VA
74LS86 E32
-KXT1 PI H
74LS10 E35
CPU DCT11 E64
DAL15
DAL14
DAL13
DAL12
DAL11
DAL10
DAL9
DAL8
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
BCLR
A17
A16
A15
A14
A13
A12
A11
A10
RAS
CAS
PI
R/WLB
R/WHB
SEL0
SEL1
XTL1
COUT
PUP
XTL0
READY
TDAL 15 H
TDAL 14 H
TDAL 13 H
TDAL 12 H
TDAL 11 H
TDAL 10 H
TDAL 09 H
TDAL 08 H
TDAL 07 H
TDAL 06 H
TDAL 05 H
TDAL 04 H
TDAL 03 H
TDAL 02 H
TDAL 01 H
TDAL 00 H
KXT1 RAS L
KXT1 CAS L
KXT1 PI H
KXT1 SEL0 H
KXT1 SEL1 H
KXT1 TCOUT H
-TCLK H
-KXT3 PUP H
GND
R1 22Ω
R2 1KΩ
M9
KXT1 SEL1 H
KXT1 RAS H
-KXT1 SEL0 H
74LS10 E35
KXT1 IAK L
+3VA
74LS86 E32
KXT1 BCLR H
74LS10 E35
74LS02 E26
-KXT1 TBS7 L
KXT1 SEL1 H
KXT1 B2CLR L
M26M24M25M27
74LS367A E42 HEX DRIVERS
GND
0D-A
1D-A
2D-A
3D-A
ENO-A
0D-B
1D-B
ENO-B
0R-A
1R-A
2R-A
3R-A
0R-B
1R-B
TDAL 15 H
TDAL 13 H
TDAL 08 H
TDAL 11 H
TDAL 14 H
4 D FF 74LS175 E33
KXT2 DMRQ H
KXT3 HLTRQ H
KXT3 BKRQ H
KXT4 PFAIL H
KXT1 B2CLR L
KXT1 CAS H
KXT1 CDMRQ H
KXT1 CTMER H
KXT1 CBKRQ H
74S32 E13
KXT1 TCOUT H
-KXT2 RQSLP H
R1 22Ω
74LS86 E32
KXT1 WBYTE H
74LS00 E28
-KXT1 WRITE L
74S11 E18
-KXT1 CAS H
-KXT2 NO BYTE H
KXT1 WT H
TDAL 12 H
KXT1 SEL0 H
-KXT1 SEL1 H
74LS27 E21
-KXT1 IAKDIN H
+3VC
74 LS74 E22
KXT1 TIAKO H
KXT1 COUT H
KXT1 BCLR L
-KXT1 RAS L
74LS08 E36
-KXT1 CAS H
-KXKT2 TSYNC H
KXT1 WRITE H
74LS27 E21
KXT1 TREAD H
KXT1 IAKDIN H
74S32 E13
KXT1 TDIN H
KXT2 TSYNC H
KXT1 PI H
KXT1 CAS H
74LS11 E9
74S08 E11
KXT1 TDOUT H
KXT1 TDOUT H
KXT1 TDIN H
74S32 E13
KXT1 TRGTM H
3-STATE LINE DRIVER 74LS240 E49
KXT1 BCLR H
-KXT1 RAS H
-KXT1 CAS H
KXT1 SEL1 H
KXT1 SEL0 H
-KXT1 COUT H
KXT1 TCOUT H
SFT0ND L
TRANS REL
0D
1D
2D
3D
4D
5D
6D
7D
0M
1M
2M
3M
4M
5M
6M
7M
KXT1 B2CLR L
KXT1 BCLR L
-KXT1 RAS L
-KXT1 CAS L
KXT1 SEL1 L
KXT1 SEL0 L
-KXT1 COUT L
KXT1 COUT L
8 BIT 3-STATE LATCH 74S373 E53
TDAL 14 H
TDAL 12 H
TDAL 10 H
TDAL 08 H
TDAL 09 H
TDAL 11 H
TDAL 13 H
TDAL 15 H
HOLD
OUT EN
KXT1 AD14 H
KXT1 AD12 H
KXT1 AD10 H
KXT1 AD08 H
KXT1 AD09 H
KXT1 AD11 H
KXT1 AD13 H
KXT1 AD15 H
R3 100Ω
GND
8 BIT 3-STATE LATCH 74S373 E63
TDAL 06 H
TDAL 04 H
TDAL 02 H
KXT3 RBS7 H
TDAL 01 H
TDAL 03 H
TDAL 05 H
TDAL 07 H
KXT1 AD06 H
KXT1 AD04 H
KXT1 AD02 H
KXT1 LBS7 H
KXT1 AD01 H
KXT1 AD03 H
KXT1 AD05 H
KXT1 AD07 H
KXT3 RSYNC H
74LS02 E26
KXT1 RSYNC L
SHEET 1 OF 7
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REVISIONS
CHK
CHANGE NO.
REV
digital
DRN L.Connolly
CHK'D K.Cameron
DATE 01-OCT-81
ENG. B.Meaker
DATE 01-OCT-81
DATE 01-OCT-81
BOARD LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
P$:<BOWEN.SCRATCH>KXT1.DRW;81-OCT-81 07:24
TITLE: KXT11-AA CPU
SIZE D
CODE CS
NUMBER M8063-0-KXT1
REV. A
METRIC DCT/ANSI SCRATCH/KXT1 DPI 1. SCALE 2. 'D' RELEASE ADX

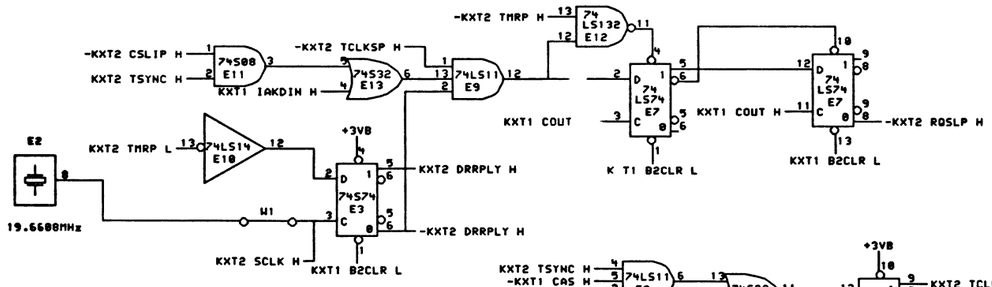


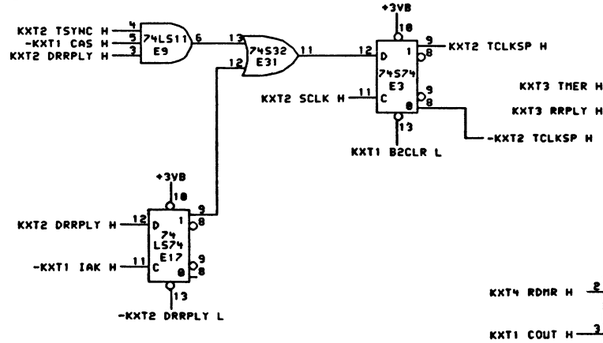


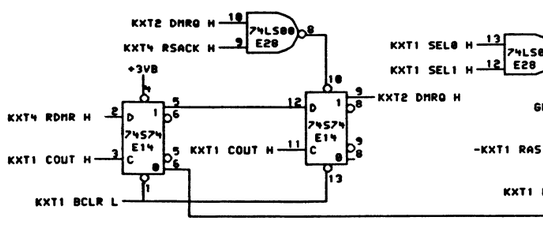


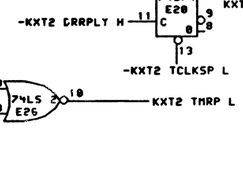


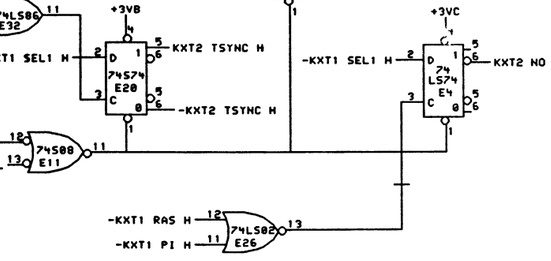


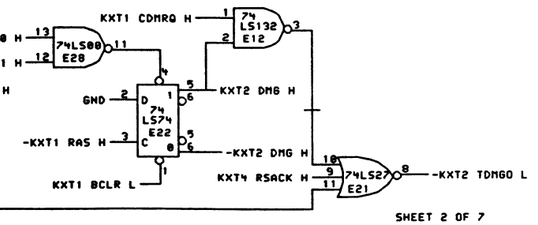












NOTE: OSCILLATOR PACKAGE IS METAL

SHEET 2 OF 7

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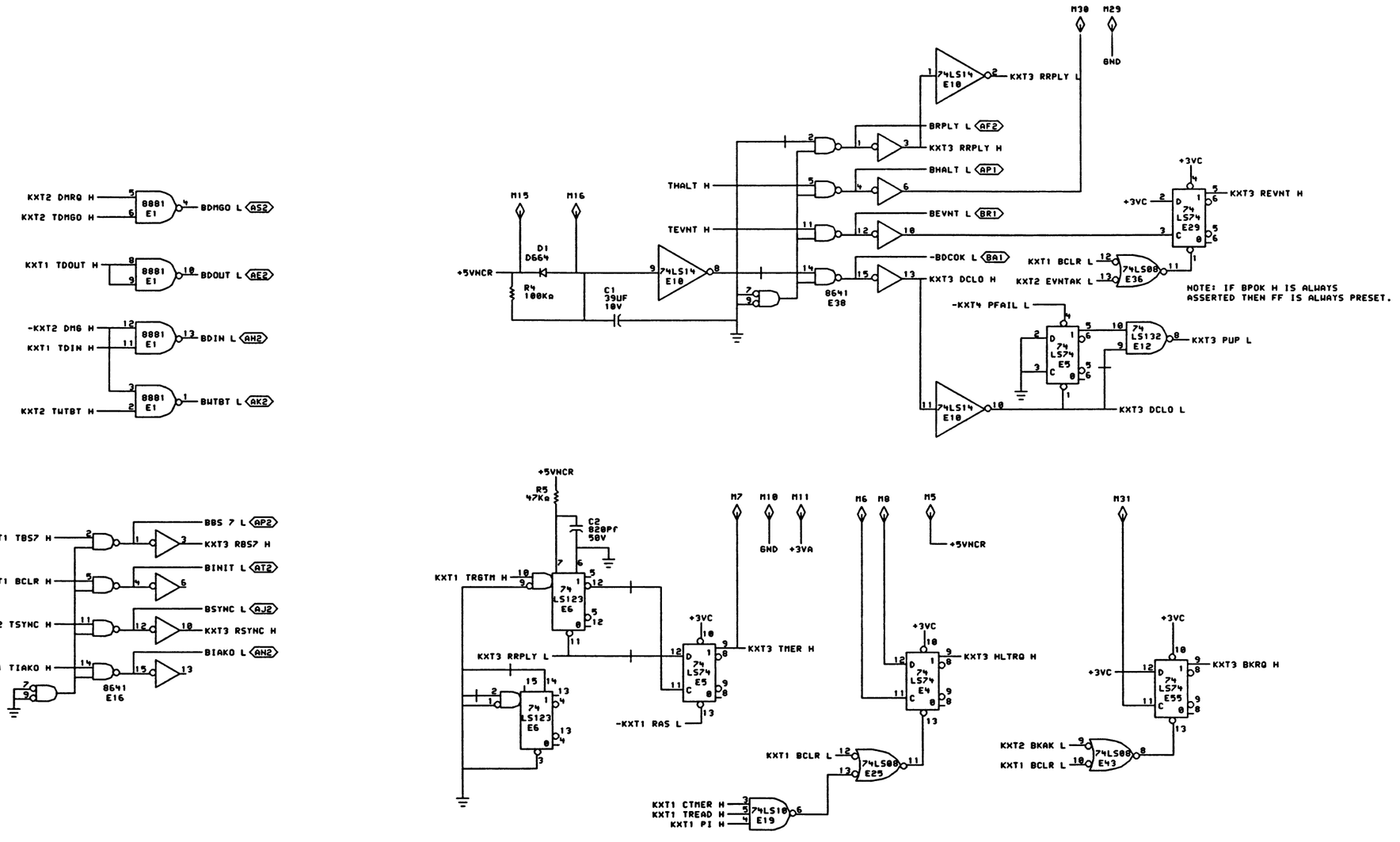
REVISIONS		
CHK	CHANGE NO.	REV
MOVED TR2		B
B. MASKAS		

digital

DRN: R.W.CAUNTER	DATE 04-DEC-81	ENG. B.MASKAS	DATE 04-DEC-81
CHK'D: R.W.CAUNTER	DATE 04-DEC-81	BOARD LOCATION: SHEET 1 OF 1	
SWDCOM:<DOMEN.SCRATCH>KXT2.RVB 02-DEC-81 16:04		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL: KXT11			

TITLE: KXT11-AA CLOCK CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT2	B



SHEET 3 OF 7

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: D. Conroy
CHK: P. Cuccia
DATE 01-OCT-81 / 01-OCT-81
ENG: B. Thacker
DATE 01-OCT-81
BOARD LOCATION:
SHEET 1 OF 1
PS:<BOWEN.SCRATCH>KXT3.DRW 01-OCT-81 07:26
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:

TITLE: KXT11-AA BUS CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT3	A

VERSATEC SUDSVP V5.0 01-OCT-81 10:31:42 KXT3.PLO METZGER

METZGER, P:<CDBOWEN.SCRATCH>KXT3.DPI .1, SCALE 1, D' PLTFMT BOX

+5VNCR
R9 3.48KΩ
C7 120PF 100V
REG SEL DC004 E24
RXCX 18
BRDLY 8 BRPLY L (AF2)
INWD 11 KXT4 READ L
OUTHB 13 KXT4 WHB L
OUTLB 12 KXT4 WLB L
SEL 8 14, 4 15, 2 16, 6 17 KXT4 SEL6 L
KXT1 RSYNC L 6 SYNC
(AK2) BWTBT L 5 WTBT
(AH2) BDIN L 7 DATA IN
(AE2) BDOUT L 9 DATA OUT
(AU2) BDAL 00 L 4 D0
(AV2) BDAL 01 L 3 D1
(BE2) BDAL 02 L 2 D2
GND 1 VEC
-KXT2 CSQB H 19 EN

RESISTOR NETWORK 1318110-00 E58
+3VA 2
(AP2) -BBS 7 H 3
(BV2) -BDAL 15 H 4
(AJ2) -BSYNC H 5
(AH2) -BDIN H 6
(AF2) -BRPLY H 7
(BK2) -BDAL 06 H 8
(BR1) -BEVNT H 9
(BN1) -BSACK H 10
(AU2) -BDAL 00 H 11
(AK2) -BWTBT H 12
+5.0V 13
330Ω 2
680Ω 1

RESISTOR NETWORK 1318110-00 E56
(BU2) -BDAL 14 H 2
+3VB 3
(BP1) BSPARE 6 H 4
(BP2) -BDAL 10 H 5
(BL2) -BDAL 07 H 6
(BR2) -BDAL 11 H 7
(BT2) -BDAL 13 H 8
(BS2) -BDAL 12 H 9
(BJ2) -BDAL 05 H 10
(BM2) -BDAL 08 H 11
(BN2) -BDAL 09 H 12
+5.0V 13
330Ω 2
680Ω 1

RESISTOR NETWORK 1318110-00 E52
(BE1) SSPARE 6 H 2
(AT2) -BINIT H 3
(AP1) -BHALT H 4
(AN1) -BDMR H 5
(BM2) -BDAL 04 H 6
(AR1) -BREF H 7
(AS2) -BDMGO H 8
(AM2) -BIAKO H 9
(AL2) -BIRQ 4 H 10
(AV2) -BDAL 01 H 11
(AA1) BSPARE 1 H 12
+5.0V 13
330Ω 2
680Ω 1

RESISTOR NETWORK 1318110-00 E50
(BF1) SSPARE 7 H 2
(BF2) -BDAL 03 H 3
(BE2) -BDAL 02 H 4
(AB1) BSPARE 2 H 5
(BB1) BPOK H 6
(AE2) -BDOUT H 7
(BC1) SSPARE 4 H 8
(BD1) SSPARE 5 H 9
(AC1) -BDAL 16 H 10
(BA1) BDCOK H 11
(AD1) -BDAL 17 H 12
+5.0V 13
330Ω 2
680Ω 1

4 BIT TRANS CEIVER DC005 E45
+5VCR 1 E39 2KΩ 4
IN/OUT D3 6 TDAL 03 H
D2 7 TDAL 02 H
D1 17 TDAL 01 H
D0 18 TDAL 00 H
MATCH H 3 KXT4 IRQ4 H
(BF2) -BDAL 03 H 8 BU3
(BE2) -BDAL 02 H 9 BU2
(AV2) -BDAL 01 H 11 BU1
(AU2) -BDAL 00 H 12 BU0
(AL2) BIRQ 4 L 13 MENB
+5VNCR 19 JA3
2 JA2
1 JA1
16 JV3
15 JV2
14 JV1
KXT4 RLB H 5 XMIT
4 REC

4 BIT TRANS CEIVER DC005 E59
+5VCR 1 E39 2KΩ 3
IN/OUT D3 6 TDAL 11 H
D2 7 TDAL 10 H
D1 17 TDAL 09 H
D0 18 TDAL 08 H
MATCH H 3 KXT4 RSACK H
(BR2) -BDAL 11 H 8 BU3
(BP2) -BDAL 10 H 9 BU2
(BM2) -BDAL 09 H 11 BU1
(BM2) -BDAL 08 H 12 BU0
(BN1) BSACK L 13 MENB
+5VNCR 19 JA3
2 JA2
1 JA1
16 JV3
15 JV2
14 JV1
KXT4 XHB H 5 XMIT
KXT4 RHLB H 4 REC

4 BIT TRANS CEIVER DC005 E51
+5VCR 1 E39 2KΩ 18
IN/OUT D3 6 TDAL 07 H
D2 7 TDAL 06 H
D1 17 TDAL 05 H
D0 18 TDAL 04 H
MATCH H 3 KXT4 RDMR H
(BL2) -BDAL 07 H 8 BU3
(BK2) -BDAL 06 H 9 BU2
(BJ2) -BDAL 05 H 11 BU1
(BM2) -BDAL 04 H 12 BU0
(AM1) BDMR L 13 MENB
+5VNCR 19 JA3
2 JA2
1 JA1
16 JV3
15 JV2
14 JV1
XMIT 5
REC 4

4 BIT TRANS CEIVER DC005 E57
+5VCR 1 E39 2KΩ 7
IN/OUT D3 6 TDAL 15 H
D2 7 TDAL 14 H
D1 17 TDAL 13 H
D0 18 TDAL 12 H
MATCH H 3 KXT4 PFAIL H
(BV2) -BDAL 15 H 8 BU3
(BU2) -BDAL 14 H 9 BU2
(BT2) -BDAL 13 H 11 BU1
(BS2) -BDAL 12 H 12 BU0
(BB1) -BPOK L 13 MENB
+5VNCR 19 JA3
2 JA2
1 JA1
16 JV3
15 JV2
14 JV1
XMIT 5
REC 4

KXT2 CSQB L 5 74LS14 E10 6 KXT4 CSQB H
KXT2 DMG H 10 74LS10 E19 8
KXT3 RSYNC H 11
9
4 74LS08 E36 5
5
13 2 74S11 E10 12 KXT4 XHB H
-KXT1 IAK H 1
-KXT1 BCLR H
KXT1 TIAKO H 9 74S32 E31 8 KXT4 RLB H
KXT4 RHLB H 10
KXT4 CSQB H 11 74S11 E10 8
KXT1 TREAD H 10
KXT2 DRRPLY H 9
11 74S32 E31 3 KXT4 RHLB H
2
KXT3 RSYNC H 2
-KXT2 CSQB H 1 74LS10 E19 12 4
13 74S08 E11 6
KXT2 DMG H 5
KXT4 READ L 3 74LS14 E10 4 KXT4 READ H

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REVISIONS		
CHK	CHANGE NO.	REV
D. Mallard	M8063-MR001	B
M. HASKAS		

digital
DRW T. Bowen 09-SEP-81
CHK D. Mallard 09-SEP-81
ENG T. BOWEN 09-SEP-81
PS:<BOWEN>KXT4.DRW 09-SEP-81 11:07
BOARD LOCATION:
SHEET OF
FIRST USED ON OPTION/MODEL:
NEXT HIGHER ASSEMBLY:

TITLE: KXT11-AA BUS I/O

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT4	B

NOTE:
M4 IS WRAPPED TO M1 AND M2 NORMALLY.
IF BATTERY BACKUP IS DESIRED FOR E47
AND E61 THEN WRAP M4 TO M2 AND M3.

M44 M48 M4 M34 M57 M43 M41 M36 M58 M56 — KXT2 CSKTA L

E61 / E47 — 28 PIN SOCK

+5VNCR
KXT1 AD08 H
KXT1 AD07 H
KXT1 AD06 H
KXT1 AD05 H
KXT1 AD04 H
KXT1 AD03 H
KXT1 AD02 H
KXT1 AD01 H
TDAL 00 H
TDAL 01 H
TDAL 02 H
GND

KXT1 AD09 H
KXT1 AD10 H
TDAL 15 H
TDAL 14 H
TDAL 13 H
TDAL 12 H
TDAL 11 H
TDAL 07 H
TDAL 06 H
TDAL 05 H
TDAL 04 H
TDAL 03 H

M32 — KXT1 AD11 H

M47 M45 M35 M37 M42 M39 M40 M38 — KXT2 CSKTB L

E62 / E48 — 28 PIN SOCK

+5VCR — E39 2Kα — E44 470α

M50 — GND
M46 — KXT1 AD13 H
M49 — KXT1 AD12 H
M33 — +5VNCR
M51
M53 M55

+5VCR — E39 2Kα — +3VC

2K X 8 STATIC RAM 2016P E60

M0 M1 M2 M3 M4 M5 M6 M7 — TDAL 08 H … TDAL 15 H

KXT1 AD01 H … KXT1 AD11 H — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

WREN
ENO
(C SEL)

-KXT4 READ H
-KXT4 WHB H
74LS08 E25
KXT2 CSRAM L

M54 M52

2K X 8 STATIC RAM 2016P E46

M0 M1 M2 M3 M4 M5 M6 M7 — TDAL 00 H … TDAL 07 H

KXT1 AD01 H … KXT1 AD11 H — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

WREN
ENO
(C SEL)

-KXT4 READ H
-KXT4 WLB H
74LS08 E25
KXT2 CSRAM L

M3 M1

AV1 +5VBB
+5.0V
AA2 BA2 BV1
+5VNCR
GND
-12V

C18 .047UF 50V
C21 .47UF 25V
C17 .047UF 50V
C25 .47UF 25V
C29 .047UF 50V
C22 .047UF 50V
C30 .047UF 50V
C16 .047UF 50V
C23 .047UF 50V
C24 .47UF 25V
C26 .47UF 25V
C28 .47UF 25V
C34 .047UF 50V
C31 .47UF 25V
C20 .047UF 50V
C27 .47UF 50V
C5 .47UF 25V
C8 .047UF 50V
AM1 AC2 AT1 AJ1 BC2 BT1 BM1 BJ1

NOTE:
THIS CAPACITOR NETWORK SHOWS THE DESIRED LOCATION OF DECOUPLING CAPACITORS SINCE EACH CAPACITOR HAS BEEN ASSIGNED A NUMBER WHICH COINCIDES WITH THE DIPS WHICH MOST NEED DECOUPLING.

M2
BD2
+12V
C9 .47UF 25V
C10 .047UF 50V
+5VCR
C11 .047UF 50V
C12 .047UF 50V
C14 .47UF 25V
C38 .047UF 50V
C13 .047UF 50V
GND TTL

SHEET 5 OF 7

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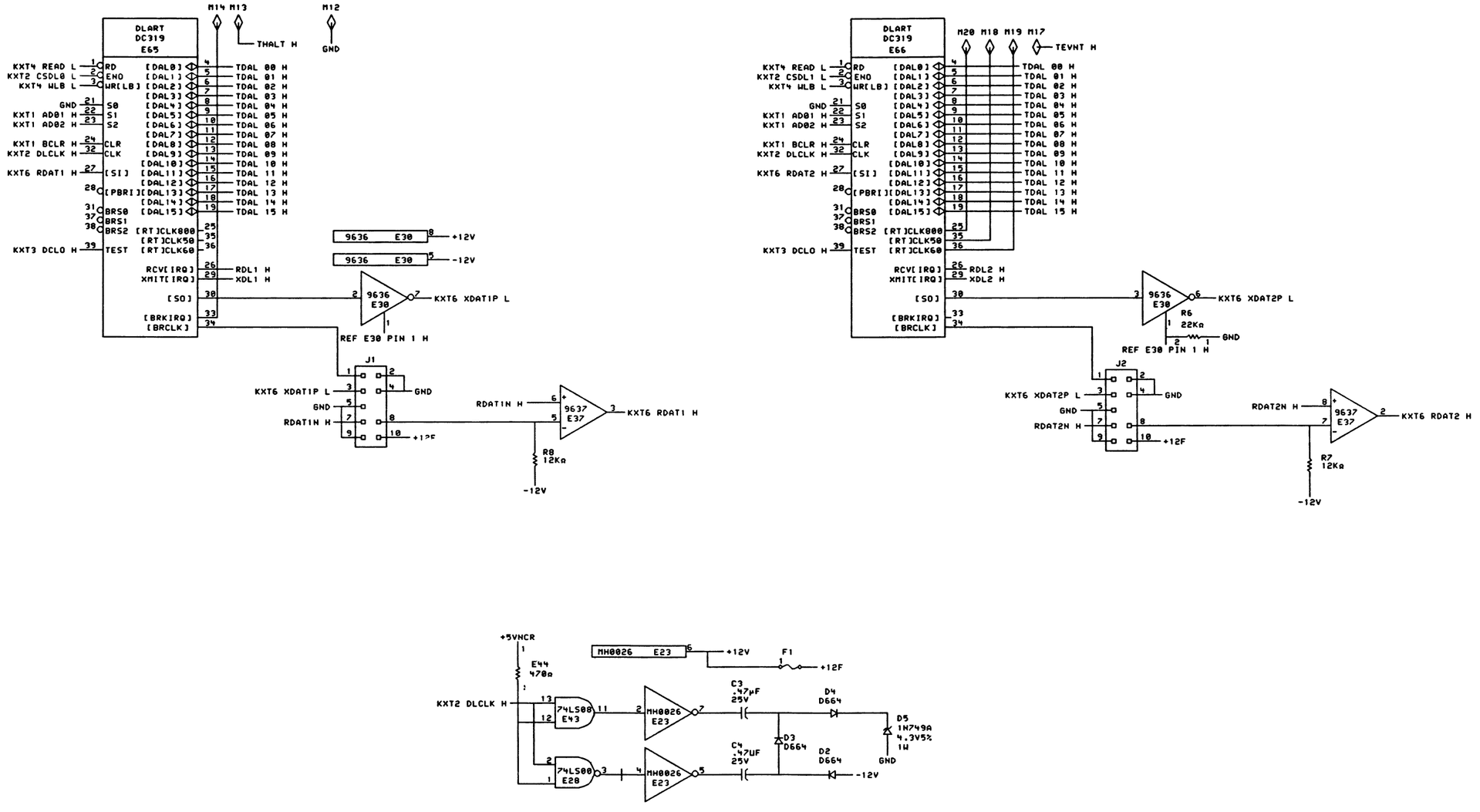
REVISIONS		
CHK	CHANGE NO.	REV
	M8063-MR3	B
R.MASKAS		

digital

DRN J.Stanley 17-MAY-82
CHK'D R.W.CAUNTER 17-MAY-82
ENG. B.MASKAS 17-MAY-82
BOARD LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
PS1:<DOWEN>KXT5.DRW 17-MAY-82 09:42
FIRST USED ON OPTION/MODEL:

TITLE: KXT11-AA MEMORY

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT5	B



SHEET 6 OF 7

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN L.Loomis 01-OCT-81 | ENG. B.Mc 01-OCT-81 | CHK J.Lawton 01-OCT-81 | BOARD LOCATION:

PS:<BOWEN.SCRATCH>KXT6.DRW 01-OCT-81 07:28 | SHEET 1 OF 1 | NEXT HIGHER ASSEMBLY:

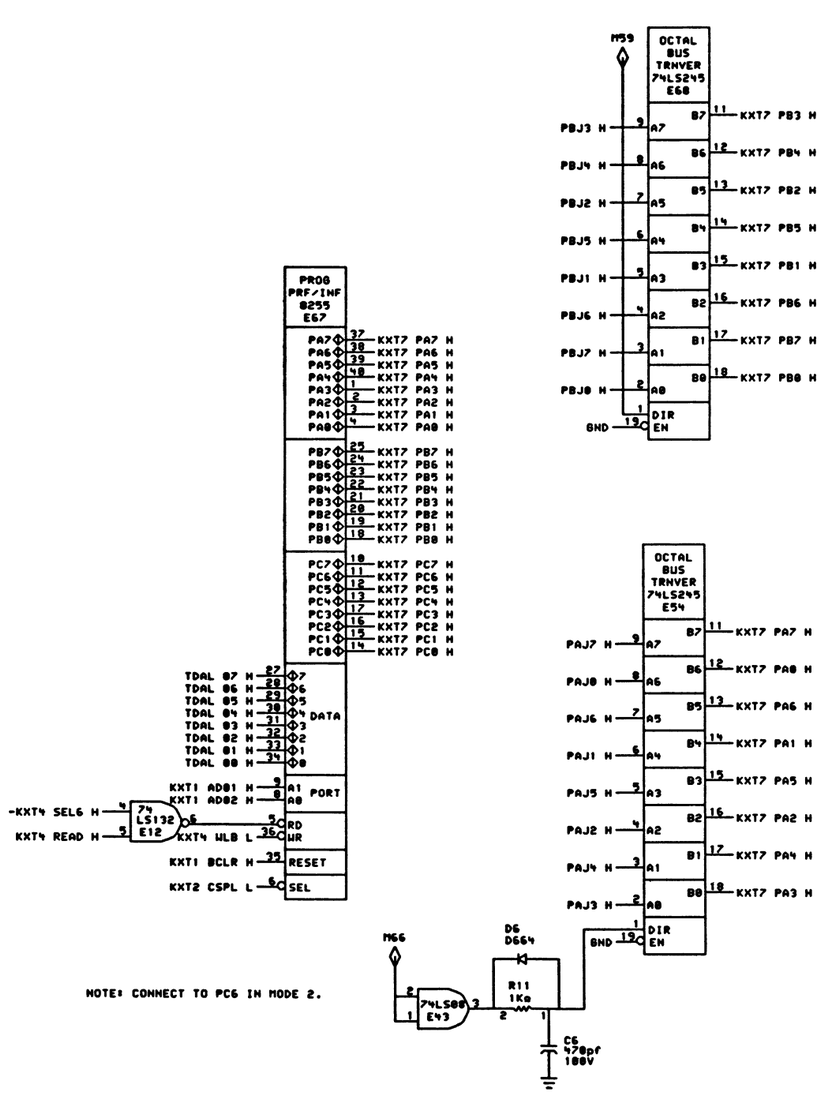
FIRST USED ON OPTION/MODEL:

TITLE: KXT11-AA SERIAL I/O

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT6	A

MET2GFR KX16.FIL 01-OCT-81 10:35:25

MET/GIP, PS:<BOWEN.SCRATCH>KXT6.DPL.1, SCALE 2. D' RELEASE BOX



SHEET 7 OF 7

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REVISIONS		
CHK	CHANGE NO.	REV
RWC	M8063-MR7	B
RWC	M8063-MR8	C
BM	M8063-MR9	D
BM	M8063-MR10	E
BM	M8063-MR11	F
BM	M8063-MR12	G
BM	M8063-MR13	H
BM	M8063-MR14	J
BM	M8063-MR15	K
BM	M8063-MR16	L
BM	M8063-MR17	M
BM	M8063-MR18	N
BM	M8063-MR19	P
BM	M8063-MR20	R
BM	M8063-MR21	S
BM	M8063-MR22	T
BM	M8063-MR23	U
BM	M8063-MR24	V
BM	M8063-MR25	W
BM	M8063-MR26	X
BM	M8063-MR27	Y
BM	M8063-MR28	Z
BM	M8063-MR29	A
BM	M8063-MR30	B

digital

DRN: D. Tansky
CHK'D: R.W. CAUMYER
DATE: 30-NOV-81
ENG: B.MASKAS
DATE: 30-NOV-81
BOARD LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
SHDC$DISK1:[ROMEW.SCRATCH]KXT7.RVB;1 13-NOV-81 13:28

TITLE: KXT11-AA PARALLEL I/O

SIZE	CODE	NUMBER	REV.
D	CS	M8063-0-KXT7	B

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MODULE VARIATION M8059-FA

NOTES
1. (A) = WIRE WRAP PIN.
2. E1 THRU E4 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING

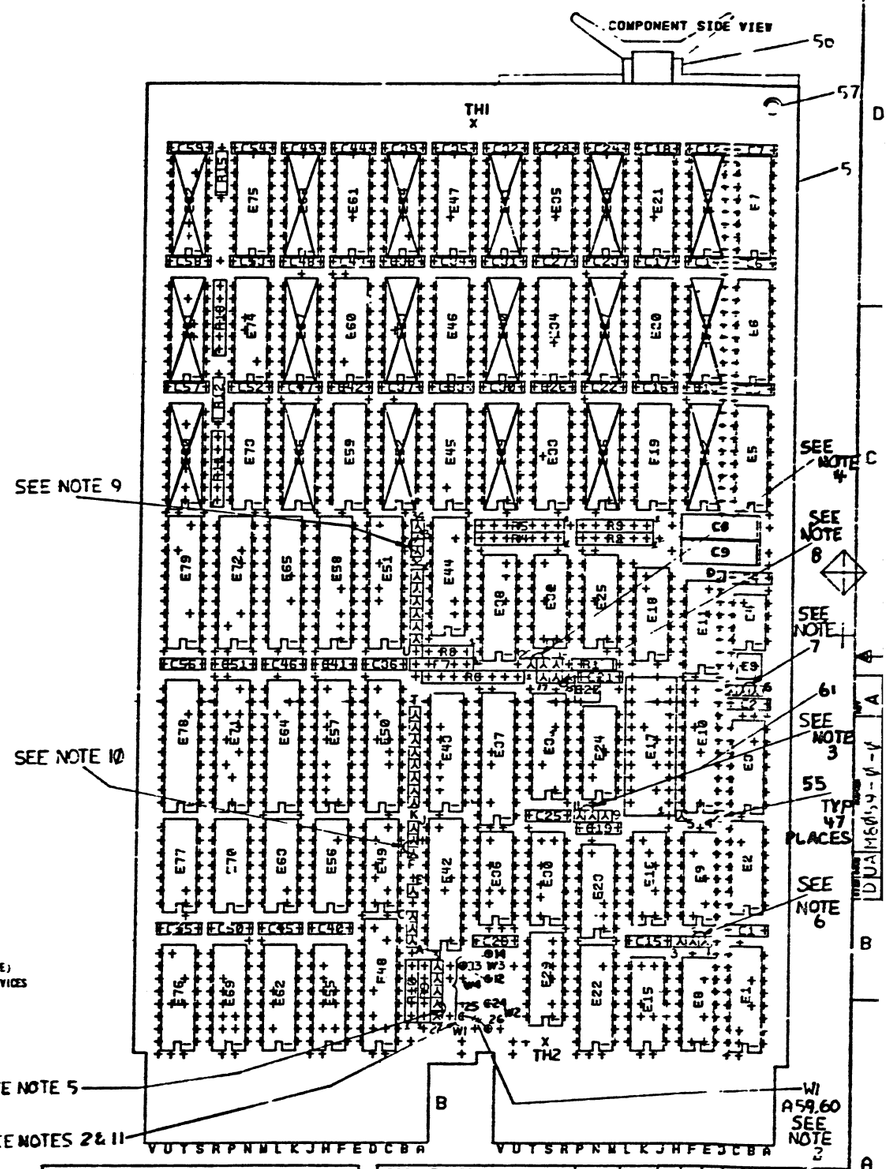


3	TYPE MEMORY	JUMPER CONFIGURATION
	NON PARITY	9 TO 10
	WITH PARITY	11 TO 10
4	TYPE MEMORY	JUMPER CONFIGURATION
	PARITY NON-CSR	18 TO 19
	PARITY WITH CSR	20 TO 19
5	PERIPHERAL PAGE SELECTION	JUMPER CONFIGURATION
	2K PERIPHERAL PAGE	29 TO 28
	4K PERIPHERAL PAGE	27 TO 28
6	PARITY ERROR REPORT	JUMPER CONFIGURATION
	REPORTED ON BIO H/L NON-CSR	3 TO 2
	REPORTED ON BIO H/L & BIO 17L WITH CSR	1 TO 2
7.	WRITE WRONG PARITY (BIT 2) DIAG BIT FOR TESTER USE	JUMPER CONFIGURATION
	WITH PARITY	6 TO 7
	NON PARITY	8 TO 7
8	REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT	JUMPER CONFIGURATION
	NORMAL OPERATION OR UPPER BANK HAS FAILED	15 TO 16
	LOWER BANK HAS FAILED	17 TO 16
9.	FULL OR ONE HALF MEMORY SELECTION	JUMPER CONFIGURATION
	FULL MEMORY SELECTION	34 TO 33
	ONE HALF MEMORY SELECTION	32 TO 33
10.	CSR SELECTION	JUMPER CONFIGURATION
	WITH CSR	F TO H
	WITHOUT CSR	J TO H
11	VOLTAGE CONNECTION	JUMPER CONFIGURATION
	+5V NON BATTERY BACKUP	26 TO 25 (51)
	+5V BATTERY BACKUP	24 TO 25 (52) 14 TO 13 (83)** OR 12 TO 13 (84)**

** AVAILABILITY FOR THE +5V BATTERY BACKUP

12 M8059-FA IS A PRIMARY VARIATION OF 64K X 18 BIT SYSTEM (NOT A MODULE TYPE)
M8059-FC, FF, FH ARE MODULE TYPES USING DIFFERENT VENDORS 64 K MOS DEVICES

13. WARNING: ALL IC'S ARE MOUNTED ON BOARD 180° FROM THE NORMAL.



NOTES: 1. THE FOLLOWING IC'S ARE NOT INSTALLED IN THE FA VARIATION: E12 THRU E14, E26 THRU E28, E39 THRU E41, E52 THRU E54, E66 THRU E68, E80 THRU E82.
2. ITEM 59 USED ONLY IN PRODUCTION TESTING

STEP	1 Y AXIS ___ STEP = ___ TIMES
REPEAT	→ X AXIS 525 ___ STEP = ___ TIMES

CHK	CHANGE NO	REV

ETCH REV. C

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH. ENG.	
PROJ. ENG.	
PROJ.	
SCALE 2:1	
SHT. 1 OF 4	
NEXT HIGHER ASSY. B-DD-M8259-A	

digital

TITLE 128K PAR/CSR MOS MEM

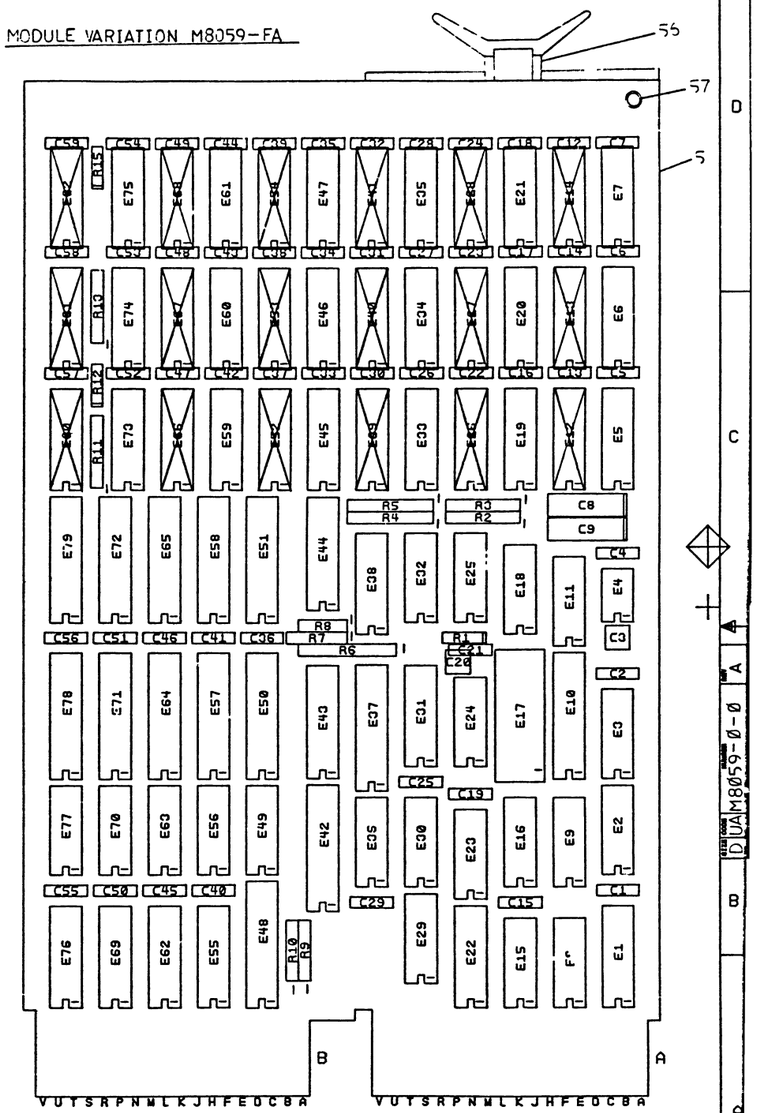
SIZE	CODE	NUMBER	REV
D	UA	M8059-Z-C	A

DUA:M8059-A-A

1 WO#_____

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MODULE VARIATION M8059-FA



NOTES:

STEP & REPEAT	↑ Y AXIS ____ STEP ____ TIMES
	→ X AXIS ____ STEP ____ TIMES

CHK	CHANGE NO	REV

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH.ENG.	
PROJ.ENG.	
PROD.	

digital

TITLE 128K PAR/CSR MOS MEM

SCALE 2:1
SHT. 2 OF 4
NEXT HIGHER ASSY. B-DD-M8059-0

SIZE	CODE	NUMBER	REV
D	UA	M8059-0-0	A

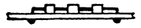
DUAM8059-0-0 A

1 WO#____

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MODULE VARIATION M8C59-KA

NOTES
1 [A] = WIRE WRAP PIN.
2 W1 THRU W4 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING



3	TYPE MEMORY	JUMPER CONFIGURATION
	NON PARITY	9 TO 10
	WITH PARITY	11 TO 10

4	TYPE MEMORY	JUMPER CONFIGURATION
	PARITY NON-CSR	18 TO 19
	PARITY WITH CSR	20 TO 19

5	PERIPHERAL PAGE SELECTION	JUMPER CONFIGURATION
	2K PERIPHERAL PAGE	29 TO 28
	4K PERIPHERAL PAGE	27 TO 28

6	PARITY ERROR REPORT	JUMPER CONFIGURATION
	REPORTED ON BAD 16L NON-CSR	3 TO 2
	REPORTED ON BAD 16L & BAD 17L WITH CSR	1 TO 2

7	WRITE WRONG PARITY (BIT 2) DIAG BIT FOR TESTER USE	JUMPER CONFIGURATION
	WITH PARITY	6 TO 7
	NON PARITY	8 TO 7

8	REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT	JUMPER CONFIGURATION
	NORMAL OPERATION OR UPPER BANK HAS FAILED	15 TO 16
	LOWER BANK HAS FAILED	17 TO 16

9.	FULL OR ONE HALF MEMORY SELECTION	JUMPER CONFIGURATION
	FULL MEMORY SELECTION	34 TO 33
	ONE HALF MEMORY SELECTION	32 TO 33

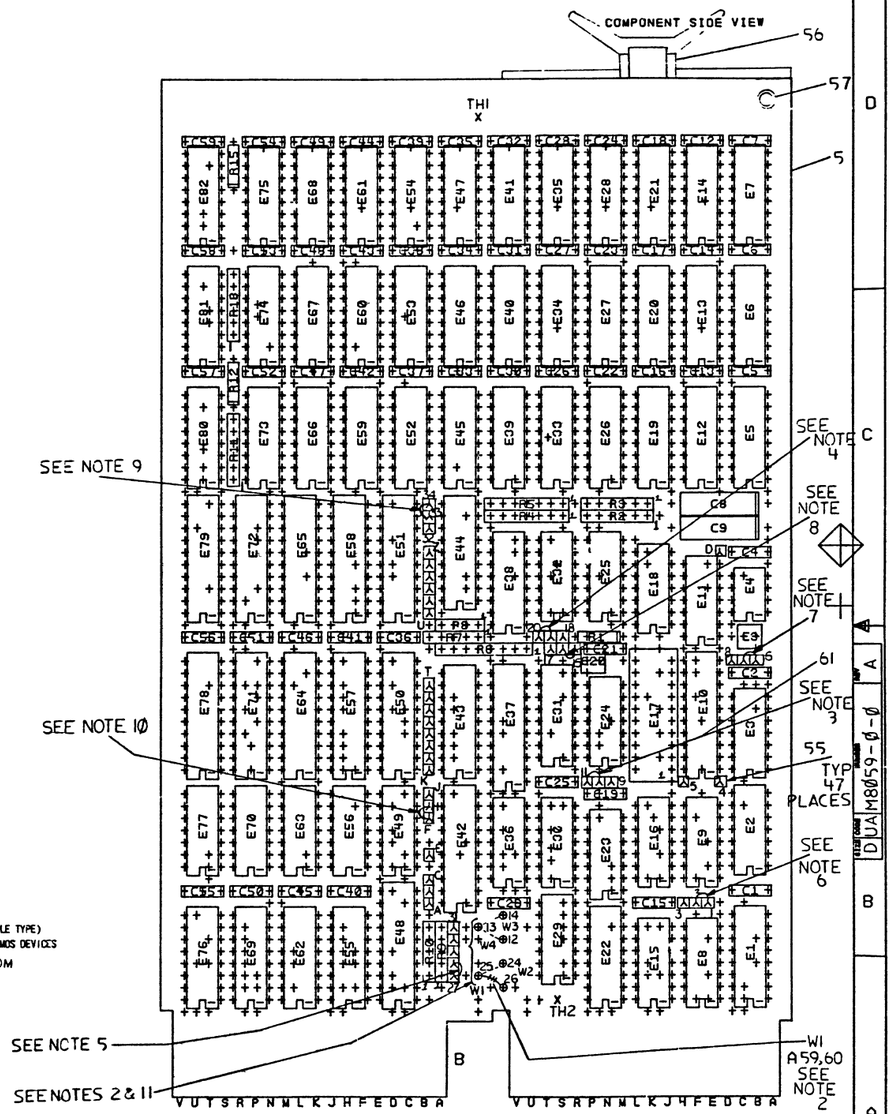
10.	CSR SELECTION	JUMPER CONFIGURATION
	WITH CSR	F TO H
	WITHOUT CSR	J TO H

11	VOLTAGE CONNECTION	JUMPER CONFIGURATION
	+5V NON BATTERY BACKUP	26 TO 25 (W1)
	+5V BATTERY BACKUP	24 TO 25 (W2) 14 TO 13 (W3)** OR 12 TO 13 (W4)**

**=AVAILABILITY FOR THE +5V BATTERY BACKUP

12 M8059-KA IS A PRIMARY VARIATION OF 128K X 18 BIT SYSTEM (NOT A MODULE TYPE)
M8059- KC,KF,KH ARE MODULE TYPES USING DIFFERENT VENDORS 64 K MOS DEVICES

13 WARNING : ALL IC'S ARE MOUNTED ON BOARD 180° FROM THE NORMAL.



NOTES: 1. ITEM 58 USED ONLY IN PRODUCTION TESTING

STEP & REPEAT	↑ Y AXIS ____ STEP ____ TIMES
	→ X AXIS ____ STEP ____ TIMES

CHK	CHANGE NO	REV

ETCH REV. C

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH.ENG.	
PROJ.ENG.	
PROD.	

digital

TITLE 128K PAR/CSR MOS MEM

SCALE 2:1 SHT 3 OF 4

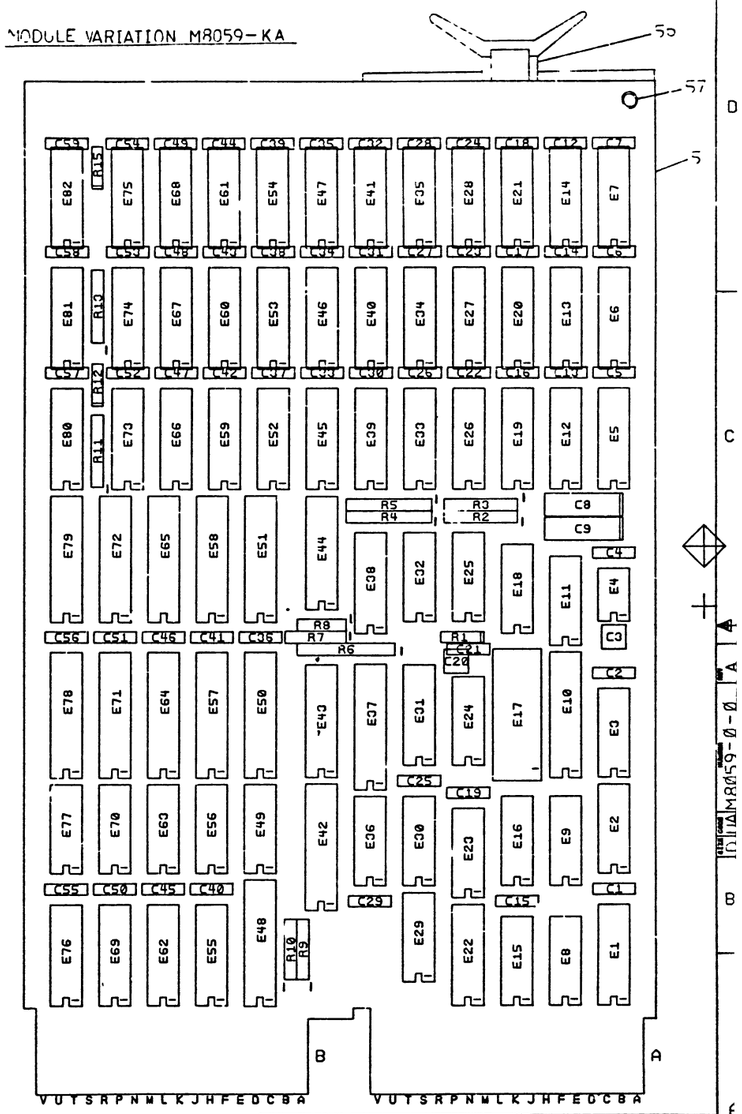
SIZE	CODE	NUMBER	REV
D	UA	M8059-0-2	A

NEXT HIGHER ASSY. B-DD-M8059-0

DUA M8059-0-0 A

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MODULE VARIATION M8059-KA



NOTES:

STEP & REPEAT	↑ Y AXIS	STEP	TIMES
	→ X AXIS	STEP	TIMES

CHANGE NO	REV

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH.ENG.	
PROJ.ENG.	
PROD.	

digital

TITLE 128K PAR/CSR MOS MEM

SCALE 2:1 | SIZE D | CODE UA | NUMBER M8059-0-0 | REV A

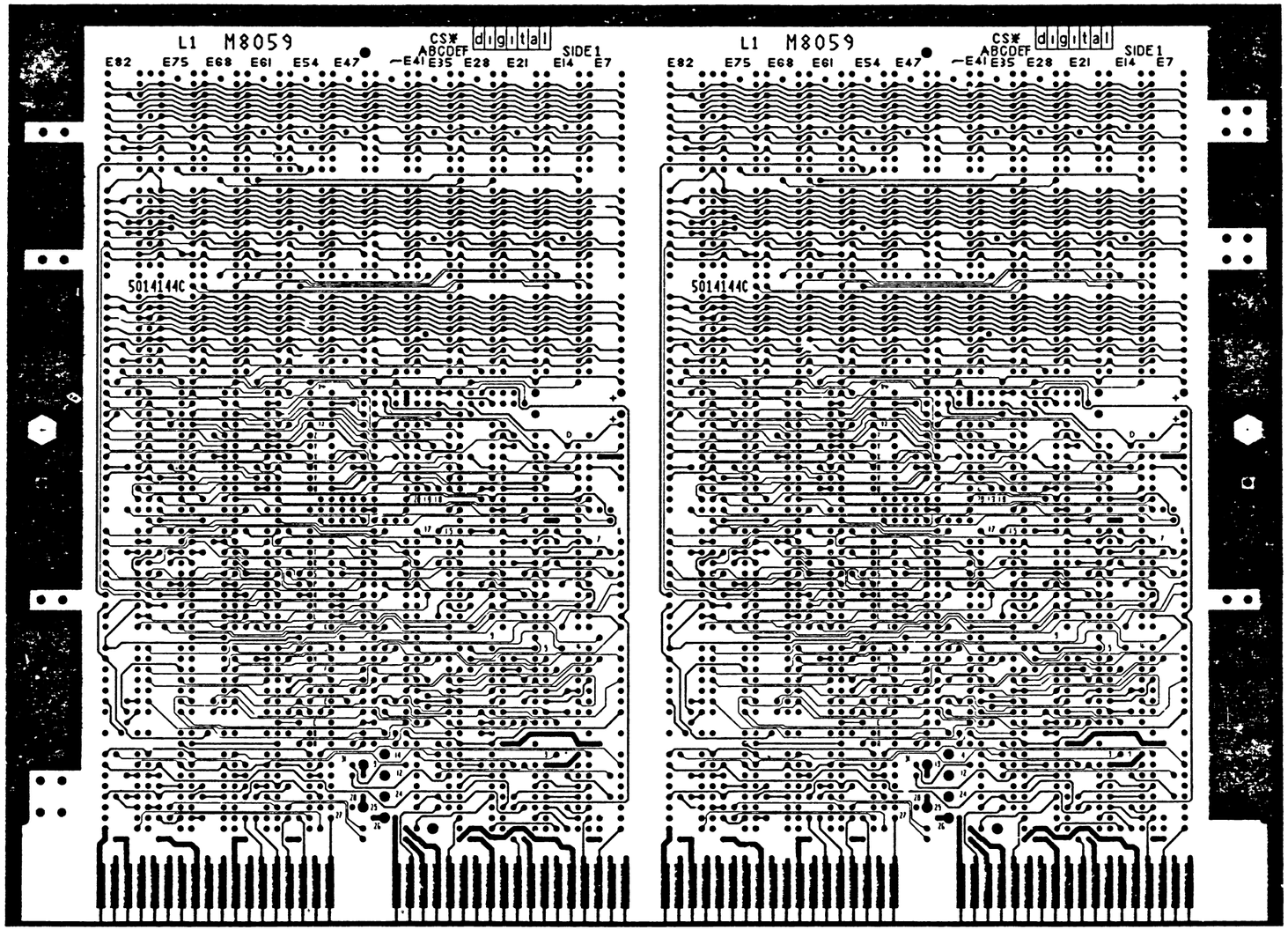
SHT 4 OF 4

NEXT HIGHER ASSY. B-DD-M8059-0

MTA M8059-0-0-A

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LAYER 1



NOTES:

CHK	CHANGE NO.	REV

SIGNATURES	DATE
DRN. V.W.	3-Feb-82
CHK'D.	
ENG.	
PROJ. ENG.	
PROD.	

digital

TITLE: ETCH CUT DRAWING

SCALE	SIZE	CODE	NUMBER	REV
2:1	D	EC	5014144-0-0	A

SHT. 1 OF 2

ETCH REV C | FIRST USED ON M8059-

LAYER 4

L4 SIDE 2

128K PAM/CSR MOS MEM 5014144C

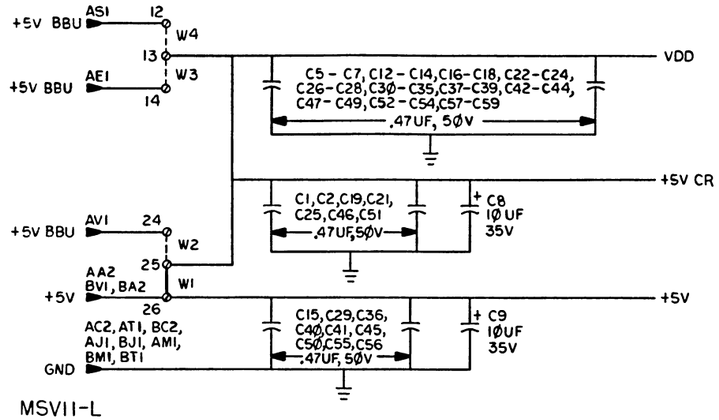
L4 SIDE 2

128K PAM/CSR MOS MEM 5014144C

TITLE	SIZE	CODE	NUMBER	REV
ETCH CUT DRAWING	D	EC	5014144-0-0	A
SCALE 2:1 SHEET 2 OF 2	DIST			

DEC 5014144-0-0 A

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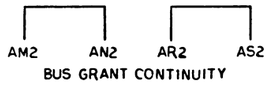
MSVII-L

STARTING ADDRESS DECIMAL (K)	STARTING ADDRESS OCTAL	JUMPERS IN (X) TO GROUND (U) Z	Y	X	W	V	COMMENTS
0	000000000						NOTE: TO OBTAIN ANY STARTING ADDRESS ON 4KW BOUNDARIES FROM 0-124KW, WIREWRAP DAISEY CHAIN FASHION FROM PIN "U" WHICH IS GROUNDED TO EACH SUCCESSIVE PIN LABELED WITH "X" FOR THAT ADDRESS.
4	000020000					X	
8	000040000				X		
12	000060000				X	X	
16	000100000			X			
20	12			X		X	
24	14			X	X		
28	16			X	X	X	
32	20		X				
36	22		X			X	
40	24		X		X		
44	26		X		X	X	
48	30		X	X			
52	32		X	X		X	
56	34		X	X	X		
60	36		X	X	X	X	
64	40	X					
68	42	X				X	
72	44	X			X		
76	46	X			X	X	
80	50	X		X			
84	52	X		X		X	
88	54	X		X	X		
92	56	X		X	X	X	
96	60	X	X				
100	62	X	X			X	
104	64	X	X		X		
108	66	X	X		X	X	
112	70	X	X	X			
116	72	X	X	X		X	
120	74	X	X	X	X		
124	00760000	X	X	X	X	X	

22 BIT CSR ADDRESS	18 BIT CSR ADDRESS	JUMPERS IN (X) TO GROUND (E) C	B	A	COMMENTS
17772100	772100				NOTE: TO OBTAIN ANY 1 OF 8 CSR ADDRESSES, WIREWRAP DAISEY CHAIN FASHION FROM PIN "E" WHICH IS GROUNDED TO EACH SUCCESSIVE PIN LABELED "X" FOR THAT ADDRESS.
102	102			X	
104	104		X		
106	106		X	X	
110	110	X			
112	112	X		X	
114	114	X	X		
17772116	772116	X	X	X	

PARTIAL STARTING ADDRESS RANGE DECIMAL (K)	OCTAL	JUMPERS IN (X) TO GROUND (K) P	N	M	L	COMMENTS
000-124	00000000-00760000					NOTE: A PARTIAL STARTING ADDRESS, ON INCREMENTAL 128K BOUNDARIES, FROM 0-2044KW MAY BE OBTAINED BY: WIREWRAP DAISEY CHAIN FASHION FROM PIN "K" WHICH IS GROUNDED TO EACH SUCESSIVE PIN LABELED "X" FOR THAT ADDRESS. TO OBTAIN ANY 4K BOUNDARY WITHIN THE 128K PARTIAL RANGE, GO TO THE STARTING ADDRESS TABLE AND CONTINUE WITH THE 4K INSTRUCTIONS.
128-252	01000000-01760000				X	
256-380	02000000-02760000			X		
384-508	03000000-03760000			X	X	
512-636	04000000-04760000		X			
640-764	05000000-05760000		X		X	
768-892	06000000-06760000		X	X		
896-1020	07000000-07760000		X	X	X	
1024-1148	10000000-10760000	X				
1152-1276	11000000-11760000	X			X	
1280-1404	12000000-12760000	X		X		
1408-1532	13000000-13760000	X		X	X	
1536-1660	14000000-14760000	X	X			
1664-1788	15000000-15760000	X	X		X	
1792-1916	16000000-16760000	X	X	X		
1920-2044	17000000-17760000	X	X	X	X	

IC TYPE	+5V	GND
1K X 4 PROM	18	9
555 (VDD IS +5V)	4,8	1
74S02,74S03,74S10,74S11,74S20, 74S32,74S37,74S64,74S74,74S280	14	7
74LS240	20	1,10,19
16C1,16L8,16R4,16R8,74S373,74LS373	20	10
74LS75	5	12
8640	8	1
8641,74LS175	16	8
2908	20	5,15
64K RAM (1 VOLTAGE)	1,8	16



NOTE 12.

VOLTAGE CONNECTION	JUMPER CONFIGURATION
+5V NON-BATTERY BACKUP	26 TO 25 (W1)
+5V BATTERY BACKUP	24 TO 25 (W2) 14 TO 13 (W3)** OR 12 TO 13 (W4)**

** = AVAILABILITY FOR THE +5V BATTERY BACK UP.
* = INDICATES BATTERY BACKUP.

NOTE 13.
SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:

[X] SIGNAL NAME [Y/Z]
- [X] — SOURCE SHEET NUMBER.
- Y — DESTINATION SHEET NUMBER.
- Z — NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.

NOTES:
1. @ = WIRE WRAP PIN
2.

TYPE MEMORY	JUMPER CONFIGURATION
NON PARITY	9 TO 10
WITH PARITY	11 TO 10

3.

TYPE MEMORY	JUMPER CONFIGURATION
PARITY NON-CSR	18 TO 19
PARITY WITH CSR	20 TO 19

4.

PERIPHERAL PAGE SELECTION	JUMPER CONFIGURATION
2K PERIPHERAL PAGE	29 TO 28
4K PERIPHERAL PAGE	27 TO 28

5.

PARITY ERROR REPORT	JUMPER CONFIGURATION
REPORTED ON BAD 16 L NON-CSR	3 TO 2
REPORTED ON BAD 16 L & BAD 17 L WITH CSR	1 TO 2

6.

WRITE WRONG PARITY DIAG. BIT FOR TESTER USE	JUMPER CONFIGURATION
ENABLE	6 TO 7
DISABLE	8 TO 7

7. JUMPER BETWEEN PIN 30 AND 31 USED FOR MANUFACTURING TEST ONLY. FOR NORMAL OPERATION, IT IS OUT.
8.

REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT	JUMPER CONFIGURATION
NORMAL OPERATION OR UPPER BANK HAS FAILED .	15 TO 16
LOWER BANK HAS FAILED	17 TO 16

9.

FULL OR ONE HALF MEMORY SELECTION	JUMPER CONFIGURATION
FULL MEMORY SELECTION	34 TO 33
ONE HALF MEMORY SELECTION	32 TO 33

10.

CSR SELECTION	JUMPER CONFIGURATION
WITH CSR	F TO H
WITHOUT CSR	J TO H

11.

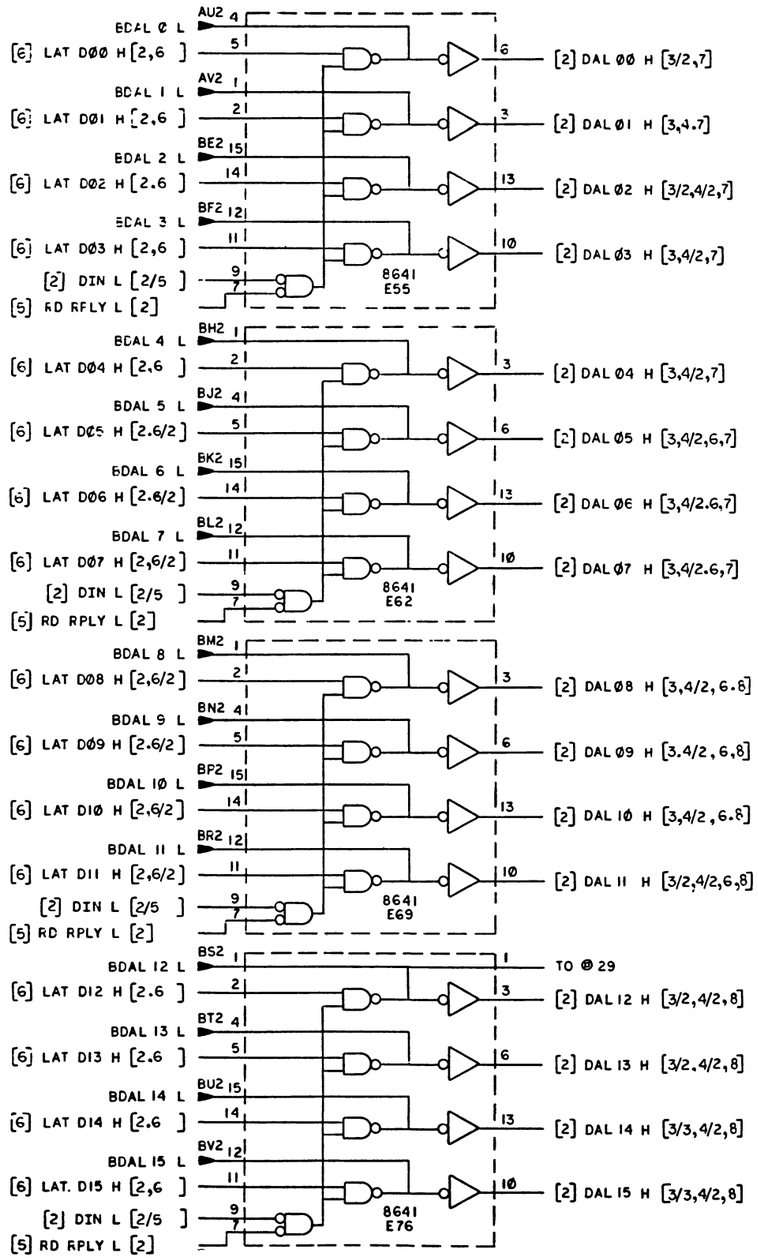
EXTENDED OR NORMAL MEMORY SELECTION	JUMPER CONFIGURATION
NORMAL OPERATION (128K)	NO JUMPER BETWEEN R TO T
EXTENDED OPERATION (2M. WORDS)	INSTALL JUMPER BETWEEN R TO T

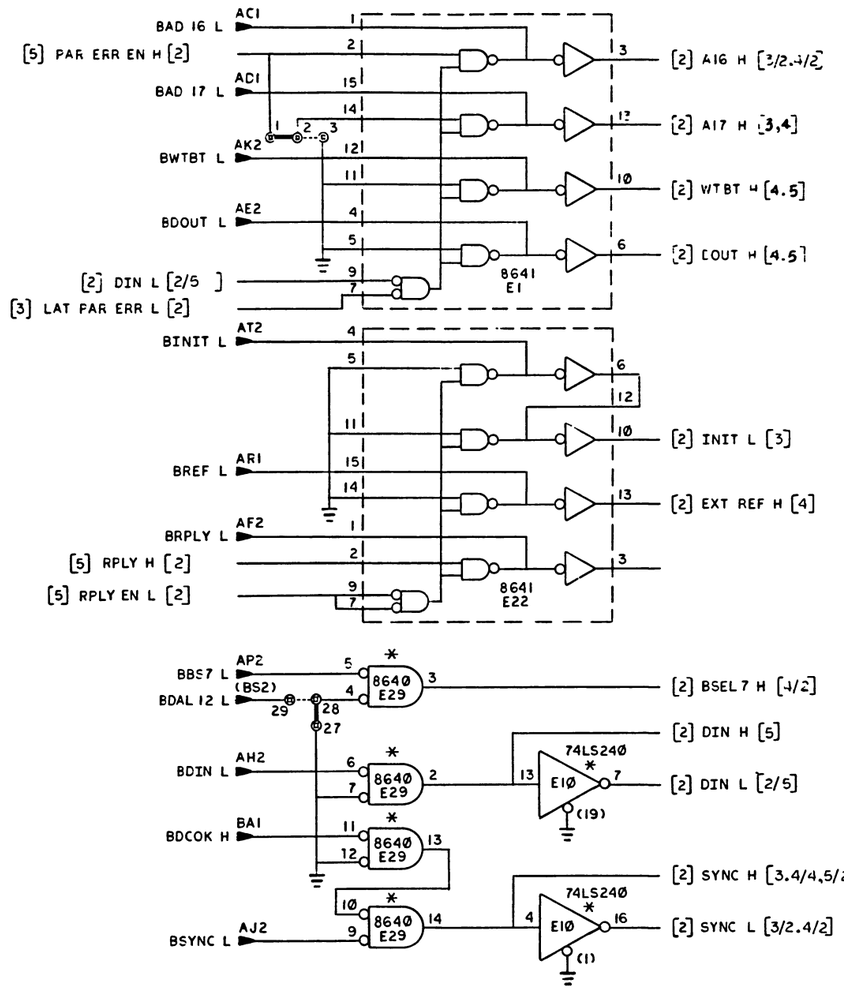
REVISIONS			
ONE	CHANGE NO.	REV.	
RK	M8059-SH002	B	
	R. GIVEN		
	G. Emery		

DRN. Greg D'Arbo	12/10/81	FIRST USED ON MSVII-L
CHK'D P. Bisignano	27 may 82	digital
ENG. R. Hixon	27 MAY 82	TITLE 128K PAR/CSR MOS MEM
PROJ. ENG. R. Hixon	27 MAY 82	
PROD. Janet Rollwitz	JUN 2, 82	
NEXT HIGHER ASSY.		
SCALE —		SIZE D CODE CS NUMBER M8059-0-1 REV. B
SHEET 1 OF 8		DIST.

M8059-0-1 REV B SIZE D CODE CS SHEET 1 OF 8

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8059-0-1	B
SCALE —//— SHEET 2 OF 8	DIST.			

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[2] DAL 00 H [3/2,7] → 74S280 E56 D6 EVEN → [3] PDI 16 H [7]
[2] DAL 01 H [3,4/2,7] → D7
[2] DAL 02 H [3/2,4/2,7] → D2
[2] DAL 03 H [3,4/2,7] → D3
[2] DAL 04 H [3,4/2,7] → D5
[2] DAL 05 H [3,4/2,6,7] → D4
[2] DAL 06 H [3,4/2,6,7] → D1
[2] DAL 07 H [3,4/2,6,7] → D0 ODD
[3] CSR 02 H [3,6] , [2] A16 H [3/2,4/2] → 16R4 E50 (23-003×3-00)

[2] DAL 08 H [3,4/2,6,8] → 74S280 E70 D7 EVEN → [3] PDI 17 H [8]
[2] DAL 09 H [3,4/2,6,8] → D6
[2] DAL 10 H [3,4/2,6,8] → D2
[2] DAL 11 H [3/2,4/2,6,8] → D3
[2] DAL 12 H [3/2,4/2,8] → D5
[2] DAL 13 H [3/2,4/2,8] → D4
[2] DAL 14 H [3/2,4/2,8] → D1
[2] DAL 15 H [3/3,4/2,8] → D0 ODD

[7] DO 00 H [3,6] → 74S280 E63 D3 EVEN
[7] DO 01 H [3,6] → D1
[7] DO 02 H [3,6] → D8
[7] DO 03 H [3,6] → D0
[7] DO 04 H [3,6] → D6
[7] DO 05 H [3,6] → D7
[7] DO 06 H [3,6] → D4
[7] DO 07 H [3,6] → D2 ODD
[7] PDO 16 H [3,6] → D5

[8] PDO 17 H [3,6] → 74S280 E77 D5 EVEN
[8] DO 08 H [3,6] → D2
[8] DO 09 H [3,6] → D1
[8] DO 10 H [3,6] → D6
[8] DO 11 H [3,6] → D0
[8] DO 12 H [3,6] → D7
[8] DO 13 H [3,6] → D8
[8] DO 14 H [3,6] → D4
[8] DO 15 H [3,6] → D3 ODD

+5V → R10 5K 5K 5K 5K
BDAL 18 L → BC1
BDAL 19 L → BD1
BDAL 20 L → BE1
BDAL 21 L → BF1
[6] REF CLK H [3,5] → 2908 E48
→ [3] LAT A18 H [4,6]
→ [3] LAT A19 H [4,6]
→ [3] LAT A20 H [4,6]
→ [3] LAT A21 H [4,6]
[2] SYNC H [3/4/5/2]

+5VCR → R61 5K, R3 5K → 74S37 E32

[2] DAL 11 H [3/2,4/2,6,8] → 74LS373 E51 D0 R0(1) → [3] LAT A11 H [6]
[2] DAL 12 H [3/2,4/2,8] → D1 R1(1) → [3] LAT A12 H [6]
[2] DAL 13 H [3/2,4/2,8] → D2 R2(1) → [3] LAT A13 H [6]
[2] DAL 14 H [3/3,4/2,8] → D3 R3(1) → [3] LAT A14 H [6]
[2] DAL 15 H [3/3,4/2,8] → D4 R4(1) → [3] LAT A15 H [6]
[2] A16 H [3/2,4/2] → D5 R5(1) → [3] LAT A16 H [6]
[2] A17 H [3,4] → D6 R6(1) → [3] LAT A17 H [6]
[2] DAL 00 H [3/2,7] → D7 R7(1) → [3] LAT A00 H [5]
EN OC
[2] SYNC L [3/2,4/2]

[3] +3.5V [3,4/2]
[2] DAL 00 H [3/2,7] → 74LS175 E38 D3 R3(1) → [3] CSR 00 H [5,6]
[2] DAL 02 H [3/2,4/2,7] → D2 R2(1) → [3] CSR 02 H [3,6]
[2] DAL 14 H [3/3,4/2,8] → D1 R1(1) → [3] CSR 14 P H [5]
D0 R0(1) → [3] +3.5V [3,4/2]
CLK CLR
[5] CSR PRCLK H [3/3]
[2] INIT L [3]

[5] DL 350 H [3], [5] MEM RD L [3] → 74S02 E2 → 74S20 E16 (with [3] LAT PAR ERR H [3], [5] DL 300 H [3])
→ 74LS240 E10 → [3] PAR ERR CLK H [6]
[5] CSR PRCLK H [3/3] → 74S32 E24 → [3] CSR CLK H [6/2]

[2] DAL 15 H [3/3,4/2,8] → 74S74 E15 D → [3] CSR 15 H [6]
[5] CSR PRCLK H [3/3] → C
PR CLR
[2] INIT L [3]

74LS175 E31
D0 R0(1) → [3] LAT PAR ERR H [3]
R0(0) → [3] LAT PAR ERR L [2]
D1 R1(1), R1(0)
[4] CSR SEL H [3] → D2 R2(1) → [3] LAT CSR SEL H [6/4]
R2(0) → [3] LAT CSR SEL L [5/2]
[4] RAS SEL L [3] → D3 R3(1), R3(0) → [3] LAT RAS H [5]
ENB1 ENB2
[4] DAT LAT L [3,6/2]
[2] SYNC L [3/2,4/2]

(PARITY AND CHECK BIT GENERATION, BUS ADDRESS RECEIVER LATCH, CSR ERROR ADDRESS STORAGE AND CSR BITS 00,02,14 AND 15

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8059-0-1	B
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NOTE : RESISTORS R11,R12,R13 AND R15 ARE 22Ω IN THE FA VARIATION.

[2] DAL Ø1 H [3,4/2,7]
[2] DAL Ø2 H [3/2,4/2,7]
[2] DAL Ø3 H [3,4/2.7]
[2] DAL Ø4 H [3,4/2.7]
[2] DAL Ø5 H [3,4/2,6.7]
[2] DAL Ø6 H [3,4/2.6.7]
[2] DAL 14 H [3/2,4/2,5]
[2] DAL 15 H [3/2,4/2,5]
[2] SYNC L [3/2,4/2]
[5] DL55 H [4,5]
[5] REF H [4/2,5/3]
74S373-Ø1 E65
74S32 E24

[2] DAL Ø7 H [3,4/2,6.7]
[2] DAL Ø8 H [3,4/2,6,8]
[2] DAL Ø9 H [3,4/2,6.8]
[2] DAL 10 H [3,4/2.6.7]
[2] DAL 11 H [3/2,4/2,6,8]
[2] DAL 12 H [3/2,4/2.8]
[2] DAL 13 H [3/2,4/2.8]
[2] A16 H [3/2,4/2]
[2] SYNC L [3/2,4/2]
74S373-Ø1 E79

[5] DLØ H [4/2,5]
[5] REF L [4/2,5/4]
74S10 E11

+5VCR
R6 500
[5] DLØ H [4/2, 5]
[5] REF H [4/2,5/3]
74S03 E18

[3] +3.5V [3,4/2]
[5] REF REQ L [4,5]
16R8 E72 (23ØØ1K5-ØØ)

R13 18 [4] MUX A1 H [7/2.8/2]
R13 18 [4] MUX A2 H [7/2.8/2]
R11 18 [4] MUX A3 H [7/2,8/2]
R11 18 [4] MUX A4 H [7/2,8/2]
R13 18 [4] MUX A5 H [7/2.8/2]
R12 18 [4] MUX A6 H [7/2,8/2]
R11 18 [4] MUX A7 H [7/2.8/2]
R15 18 [4] MUX A8 H [7/2,8/2]

+5V
R9 5K R9 5K R9 5K R9 5K
[2] DAL 12 H [3/2,4/2,8]
[2] DAL 11 H [3/2,4/2,6,8]
[2] DAL 10 H [3,4/2,6.8]
[2] DAL Ø9 H [3,4/2.6.8]
[2] DAL Ø8 H [3,4/2.6.8]
[2 DAL Ø7 H [3,4/2.6.7]
[2] DAL Ø6 H [3,4/2.6.7]
[2] DAL Ø5 H [3,4/2,6.7]
[2] BSEL7 H [4/2]
[2] DAL Ø4 H [3,4/2.7]
[2] DAL Ø3 H [3,4/2,7]
[2] DAL Ø2 H [3/2,4/2,7]
[2] DAL Ø1 H [3,4/2,7]
16C1 E42 (23ØØ1J6-ØØ)
[4] CSR SEL H [3]

+5V CR
R6 5K R6 5K
+5V
R7 5K R7 5K
[3] LAT A21 H [4,6]
[3] LAT A20 H [4.6]
[3] LAT A19 H [4.6]
[3] LAT A18 H [4.6]
[2] EXT REF H [4]
[2] BSEL7 H [4/2]
1K X4 PROM E43 (2362ØFI-ØØ)

+5V
R7 5K R7 5K
R8 5K R8 5K R8 5K
SA16 L AUI
SEE NOTE 7 ON SHEET 1
[2] A17 H [3,4]
[2] A16 H [3/2,4/2]
[2] DAL 15 H [3/2,4/2,8]
[2] DAL 14 H [3/3,4/2,8]
[2] DAL 13 H [3/2,4/2,8]
1K X4 PROM E44 (23696FI-ØØ)
[3] +3.5V [3,4/2]
[4] RAS SEL L [3]

74S64 E49

+5VCR
R6 1K
+3V BBU
[2] WTBT H [4,5]
74S02 E2
74S74 E9
[2] SYNC H [3,4/4,5/2]
[4] RD END L [4]
[4] RD REQ H [4]
[4] RD REQ L [4/2,5/3]
[4] WT END L [4]
[4] WT REQ L [5]
[2] DOUT H [4,5]
74S03 E18
[4] DAT LAT H [4]
8640 E8
[4] RD END L [4]
[2] SYNC H [3,4/4,5/6]
[4] RD REQ H [4]
[4] WT END L [4]

+3V BBU
[5] DL14Ø H [4.5/2]
[5] DL28Ø L [4]
[5] REF L [4/2,5/3]
74S10 E30
74S74 E15
[2] SYNC H [3,4/4,5/2]
[4] DAT LAT H [4]
[4] DAT LAT L [3,6/2]

(ARRAY ADDRESS MUX DRIVERS STARTING ADDRESS SELECTION, CSR ADDRESS SELECTION AND R/W CYCLE.)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8059-0-1	B
SCALE —//— SHEET 4 OF 8	DIST.			

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+5VCR R3 5K
+3VBBU
S
AK1
REF INH L
74S74 E3 (0,1)
[6] REF CLK H [3,5]
[5] DL140 L [5/3]
[5] DL220 H [5/2]
[5] REF CLR EN H [5]
74S10 E30
[5] REF REQ L [4,5]
[4] RD REQ L [4/2,5/3]
[4] WT REQ L [5]
[5] DL140 L [5/3]
[5] DL220 L [5/4]
74S10 E11
74S11 E23
74LS240 E10 (19)
74S03 E18
R1 19.6,1%
+5VCR R2 1.5K
R2 210
C20 220PF 1%
74LS240 E10 (1)
74LS240 E10
[5] REF REQ L [4,5]
+3VBBU
[5] REF H [4/2,5/3]
[5] REF L [4/2,5/4]
[5] DL140 H [4,5/2]
74S02 E2
[5] DL140 L [5/3]
[5] DL220 H [5/2]
74LS240 E10
[5] DL220 L [5/4]
[5] DL280 H [5]
74S10 E30
[5] DL280 L [4]
BUF. DELAY LINE E17
+5VCR
[5] DL350 H [3]
[5] DL300 H [3]
[5] DL280 H [5]
[5] DL220 H [5/2]
[5] DL140 H [4,5/2]
[5] DL100 H [5/3]
[5] DL55 H [4,5/2]
[5] DLØ H [4/2,5]
@5
@4

16L8(23010J5-00) E37
DL55 H
DL140 L
DL220 L
REF H
[5] REF CLR EN H [5]
DL55 H
DL220 L
RD REQ L
REF H
LAT CSR SEL L
[5] CSR PRCLK H [3/3]
[5] DL55 H [4,5/2]
[5] DL140 L [5/3]
[5] DL220 L [5/4]
[5] REF H [4/2,5/3]
[4] RD REQ L [4/2,5/3]
[5] RD RPLY H [5]
[3] LAT CSR SEL L [5/2]
[3] CSRØØ H [5,6]
[3] CSR 14P H [5]
[5] SM SYS H [5]
RD RPLY H
CSR 14P H
LAT CSR SEL L
[5] CSR OC L [6/2]
RD RPLY H
LAT CSR SEL L
[5] OC L [6/2]
RD RPLY H
SM SYS H
CSR 14P H
LAT CSR SEL L
[5] X ADD OC L [6/2]
DL55 H
DL220 L
REF H
LAT CSR SEL L
RD REQ L
[5] MEM RD L [3]
DL140 L
RD RPLY H
LAT CSR SEL L
CSRØØ H
[5] PAR ERR EN H [2]
SM SYS H
CSR14P H
[5] CSR 14 H [6]
+5VCR R6 5K
[5] SM SYS H [5]

[5] REF H [4/2,5/3]
[3] LAT RAS H [5]
[5] REF L [4/2,5/4]
[5] DL100 H [5/3]
[5] DL 55 H [4,5/2]
[5] REF H [4/2,5/4]
[5] DLØ H [4/2,5]
[5] REF L [4/2,5/4]
[3] LAT CSR SEL L [5/2]
74S32 E24
74S10 E11
74S11 E23
74S32 E24
74S11 E23
[5] RPLY CLK H [5]
+5VCR R5 360 R5 18
74S37 E25
[5] RAS Ø L [7,8]
74S37 E32
[5] RAS 1 L [7,8]
+5VCR R4 360 R4 18
74S37 E25
[5] CAS Ø L [7/2]
[5] REF L [4/2,5/4]
[5] DL100 H [5/3]
74S37 E32
[5] CAS 1 L [8/2]

[3] LAT AØØ H [5]
[5] WT RPLY H [5]
[2] WTBT H [4,5]
16R4 E58 (B) (23004K3-00)
[5] DL220 L [5/4]
+5VCR R5 360 R5 18
74S37 E25
[5] WTBT Ø L [7/2]
74S37 E32
[5] WTBT 1 L [8/2]
+5VCR R4 360 R4 18

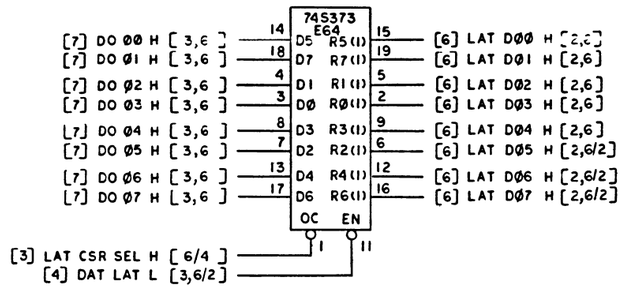
[5] WT RPLY L [5]
[5] REF L [4/2,5/4]
[5] DL220 L [5/4]
[5] DL100 H [5/3]
[5] DL140 H [4, 5/2]
74S20 E16
[2] DIN H [5]
[2] DOUT H [4,5]
74S02 E2
[5] RPLY EN L [2]
74S74 E36
[5] RD RPLY H [5]
[5] RD RPLY L [2]
[2] SYNC H [3,4/4,5/2]
74S37 E25
[5] RPLY H [2]
+3V BBU
[4] RD REQ L [4/2,5/3]
[5] RPLY CLK H [5]
[2] SYNC H [3,4/4,5/2]
74S74 E36
[5] WT RPLY H [5]
[5] WT RPLY L [5]

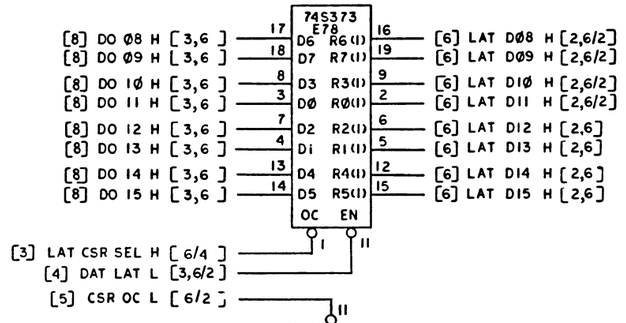
(TIMING CHAIN AND CONTROL SIGNALS)

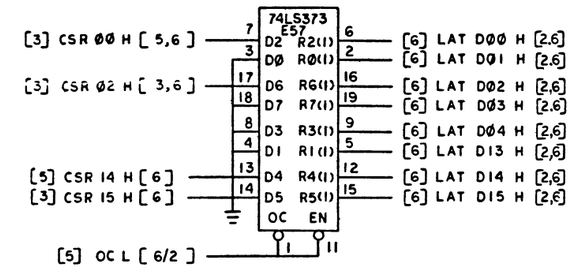
REVISIONS
CHK | CHANGE NO. | REV.

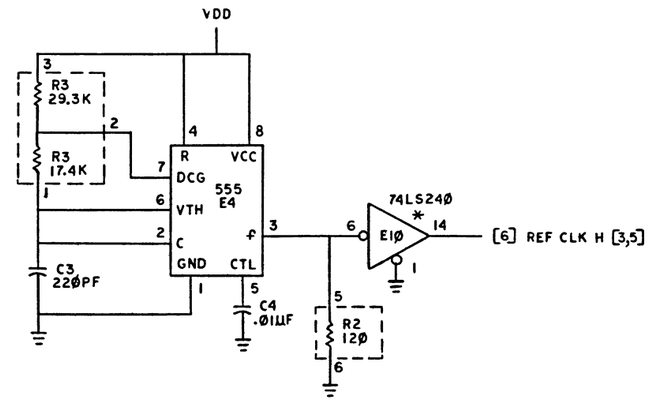
TITLE 128K PAR/CSR MOS MEM
SIZE D CODE CS NUMBER M8059-Ø-1 REV B
SCALE — SHEET 5 OF 8 DIST.

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(DATA - ADDRESS LATCHES, CSR DATA - ADDRESS LATCHES AND REF. CLK)

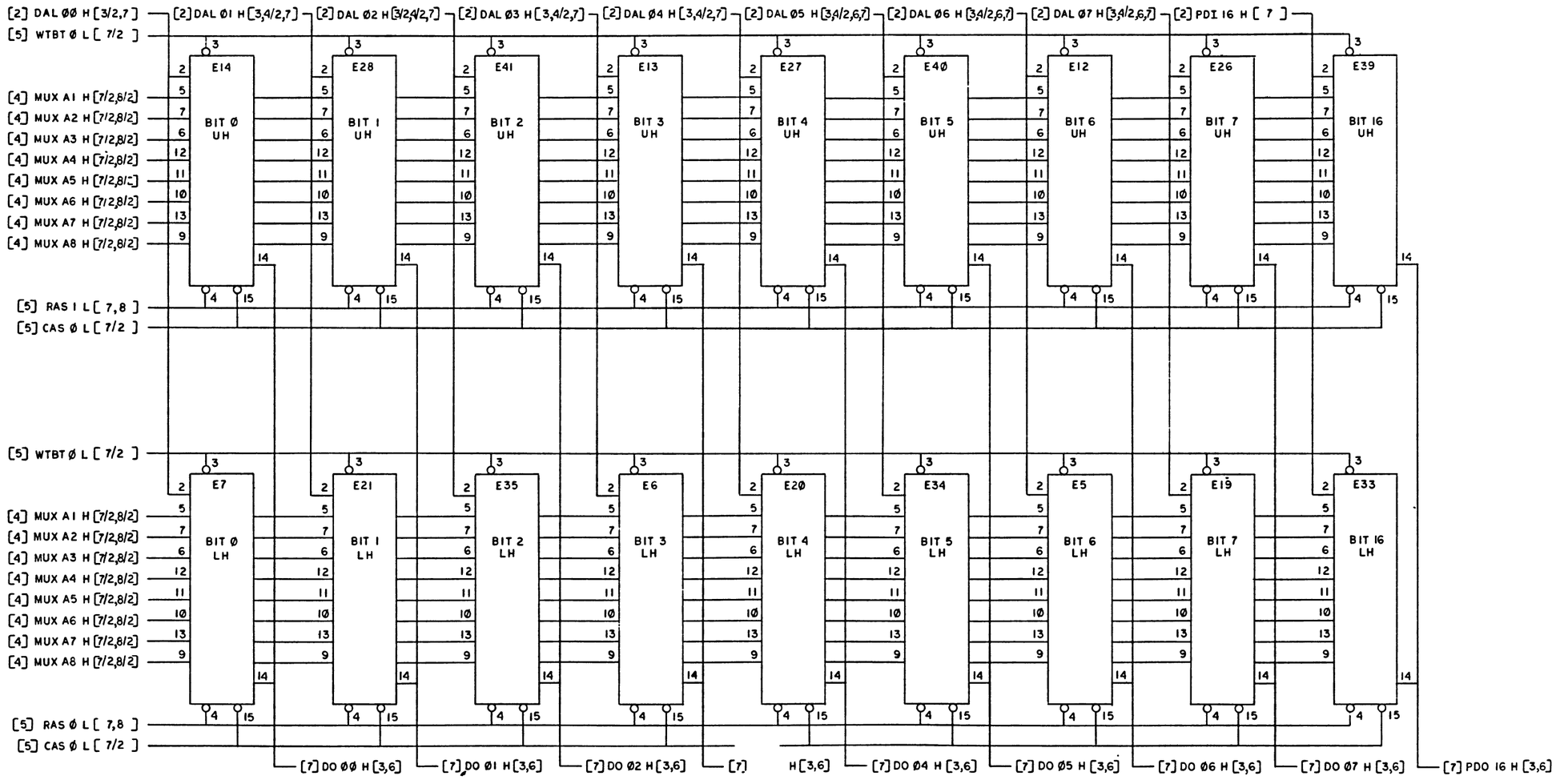
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8Ø59-Ø-1	B
SCALE —// — SHEET 6 OF 8	DIST.			

M8Ø59-Ø-1 REV B

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NOTE: THE VOLTAGE FOR ALL MOS RAMS ARE BATTERY BACK UP.



(MOS ARRAY)

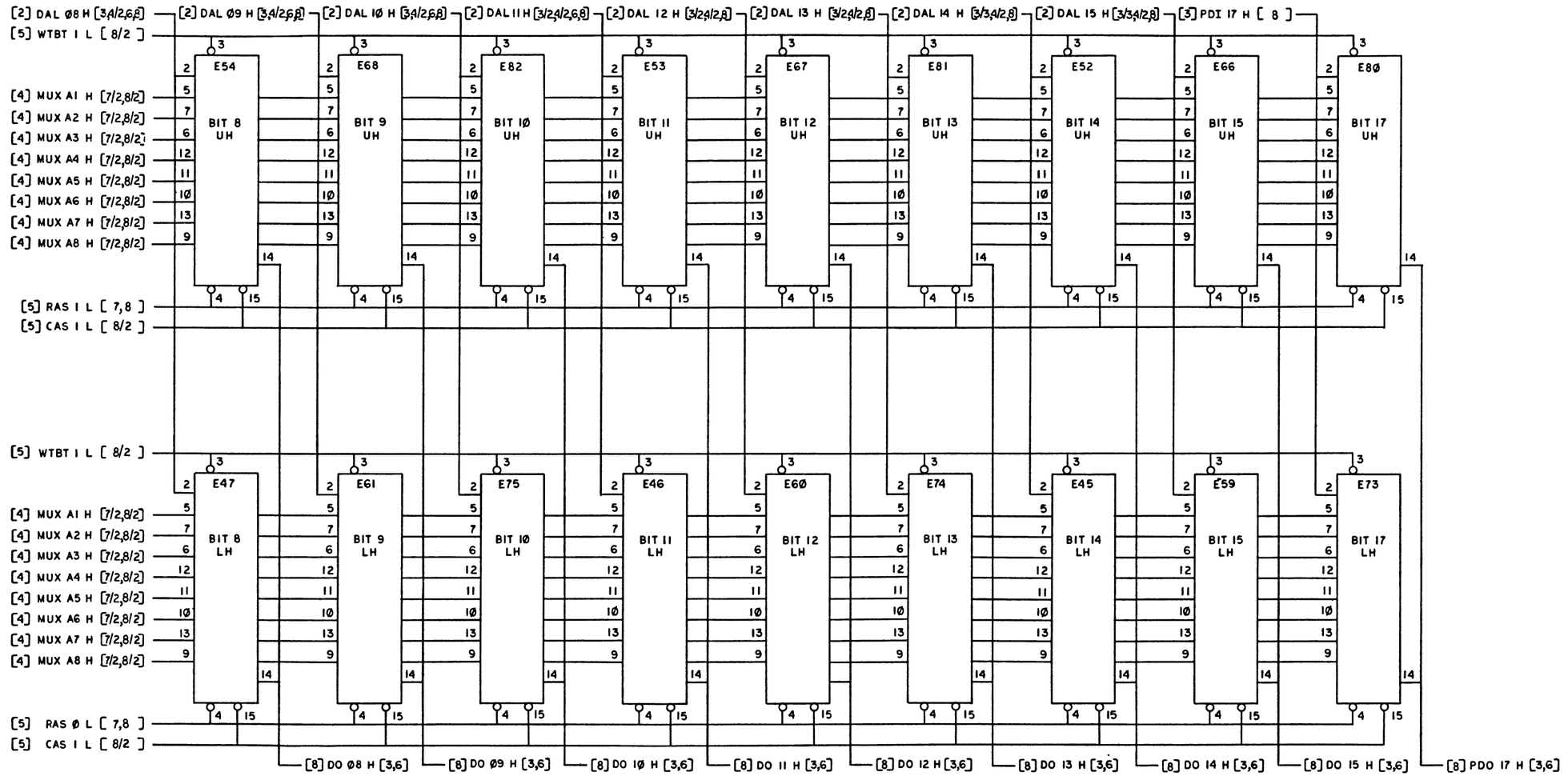
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8059-0-1	B
SCALE —	SHEET 7 OF 8	DIST.		

M8059-0-1 REV. B

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NOTE: THE VOLTAGE FOR ALL MOS RAMS ARE BATTERY BACK UP.



(MOS ARRAY)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	D	CS	M8059-Ø-1	B
SCALE —//	SHEET 8 OF 8		DIST.	

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